HFCT-5953xxxZ/HFCT-5954xxxZ

Single Mode SFF Transceivers for SONET OC-12/SDH STM-4 (S4.1)
Multirate Operation
Part of the Avago METRAK family

Datasheet

Description

The HFCT-5953xxxZ/HFCT-5954xxxZ SFF transceivers are high performance, cost effective modules for serial optical data communication applications specified at 622 Mbit/s for Intermediate Reach links. They are designed to allow multirate transmission at OC3 (155 Mbit/s) and OC12 (622 Mbit/s) providing OC12 SONET/SDH compliance.

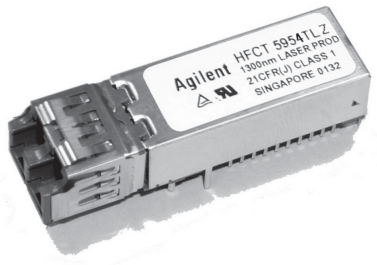
All modules are designed for single mode fiber and operate at a nominal wavelength of 1300 nm. They incorporate high performance, reliable, long wavelength optical device and proven circuit technology to give long life and consistent service.

The transmitter section consists of a Fabry Perot Laser (FP). The transmitter has full IEC 825 and CDRH Class 1 eye safety.

The receiver section uses a MOVPE grown planar PIN photodetector for low dark current and excellent responsivity.

A pseudo-ECL logic interface simplifies interface to external circuitry.

These transceivers are supplied in 2 x 5 and 2 x 10 DIP style footprint with the LC fiber connector interface and are fully compliant with SFF Multi Source Agreement (MSA).



Features

- RoHS Compliant
- Multirate operation from 155 Mbit/s to 622 Mbit/s and OC-12 SONET compliance
- HFCT-5953xxxZ/HFCT-5954xxxZ are compliant to the intermediate reach SONET OC12/SDH STM-4 (S4.1) specifications
- Multisourced 2 x 5 and 2 x 10 package styles with LC receptacle
- Single +3.3 V power supply
- Temperature range:
  0°C to +70°C HFCT-595xTLZ/TGZ
  -40°C to +85°C HFCT-595xATLZ/ATGZ
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO9002 certified facility
- Performance
  HFCT-5953xxxZ/HFCT-5954xxxZ:
  Links of 15 km with 9/125 µm SMF
- Fully Class 1 CDRH/IEC 825 compliant
- Pin Outs:
  HFCT-5953xxxZ 2 x 5
  HFCT-5954xxxZ 2 x 10

Applications

- SONET/SDH equipment interconnect, STS-12/SDH STM-4 rate
- Multirate Client Interface on Metro Gateways and Edge Switches

Functional Description
Receiver Section

Design

The receiver section contains an InGaAs/InP photo detector and a preamplifier mounted in an optical subassembly. This optical subassembly is coupled to a postamp/decision circuit.

The postamplifier is ac coupled to the preamplifier as illustrated in Figure 1. The coupling capacitors are large enough to pass the SONET/SDH test pattern at 622 MBd without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion could be degraded.

Figure 1 also shows a filter function which limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity.

These components will reduce the sensitivity of the receiver as the signal bit rate is increased above 622 Mb/s.

The device incorporates a photodetector bias circuit. This output must be connected to V_{CC} and can be monitored by connecting through a series resistor (see application section).

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. However under some conditions of EMI and power supply noise, external power supply filtering may be necessary (see application section).

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. The SD output is low voltage TTL.

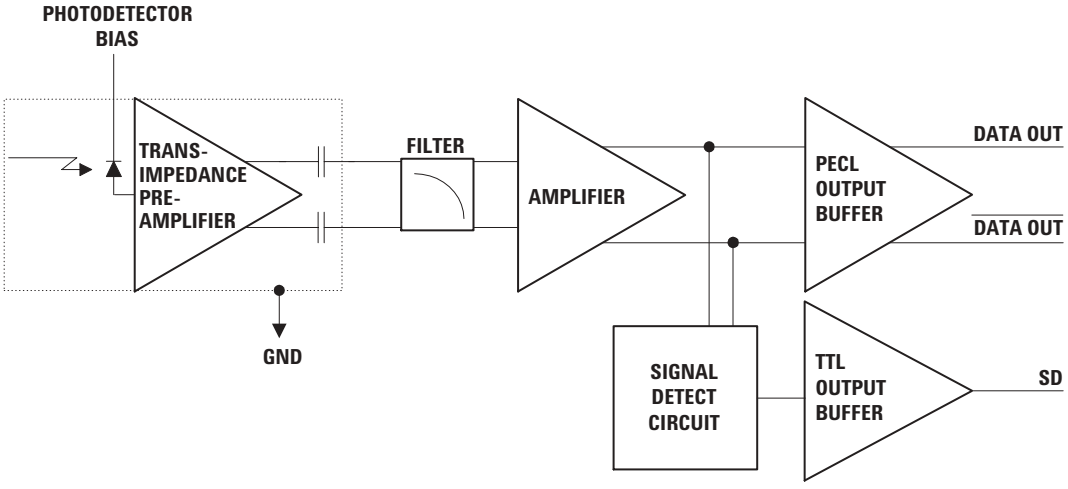


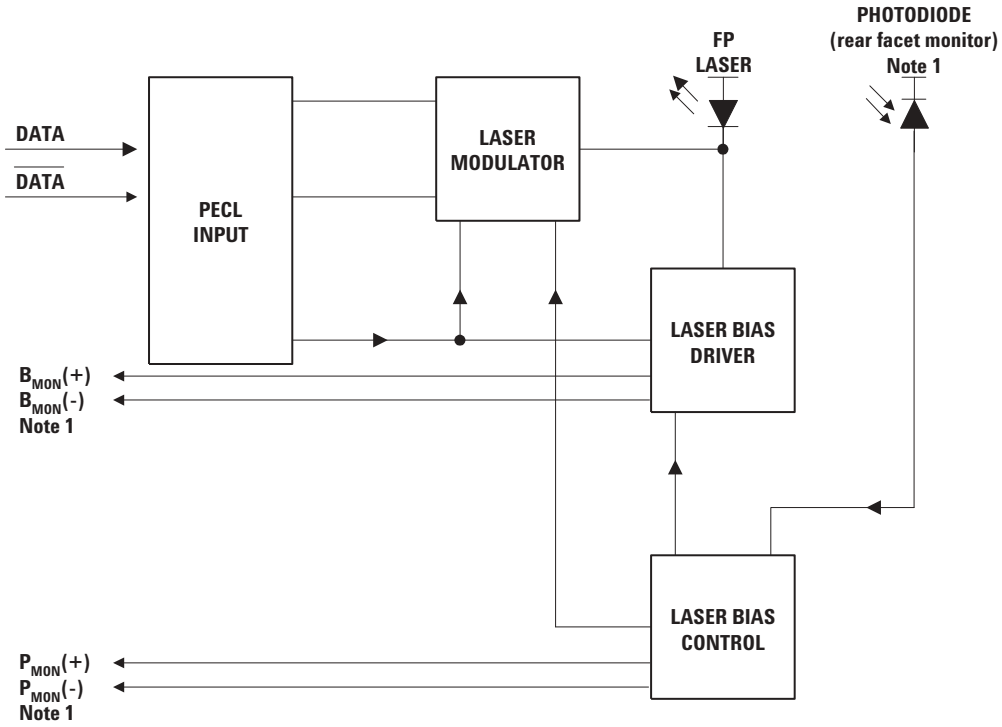
Figure 1 - Receiver Block Diagram

Functional Description
Transmitter Section

Design

The transmitter section uses a Fabry Perot (FP) laser as its optical source, see Figure 2. The package has been designed to be compliant with IEC 825 eye safety requirements under any single fault condition. The optical output is controlled by a custom IC that detects the laser output via the monitor photodiode. This IC provides both dc and ac current drive to the laser to ensure correct modulation, eye diagram and extinction ratio over temperature, supply voltage and operating life.

The transmitter section also includes monitor circuitry for both the laser diode bias current and laser diode optical power.



Note 1: THESE FUNCTIONS ONLY AVAILABLE ON 2 x 10 PINOUT DESIGN

Figure 2 - Simplified Transmitter Schematic

Package

The overall package concept for the Avago transceiver consists of four basic elements; two optical subassemblies and two electrical subassemblies. They are housed as illustrated in the block diagram in Figure 3.

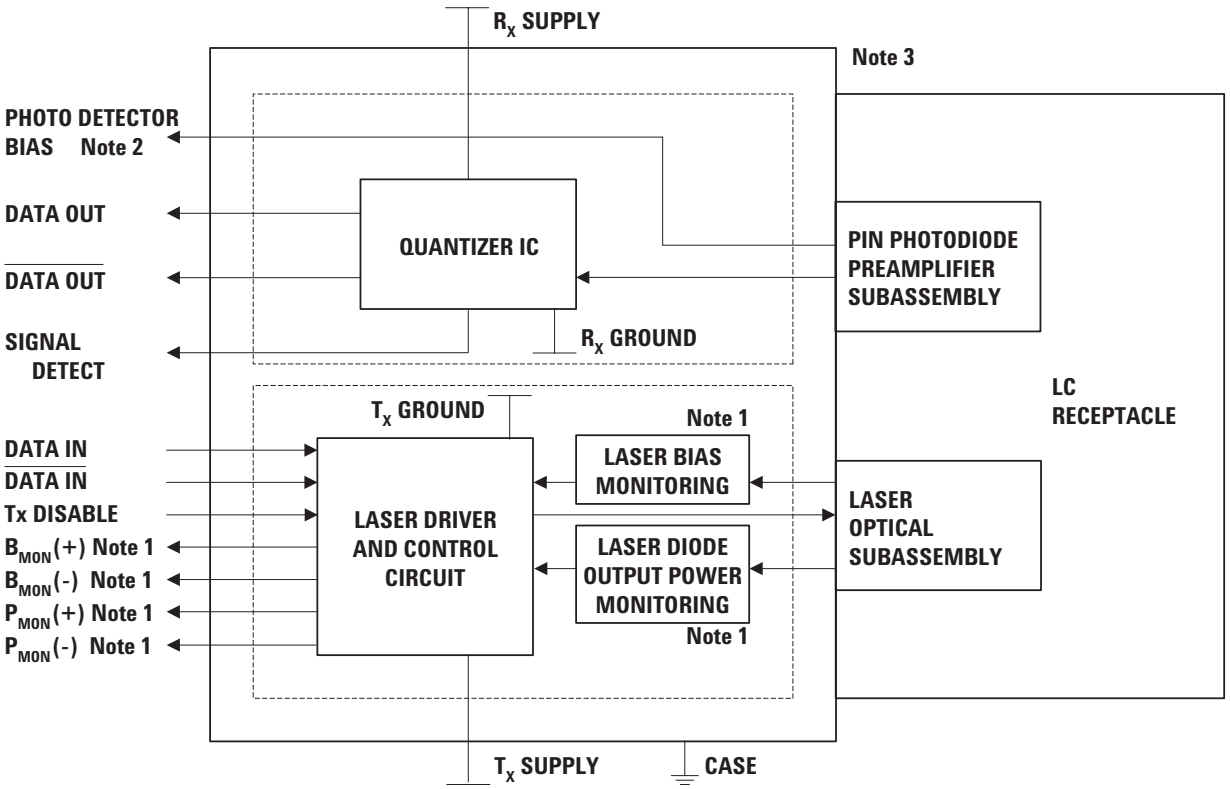
The package outline drawing and pin out are shown in Figures 4, 5 and 6. The details of this package outline and pin out are compliant with the multisource definition of the 2 x 5 and 2 x 10 DIP.

The electrical subassemblies consist of high volume multilayer printed circuit boards on which the IC and various surface-mounted passive circuit elements are attached.

The receiver electrical subassembly includes an internal shield for the electrical and optical subassemblies to ensure high immunity to external EMI fields.

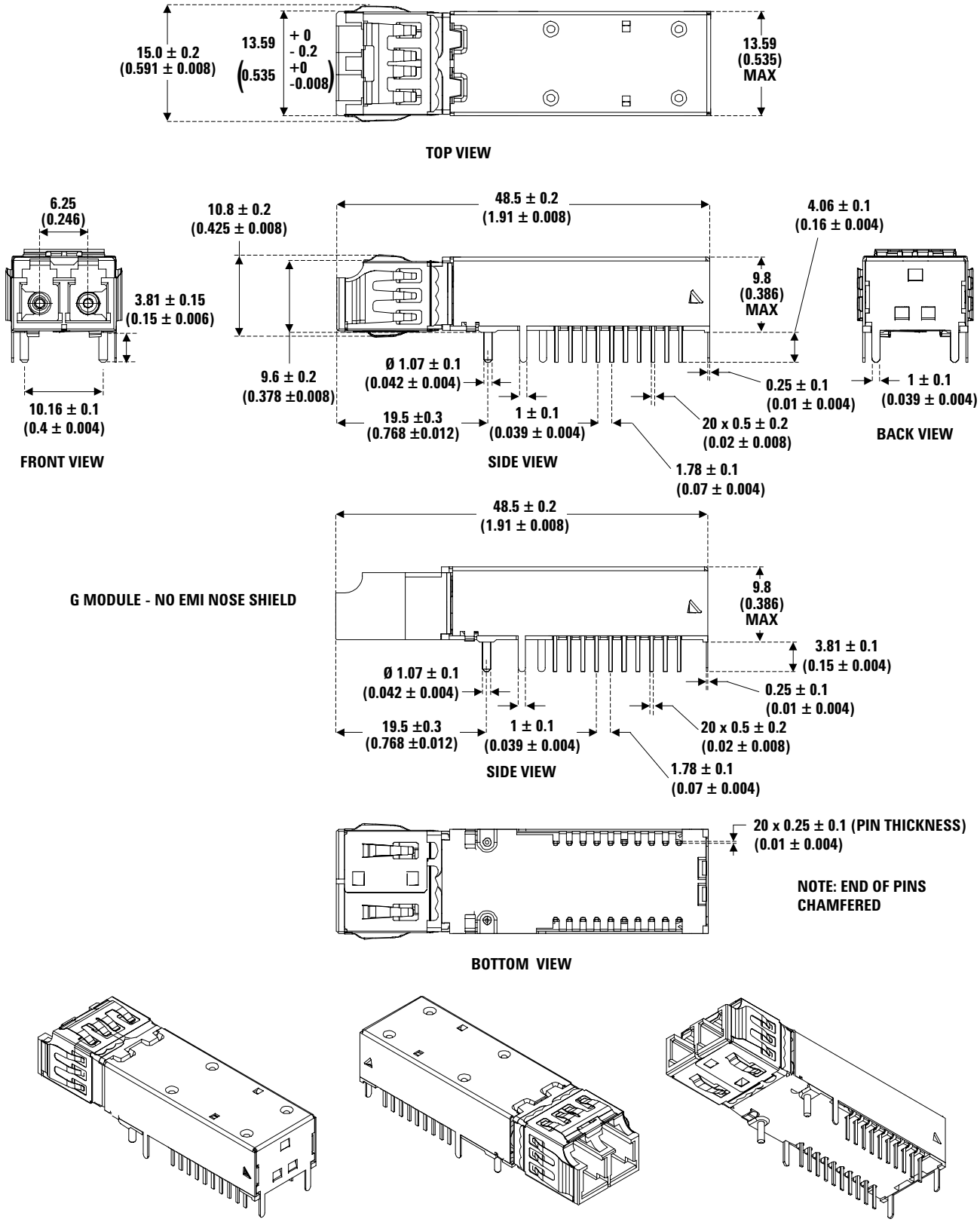
The optical subassemblies are each attached to their respective transmit or receive electrical subassemblies. These two units are than fitted within the outer housing of the transceiver that is molded of filled nonconductive plastic to provide mechanical strength. The housing is then encased with a metal EMI protective shield. Four ground connections are provided for connecting the EMI shield to signal ground.

The PCB's for the two electrical subassemblies both carry the signal pins that exit from the bottom of the transceiver. The solder posts are fastened into the molding of the device and are designed to provide the mechanical strength required to withstand the loads imposed on the transceiver by mating with the LC connectored fiber cables. Although they are not connected electrically to the transceiver, it is recommended to connect them to chassis ground.



Note 1: THESE FUNCTIONS ONLY AVAILABLE ON 2 x 10 PINOUT DESIGN
Note 2: CONNECTED TO $R_X V_{CC}$ IN 2 x 5 DESIGN
Note 3: NOSE CLIP PROVIDES CONNECTION TO CHASSIS GROUND FOR BOTH EMI AND THERMAL DISSIPATION.

Figure 3 - Block Diagram.



DIMENSIONS IN MILLIMETERS (INCHES)

DIMENSIONS SHOWN ARE NOMINAL. ALL DIMENSIONS MEET THE MAXIMUM PACKAGE OUTLINE DRAWING IN THE SFF MSA.

Figure 4 - HFCT-5953xxxZ/HFCT-5954xxxZ Package Outline Drawing (2 x 10 Design shown)

Connection Diagram (HFCT-5954xxxZ)

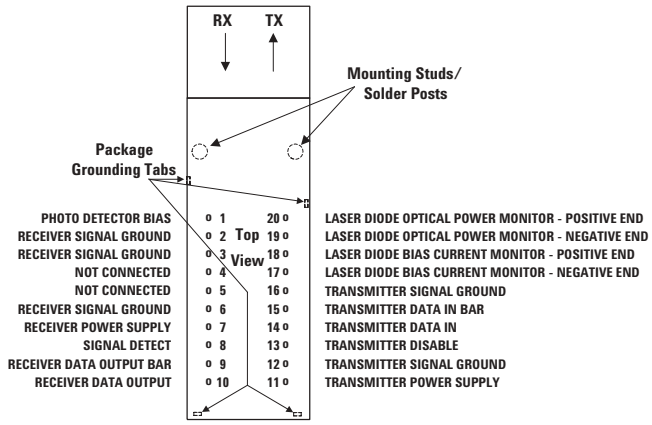


Figure 5 - Pin Out Diagram (Top View)

Pin Descriptions:

Pin 1 Photo Detector Bias, VpdR:
Pin 1 must be connected to VCC for the receiver to work. This pin enables monitoring of photo detector bias current. It must be connected directly to V_{CC}RX, or to V_{CC}RX through a resistor (Max 200 R) for monitoring photo detector bias current.

Pins 2, 3, 6 Receiver Signal Ground V_{EE} RX:
Directly connect these pins to the receiver ground plane.

Pins 4, 5 DO NOT CONNECT

Pin 7 Receiver Power Supply V_{CC} RX:
Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin. Note: the filter circuit should not cause V_{CC} to drop below minimum specification.

Pin 8 Signal Detect SD:
Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a logic "0" output.

This Signal Detect output can be used to drive a low voltage TTL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 9 Receiver Data Out Bar RD-:
Nointernalterminationsareprovided.Seerecommended circuit schematic.

Pin 10 Receiver Data Out RD+:
Nointernalterminationsareprovided.Seerecommended circuit schematic.

Pin 11 Transmitter Power Supply V_{CC} TX:
Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pins 12, 16 Transmitter Signal Ground V_{EE} TX:
Directly connect these pins to the transmitter signal ground plane.

Pin 13 Transmitter Disable T_{DIS}:
Optional feature, connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 14 Transmitter Data In TD+:
Nointernalterminationsareprovided.Seerecommended circuit schematic.

Pin 15 Transmitter Data In Bar TD-:
Nointernalterminationsareprovided.Seerecommended circuit schematic.

Pin 17 Laser Diode Bias Current Monitor - Negative End B_{MON-}
The laser diode bias current is accessible by measuring the voltage developed across pins 17 and 18. Dividing the voltage by 10 Ohms (internal) will yield the value of the laser bias current.

Pin 18 Laser Diode Bias Current Monitor - Positive End B_{MON}+
See pin 17 description.

Pin 19 Laser Diode Optical Power Monitor - Negative End P_{MON}–
The back facet diode monitor current is accessible by measuring the voltage developed across pins 19 and 20. The voltage across a 200 Ohm internal resistor between pins 19 and 20 will be proportional to the photo current.

Pin 20 Laser Diode Optical Power Monitor - Positive End P_{MON}+
See pin 19 description.

Mounting Studs/Solder Posts
The two mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Package Grounding Tabs
Connect four package grounding tabs to signal ground.

Connection Diagram (HFCT-5953xxxZ)

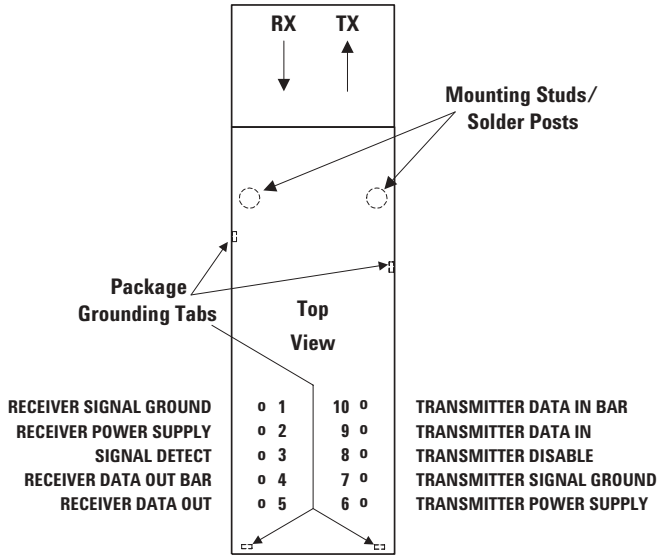


Figure 6 - Pin Out Diagram (Top View)

Pin Descriptions:

Pin 1 Receiver Signal Ground V_{EE} RX:
Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply V_{CC} RX:
Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin. Note: the filter circuit should not cause V_{CC} to drop below minimum specification.

Pin 3 Signal Detect SD:
Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a logic "0" output.

This Signal Detect output can be used to drive a low voltage TTL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 4 Receiver Data Out Bar RD-:
No internal terminations are provided. See recommended circuit schematic.

Pin 5 Receiver Data Out RD+:
No internal terminations are provided. See recommended circuit schematic.

Pin 6 Transmitter Power Supply V_{CC} TX:
Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground V_{EE} TX:
Directly connect this pin to the transmitter signal ground plane.

Pin 8 Transmitter Disable T_{DIS}:
Optional feature, connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 9 Transmitter Data In TD+:
No internal terminations are provided. See recommended circuit schematic.

Pin 10 Transmitter Data In Bar TD-:
No internal terminations are provided. See recommended circuit schematic.

Mounting Studs/Solder Posts
The two mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Package Grounding Tabs
Connect four package grounding tabs to signal ground.

Application Information

The Applications Engineering Group at Avago is available to assist you with technical understanding and design trade-offs associated with these transceivers. You can contact them through your Avago sales representative.

The following information is provided to answer some of the most common questions about the use of the parts.

Optical Power Budget and Link Penalties

The worst-case Optical Power Budget (OPB) in dB for a fiber-optic link is determined by the difference between the minimum transmitter output optical power (dBm avg) and the lowest receiver sensitivity (dBm avg). This OPB provides the necessary optical signal range to establish a working fiber-optic link. The OPB is allocated for the fiber-optic cable length and the corresponding link penalties. For proper link performance, all penalties that affect the link performance must be accounted for within the link optical power budget.

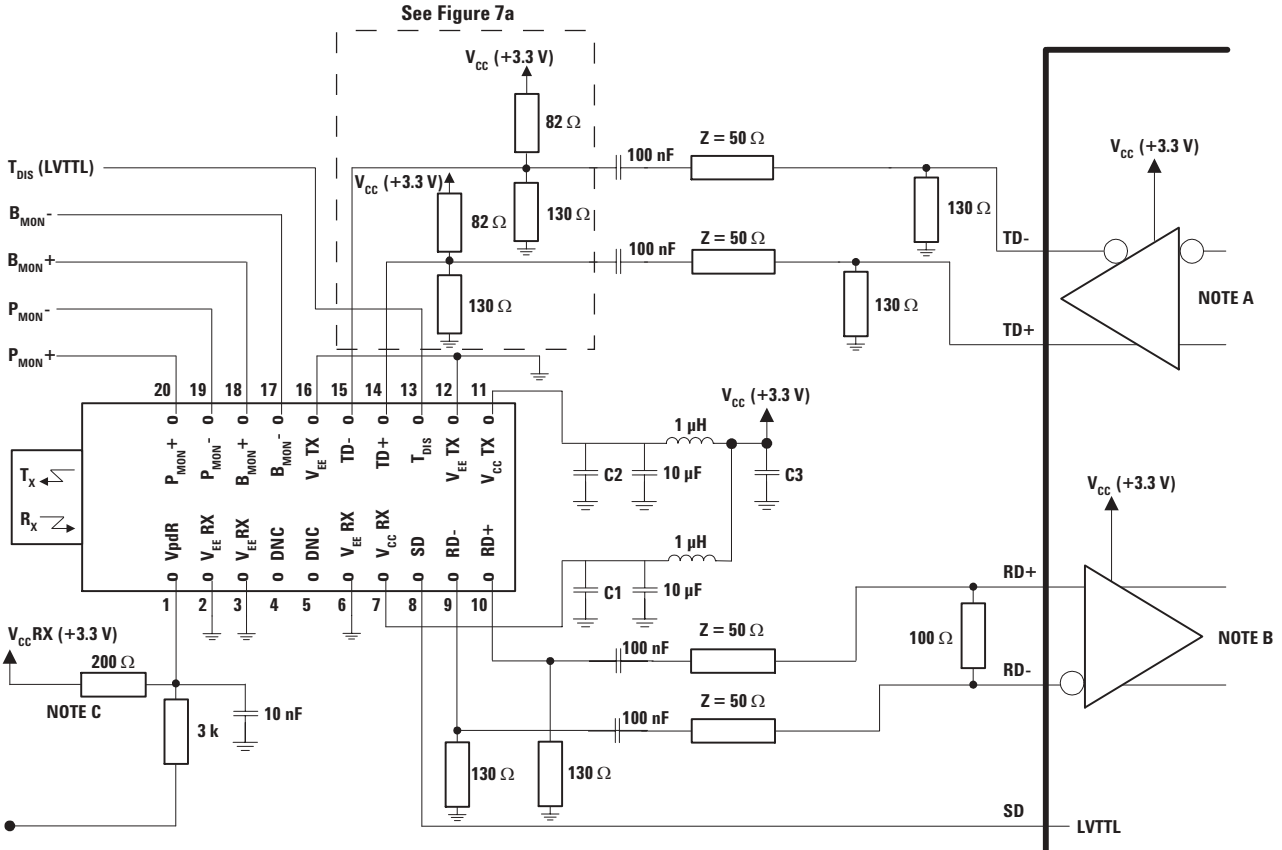
Recommended Circuit

Figures 7 and 8 shows the recommended interface for deploying the Avago transceivers in a +3.3 V system.

Data Line Interconnections

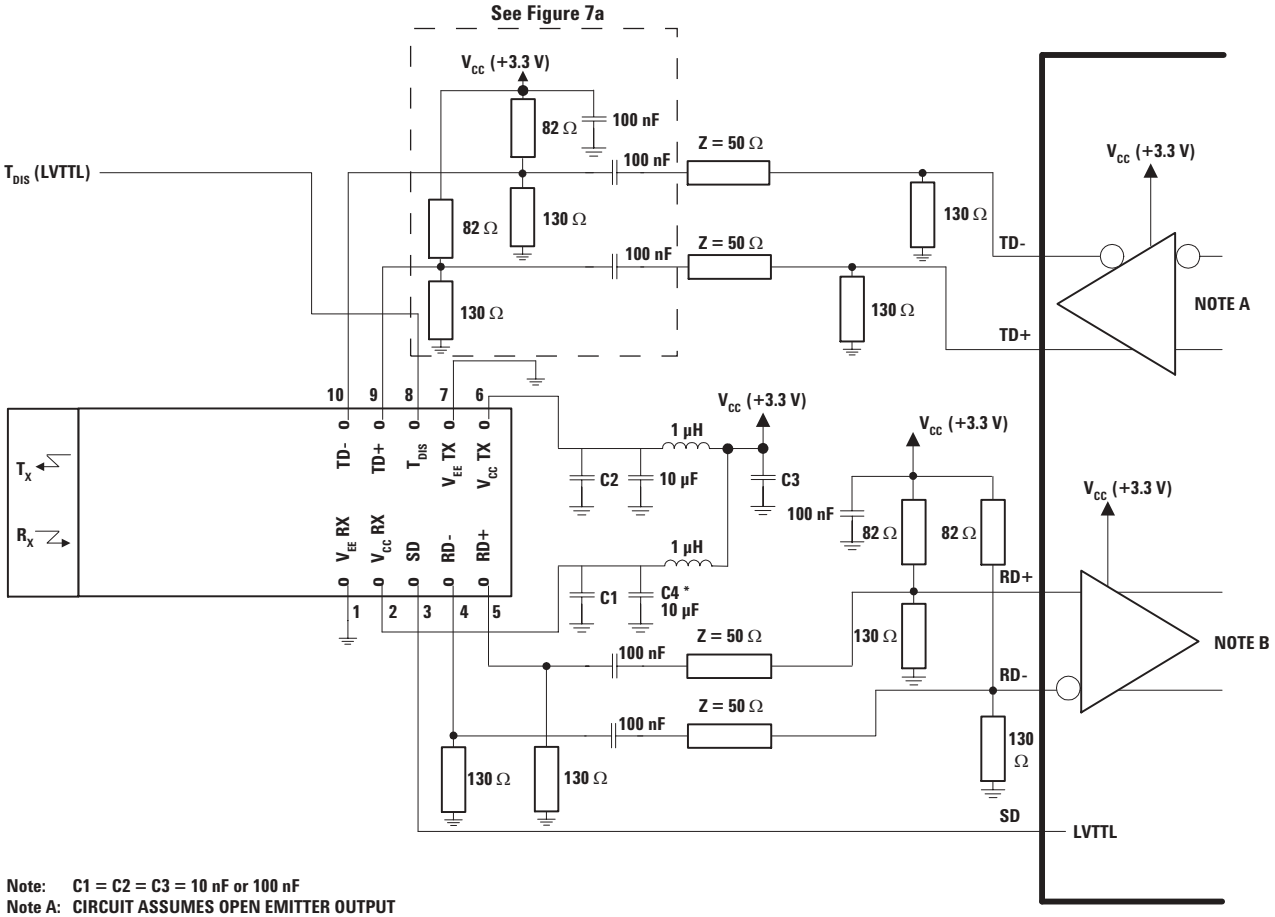
Avago's HFCT-5953xxxZ/HFCT-5954xxxZ fiber-optic transceivers are designed to couple to +3.3 V PECL signals. The transmitter driver circuit regulates the output optical power. The regulated light output will maintain a constant output optical power provided the data pattern is reasonably balanced in duty cycle. If the data duty cycle has long, continuous state times (low or high data duty cycle), then the output optical power will gradually change its average output optical power level to its preset value.

Electrical and Mechanical Interface



Note: C1 = C2 = C3 = 10 nF or 100 nF
Note A: CIRCUIT ASSUMES OPEN EMITTER OUTPUT
Note B: CIRCUIT ASSUMES HIGH IMPENDANCE INTERNAL BIAS @ V_{CC} - 1.3 V.
Note C: THE BIAS RESISTOR FOR VpdR SHOULD NOT EXCEED 200 OHM.

Figure 7 - Recommended Interface Circuit (HFCT-5954xxxZ)



Note: C1 = C2 = C3 = 10 nF or 100 nF
Note A: CIRCUIT ASSUMES OPEN EMITTER OUTPUT
Note B: WHEN INTERNAL BIAS IS PROVIDED REPLACE SPLIT RESISTORS WITH 100Ω TERMINATION
* C4 IS AN OPTIONAL BYPASS CAPACITOR FOR ADDITIONAL LOW FREQUENCY NOISE FILTERING.

Figure 8 - Recommended Interface Circuit (HFCT-5953xxxZ)

The HFCT-5953xxxZ/HFCT-5954xxxZ have a transmit disable function which is a single-ended +3.3 V TTL input which is dc-coupled to pin 13 on the HFCT-5954xxxZ and pin 8 on HFCT- 5953xxxZ. In addition the HFCT-5954xxxZ offers the designer the option of monitoring the laser diode bias current and the laser diode optical power. The voltage measured between pins 17 and 18 is proportional to the bias current through an internal 10 Ω resistor. Similarly the optical power rear facet monitor circuit provides a photo current which is proportional to the voltage measured between pins 19 and 20 on the 2 x 10 version, this voltage is measured across an internal 200 Ω resistor.

As for the receiver section, it is internally ac-coupled between the preamplifier and the postamplifier stages. The actual Data and Data-bar outputs of the postamplifier are dc-coupled to their respective output pins (pins 9 and 10 on the HFCT-5953xxxZ and pins 14 and 15 on the HFCT-5954xxxZ). The two data outputs of the receiver should be terminated with identical load circuits to avoid unnecessarily large ac currents in V_{CC}. If the outputs are loaded identically the ac current is largely nulled.

Signal Detect is a single-ended, +3.3 V TTL compatible output signal that is dc-coupled to pin 3 on the HFCT-5953xxxZ and pin 8 on the HFCT-5954xxxZ modules. Signal Detect should not be ac-coupled externally to the follow-on circuits because of its infrequent state changes.

The HFCT-5954xxxZ offers the designer the option of monitoring the PIN photo detector bias current. Figures 7 and 8 show a resistor network, which could be used to do this. Note that the photo detector bias current pin must be connected to V_{CC}. Avago also recommends that a decoupling capacitor is used on this pin.

Power Supply Filtering and Ground Planes

It is important to exercise care in circuit board layout to achieve optimum performance from these transceivers. Figures 7 and 8 show the power supply circuit which complies with the small form factor multisource agreement. It is further recommended that a continuous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Package footprint and front panel considerations

The Avago transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the current multisource agreement which defined the 2 x 5 and 2 x 10 package styles. This drawing is reproduced in Figure 9 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board. Figure 10 shows the front panel dimensions associated with such a layout.

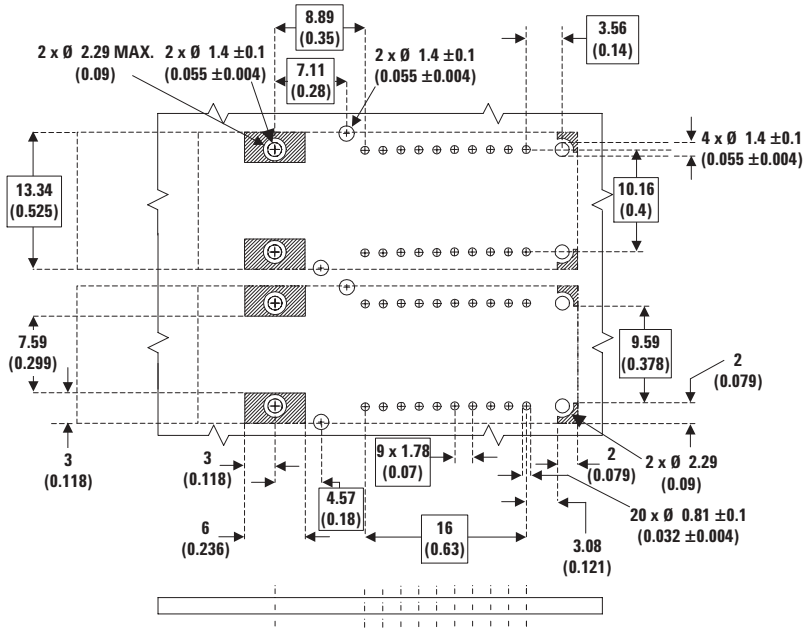
Eye Safety Circuit

For an optical transmitter device to be eye-safe in the event of a single fault failure, the transmitter must either maintain eye-safe operation or be disabled.

The HFCT-5953xxxZ/HFCT-5954xxxZ is intrinsically eye safe and does not require shut down circuitry.

Signal Detect

The Signal Detect circuit provides a deasserted output signal when the optical link is broken (or when the remote transmitter is OFF). The Signal Detect threshold is set to transition from a high to low state between the minimum receiver input optional power and -45 dBm avg. input optical power indicating a definite optical fault (e.g. unplugged connector for the receiver or transmitter, broken fiber, or failed far-end transmitter or data source). The Signal Detect does not detect receiver data error or error-rate. Data errors can be determined by signal processing offered by upstream PHY ICs.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:

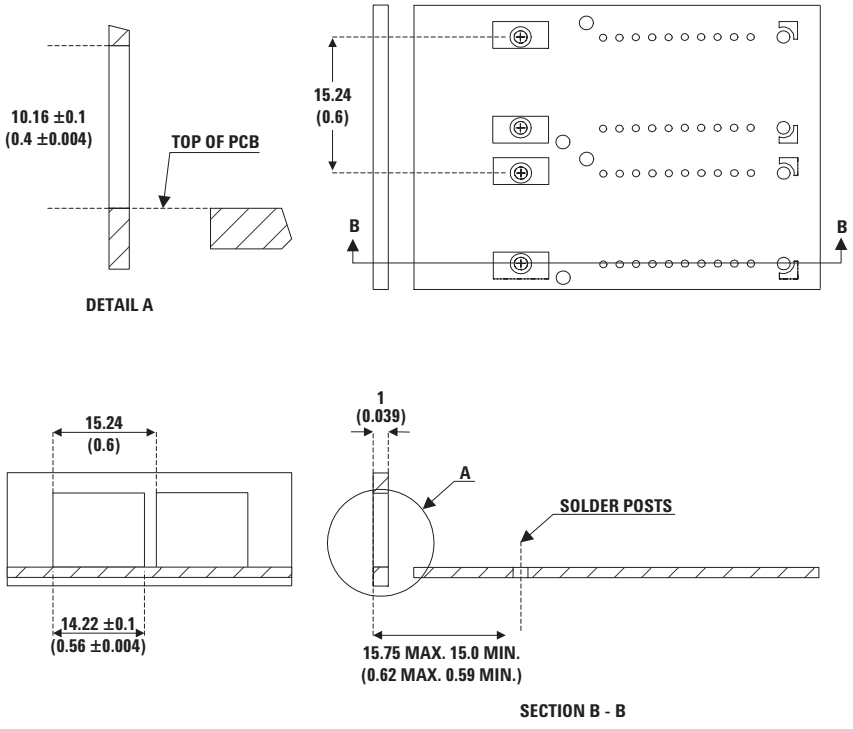
1. THIS FIGURE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT FOR THE SFF TRANSCEIVER.
2. THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.
3. 2 x 10 TRANSCEIVER MODULE REQUIRES 26 PCB HOLES (20 I/O PINS, 2 SOLDER POSTS AND 4 PACKAGE GROUNDING TABS). PACKAGE GROUNDING TABS SHOULD BE CONNECTED TO SIGNAL GROUND.
4. 2 x 5 TRANSCEIVER MODULE REQUIRES 16 PCB HOLES (10 I/O PINS, 2 SOLDER POSTS AND 4 PACKAGE GROUNDING TABS). PACKAGE GROUNDING TABS SHOULD BE CONNECTED TO SIGNAL GROUND.
5. THE MOUNTING STUDS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY AND TO ENSURE FOOTPRINT COMPATIBILITY WITH OTHER SFF TRANSCEIVERS.
6. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

Figure 9 - Recommended Board Layout Hole Pattern

Electromagnetic Interference (EMI)

One of a circuit board designer's foremost concerns is the control of electromagnetic emissions from electronic equipment. Success in controlling generated Electromagnetic Interference (EMI) enables the designer to pass a governmental agency's EMI regulatory standard and more importantly, it reduces the possibility of interference to neighboring equipment. Avago has designed the HFCT-5953xxxZ/HFCT-5954xxx to provide excellent EMI performance. The EMI performance of a chassis is dependent on physical design and features which help improve EMI suppression. Avago encourages using standard RF suppression practices and avoiding poorly EMI-sealed enclosures.

Avago's HFCT-5953ATLZ/TLZ/ HFCT-5954ATLZ/ TLZ OC-12/STM-4 LC transceivers have nose shields which provide a convenient chassis connection to the nose of the transceiver. This nose shield improves system EMI performance by closing off the LC aperture. Localized shielding is also improved by tying the four metal housing package grounding tabs to signal ground on the PCB. Though not obvious by inspection, the nose shield and metal housing are electrically separated for customers who do not wish to directly tie chassis and signal grounds together. Figure 10 shows the recommended positioning of the transceivers with respect to the PCB and faceplate.



DIMENSIONS IN MILLIMETERS (INCHES)

1. FIGURE DESCRIBES THE RECOMMENDED FRONT PANEL OPENING FOR A LC OR SG SFF TRANSCEIVER.
2. SFF TRANSCEIVER PLACED AT 15.24 mm (0.6) MIN. SPACING.

Figure 10 - Recommended Panel Mounting

Package and Handling Instructions

Flammability

The HFCT-5953xxxZ/HFCT-5954xxxZ transceivers housing consist of high strength, heat resistant and UL 94 V-0 flame retardant plastic and metal packaging.

Recommended Solder and Wash Process

The HFCT-5953xxxZ/HFCT-5954xxxZ are compatible with industry-standard wave processes.

Process plug

The transceivers are supplied with a process plug for protection of the optical port within the LC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping and storage. It is made of a high-temperature, molded sealing material.

Recommended Solder fluxes

Solder fluxes used with the HFCT-5953xxxZ/ HFCT-5954xxxZ should be water-soluble, organic fluxes. Recommended solder fluxes include Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-Metals of Jersey City, NJ.

Recommended Cleaning/ Degreasing Chemicals

Alcohols: methyl, isopropyl, isobutyl.
Aliphatics: hexane, heptane
Other: naphtha.

Do not use partially halogenated hydrocarbons such as 1,1.1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, Avago does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

LC SFF Cleaning Recommendations

In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop stick type (diam. 1.25 mm) and HFE7100 cleaning fluid.

Table 1: Regulatory Compliance - Targeted Specification

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883 Method 3015	Class 2 (>2 kV).
Electrostatic Discharge (ESD) to the LC Receptacle	Variation of IEC 61000-4-2	Tested to 8 kV contact discharge.
Electromagnetic Interference (EMI)	FCC Class B	Margins are dependent on customer board and chassis designs.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 27 to 1000 MHz applied to the transceiver without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	FDA CDRH 21-CFR 1040 Class 1	Accession Number: ⇒ 9521220
	IEC 60825-1 Amendment 2 2001-01	License Number: ⇒ 933/510216
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment.	UL File. E173874

Regulatory Compliance
The Regulatory Compliance for transceiver performance is shown in Table 1. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)
There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the LC connector receptacle is exposed to the outside of the equipment chassis it may be subject to whatever system-level ESD test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)
Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet FCC regulations in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. Refer to EMI section (page 9) for more details.

Immunity
Transceivers will be subject to radio-frequency electromagnetic fields following the IEC 61000-4-3 test method.

Eye Safety
These laser-based transceivers are classified as AEL Class I (U.S. 21 CFR(J) and AEL Class 1 per EN 60825-1 (+A11). They are eye safe when used within the data sheet limits per CDRH. They are also eye safe under normal operating conditions and under all reasonably foreseeable single fault conditions per EN60825-1. Avago has tested the transceiver design for compliance with the requirements listed below under normal operating conditions and under single fault conditions where applicable. TUV Rheinland has granted certification to these transceivers for laser eye safety and use in EN 60950 and EN 60825-2 applications. Their performance enables the transceivers to be used without concern for eye safety up to 3.6 V transmitter V_{CC}.

CAUTION:
There are no user serviceable parts nor any maintenance required for the HFCT-5953xxxZ/HFCT-5954xxxZ. All adjustments are made at the factory before shipment to our customers. Tampering with or modifying the performance of the HFCT-5953xxxZ/HFCT-5954xxxZ will result in voided product warranty. It may also result in improper operation of the HFCT-5953xxxZ/HFCT-5954xxxZ circuitry, and possible overstress of the laser source. Device degradation or product failure may result.

Connection of the HFCT-5953xxxZ/HFCT-5954xxxZ to a non-approved optical source, operating above the recommended absolute maximum conditions or operating the HFCT-5953xxxZ/HFCT-5954xxxZ in a manner inconsistent with their design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to recertify and reidentify the laser product under the provisions of U.S. 21 CFR (Subchapter J).

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		+85	°C	
Supply Voltage	V_{CC}	-0.5		3.6	V	1
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Data Output Current	I_D			50	mA	
Relative Humidity	RH			85	%	

Recommended Multirate Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature						
HFCT-5953TLZ/TGZ/HFCT-5954TLZ/TGZ	T_A	0		+70	°C	2
HFCT-5953ATLZ/ATGZ/HFCT-5954ATLZ/ATGZ	T_A	-40		+85	°C	2
Supply Voltage	V_{CC}	3.14		3.47	V	
Power Supply Rejection	PSR		100		mV_{Pk-Pk}	3
Transmitter Differential Input Voltage	V_D	0.3		1.6	V	
Data Output Load	R_{DL}		50		Ω	
TTL Signal Detect Output Current - Low	I_{OL}			1.0	mA	
TTL Signal Detect Output Current - High	I_{OH}	-400			µA	
Transmit Disable Input Voltage - Low	T_{DIS}			0.6	V	
Transmit Disable Input Voltage - High	T_{DIS}	2.2			V	
Transmit Disable Assert Time	T_{ASSERT}			10	µs	4
Transmit Disable Deassert Time	$T_{DEASSERT}$			1.0	ms	5

Process Compatibility

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Wave Soldering and Aqueous Wash	T_{SOLD}/t_{SOLD}			+260/10	°C/sec.	6

Notes:

1. The transceiver is class 1 eye safe up to V_{CC} = 3.6 V.
2. Ambient operating temperature utilizes air flow of 2 ms^{-1} over the device.
3. Tested with a sinusoidal signal in the frequency range from 10 Hz to 1 MHz on the V_{CC} supply with the recommended power supply filter in place. Typically less than a 1 dB change in sensitivity is experienced.
4. Time delay from Transmit Disable Assertion to laser shutdown.
5. Time delay from Transmit Disable Deassertion to laser startup.
6. Aqueous wash pressure <110 psi.

Transmitter Electrical Characteristics for multirate operations at OC3 (155 Mbit/s) and OC12 (622 Mbit/s)
HFCT-5953TLZ/TGZ/HFCT-5954TLZ/TGZ: T_A = 0°C to +70°C, V_{CC} = 3.14 V to 3.47 V
HFCT-5953ATLZ/ATGZ/HFCT-5954ATLZ/ATGZ: T_A = -40°C to +85°C, V_{CC} = 3.14 V to 3.47 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCT}		30	120	mA	1
Power Dissipation	P_{DIST}		0.10	0.42	W	
Data Input Voltage Swing (single-ended)	V_{IH} - V_{IL}	250	800	930	mV	
Transmitter Differential Data Input Current - Low	I_{IL}	-350			µA	
Transmitter Differential Data Input Current - High	I_{IH}			350	µA	
Laser Diode Bias Monitor Voltage				700	mV	2, 3
Power Monitor Voltage		10		200	mV	2, 3

Receiver Electrical Characteristics for multirate operations at OC3 (155 Mbit/s) and OC12 (622 Mbit/s)
HFCT-5953TLZ/TGZ/HFCT-5954TLZ/TGZ: T_A = 0°C to +70°C, V_{CC} = 3.14 V to 3.47 V
HFCT-5953ATLZ/ATGZ/HFCT-5954ATLZ/ATGZ: T_A = -40°C to +85°C, V_{CC} = 3.14 V to 3.47 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CCR}		70	110	mA	1
Power Dissipation	P_{DISR}		0.23	0.38	W	4
Data Output Voltage Swing (single-ended)	V_{OH} - V_{OL}	575	800	930	mV	5
Data Output Rise Time	t_r			0.5	ns	6
Data Output Fall Time	t_f			0.5	ns	6
Signal Detect Output Voltage - Low	V_{OL}			0.8	V	7
Signal Detect Output Voltage - High	V_{OH}	2.0			V	7
Signal Detect Assert Time (OFF to ON)	AS_{MAX}			100	µs	
Signal Detect Deassert Time (ON to OFF)	ANS_{MAX}	2.3		100	µs	

Notes:
1. Excludes data output termination currents.
2. The laser bias monitor current and laser diode optical power are calculated as ratios of the corresponding voltages to their current sensing resistors, 10 Ω and 200 Ω (see Figure 7). On the 2 x 10 version only.
3. On the 2 x 10 version only.
4. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and currents.
5. These outputs are compatible with 10 k, 10 kH, and 100 k ECL and PECL inputs.
6. These are 20-80% values.
7. SD is LVTTL compatible.

Transmitter Optical Characteristics for multirate operations at OC3 (155 Mbit/s) and OC12 (622 Mbit/s)
HFCT-5953TLZ/TGZ/HFCT-5954TLZ/TGZ: T_A = 0°C to +70°C, V_{CC} = 3.14 V to 3.47 V
HFCT-5953ATLZ/ATGZ/HFCT-5954ATLZ/ATGZ: T_A = -40°C to +85°C, V_{CC} = 3.14 V to 3.47 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 9 µm SMF	P_{OUT}	-15		-8	dBm	1
Center Wavelength	I_C	1274		1356	nm	
Spectral Width - rms	s			2.5	nm rms	2
Optical Rise Time	t_r		250	1000	ps	3
Optical Fall Time	t_f		250	1000	ps	3
Extinction Ratio	E_R	8.2			dB	
Output Optical Eye	Compliant with eye mask Bellcore GR-CORE-000253 and ITU-T G.957					
Back Reflection Sensitivity				-8.5	dB	4
Jitter Generation	pk to pk		25	70	mUI	5
	RMS		2	7	mUI	5

Receiver Optical Characteristics for multirate operations at OC3 (155 Mbit/s) and OC12 (622 Mbit/s)
HFCT-5953TLZ/TGZ/HFCT-5954TLZ/TGZ: T_A = 0°C to +70°C, V_{CC} = 3.14 V to 3.47 V
HFCT-5953ATLZ/ATGZ/HFCT-5954ATLZ/ATGZ: T_A = -40°C to +85°C, V_{CC} = 3.14 V to 3.47 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Receiver Sensitivity	P_{IN} MIN		-32	-28	dBm avg.	6
Receiver Overload	P_{IN} MAX	-8			dBm avg.	6
Input Operating Wavelength	l	1270		1570	nm	
Signal Detect - Asserted	P_A		-34	-28	dBm avg.	
Signal Detect - Deasserted	P_D	-45	-34.3		dBm avg.	
Signal Detect - Hysteresis	P_H	0.5		4	dB	
Optical Return Loss, ORL			-35	-14	dB	

Notes:
1. The output power is coupled into a 1 m single-mode fiber. Minimum output optical level is at end of life.
2. The relationship between FWHM and RMS values for spectral width can be derived from the assumption of a Gaussian shaped spectrum which results in RMS = FWHM/2.35.
3. These are unfiltered 20-80% values. The typical value is for OC12 operation only.
4. This meets the "desired" requirement in SONET specification (GR253). The figure given is the allowable mismatch for 1 dB degradation in receiver sensitivity.
5. For the jitter measurements, the device was driven with SONET OC-12C data pattern filled with a 2^{23}-1 PRBS payload.
6. Minimum sensitivity and saturation levels for a 2^{23}-1 PRBS with 72 ones and 72 zeros inserted. Over the range the receiver is guaranteed to provide output data with a Bit Error Rate better than or equal to 1×10^{-10}.

Design Support Materials

Avago has created a number of reference designs with major PHY IC vendors in order to demonstrate full functionality and interoperability. Such design information and results can be made available to the designer as a technical aid. Please contact your Avago representative for further information if required.

Ordering Information

Temperature range 0°C to +70°C

HFCT-5953TLZ	2 x 5 footprint	with EMI nose shield
HFCT-5954TLZ	2 x 10 footprint	with EMI nose shield
HFCT-5953TGZ	2 x 5 footprint	without EMI nose shield
HFCT-5954TGZ	2 x 10 footprint	without EMI nose shield

Temperature range -40°C to +85°C

HFCT-5953ATLZ	2 x 5 footprint	with EMI nose shield
HFCT-5954ATLZ	2 x 10 footprint	with EMI nose shield
HFCT-5953ATGZ	2 x 5 footprint	without EMI nose shield
HFCT-5954ATGZ	2 x 10 footprint	without EMI nose shield

Class 1 Laser Product: This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture

Date of Manufacture:_____

Avago Technologies Inc., No 1 Yishun Ave 7, Singapore

Handling Precautions

1. The HFCT-5953xxxZ/HFCT-5954xxxZ can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.
2. Normal handling precautions for electrostatic sensitive devices should be taken.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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