SPECIFICATIONS FOR LCD MODULE

MODEL NO.
BF128128E series
VER.01

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

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History of Version

Version	Contents	Date	Note
01	NEW VERSION	2006/12/14	SPEC.

C O N T E N T S

1. Numbering System

	B	F	128128	E	-	-	-	-	-	xxx
	0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	G=STN/gray Y=STN/yellow-green PLED/yellow-green C=color STN,OLED/RGB	B=STN/blue,OLED/blue F=FSTN T=TN D=OLED/blue+yellow A=OLED/blue+yellow+green
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB array I=RGB edge Q=LED edge/red N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on datasheet	t=temperature compensation for LCD p=touch panel $=RoHS

2. General Specification

(1) Mechanical Dimension

Item	Dimension	Unit
Number of Dots	128 x 128	dots
Module dimension (L x W x H)	83.5 x 36.3 x 1.4 (MAX) 83.5 x 36.3 x 4.0 (LED B/L)	mm
View area	30.5 x 32.0	mm
Active area	27.25 x 29.81	mm
Dot size	0.199 x 0.219	mm
Dot pitch	0.213 x 0.233	mm

(2) Controller IC: HD66750 controller

(3) Temperature Range

	Normal	Wide
Operating	0 ~+50℃	-20 ~+70℃
Storage	-10 ~+60℃	-30 ~+80℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	0	-	+50	℃
Storage Temperature	T_{ST}	-20	-	+70	℃
Input Voltage	V_I	Vss	-	Vdd	V
Supply Voltage For Logic	Vdd-Vss	-0.3	-	+3.6	V
Supply Voltage For LCD	Vo-Vss	+5.0	+10.5	+15.5	V

4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	—	2.8	—	3.6	V
Supply Voltage For LCD	Vdd-Vo	＊Ta=-20℃ Ta=25℃ ＊Ta=+70℃	— — —	11.5 **10.5** 9.5	— — —	V
Input High Volt.	V_{IH}	—	2.8	—	Vdd	V
Input Low Volt.	V_{IL}	—	0	—	0.8	V
Output High Volt.	V_{OH}	—	1.0	—	Vdd	V
Output Low Volt.	V_{OL}	—	0	—	0.4	V
Supply Current	Idd	Vdd=2.8V	—	0.2	0.4	mA

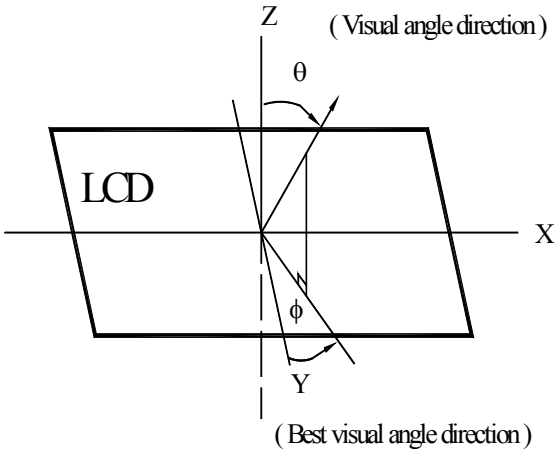
5. Optical Characteristics

a. FSTN

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧3	10	-	60	deg
	(H) φ	CR≧3	-45	-	45	deg
Contrast Ratio	CR	-	-	5	-	-
Response Time 25℃	T rise	-	-	100	150	ms
	T fall	-	-	150	200	ms

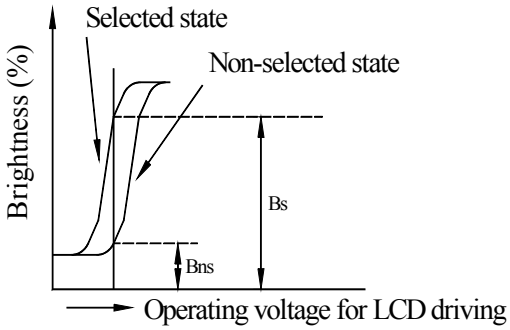
5.1 Definitions

■View Angles

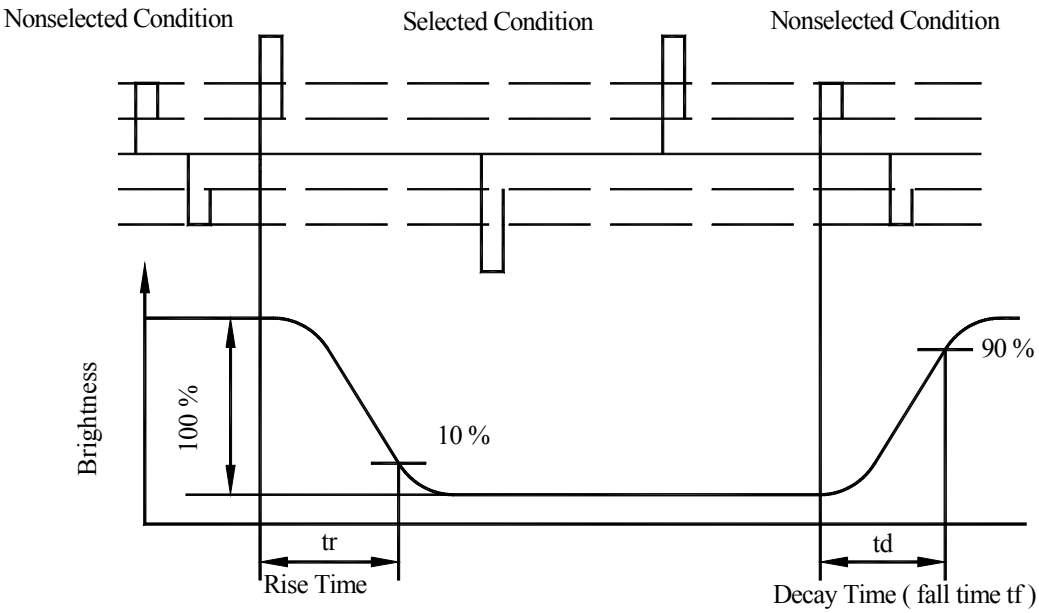


■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



■Response Time

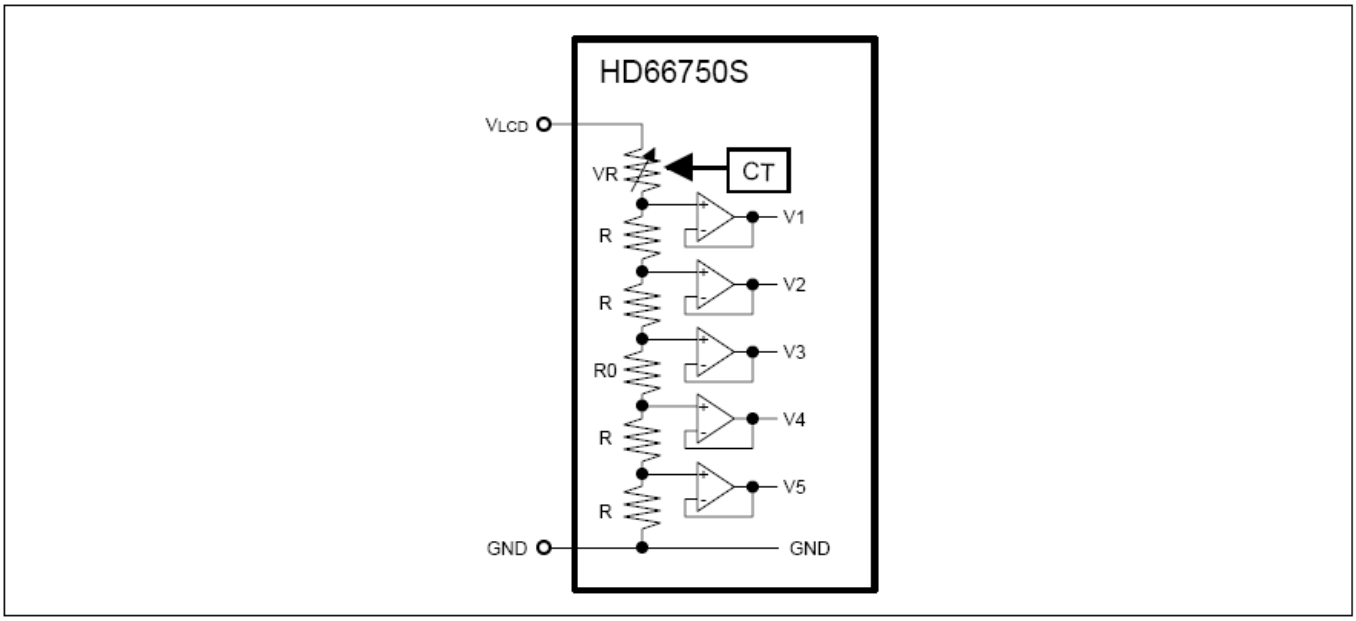


6. Interface Description

Pin No.	Symbol	Level	Description
1	Vdd	-	Power supply (+3.3 V)
2	DB7	H / L	Data bus line
3	DB6	H / L	Data bus line
4	DB5	H / L	Data bus line
5	DB4	H / L	Data bus line
6	DB3	H / L	Data bus line
7	DB2	H / L	Data bus line
8	DB1	H / L	Data bus line
9	DB0	H / L	Data bus line
10	/RESET	H / L	H : Normal ; L : Initialize
11	/CS	L	L : Chip select
12	RS	H / L	Register select(H : control L : index/status)
13	/WR	L	Data write. Write data into HD66750 when WR = L
14	/RD	L	Data read. Read data from HD66750 when RD = L
15	Vss	-	Power supply (GND)

7. Contrast Adjustment

Software can adjust 64-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between VLCD and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between VLCD and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 3.20 x R, where R is a reference resistance obtained by dividing the total resistance.
The HD66750S incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that potential difference between VLCD and V1 is 0.1 V or higher and that between V4 and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.



Contrast Control (R04h)
CT5–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 64-step contrast. For details, see the Contrast Adjuster section.

Index Instruction

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	*	*	*	*	*	*	*	*	Index high 8bit
0	0	*	*	*	ID4	ID3	ID2	ID1	ID0	Index low 8bit
0	0	0	0	0	0	0	0	0	0	Index high 8bit
0	0	0	0	0	0	0	1	0	0	Index low 8bit

Contrast Control Instruction

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	*	*	*	*	*	*	*	*	data high 8bit
0	1	*	*	CT5	CT4	CT3	CT2	CT1	CT0	data low 8bit
0	1	0	0	0	0	0	0	0	0	data high 8bit
0	1	0	0	0	1	0	0	0	0	data low 8bit

Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value						Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	3.20 x R	(Small)	(Light)
0	0	0	0	0	1	3.15 x R		
0	0	0	0	1	0	3.10 x R		
0	0	0	0	1	1	3.05 x R		
0	0	0	1	0	0	3.00 x R		
0	0	0	1	0	1	2.95 x R		
0	0	0	1	1	0	2.90 x R		
0	0	0	1	1	1	2.85 x R		
0	0	1	0	0	0	2.80 x R		
0	0	1	0	0	1	2.75 x R		
0	0	1	0	1	0	2.70 x R		
0	0	1	0	1	1	2.65 x R		
0	0	1	1	0	0	2.60 x R		
0	1	1	1	1	1	1.65 x R		
1	0	0	0	0	0	1.60 x R		
1	0	0	0	0	1	1.55 x R		
1	0	0	0	1	0	1.50 x R		
1	0	0	0	1	1	1.45 x R		
1	0	0	1	0	0	1.40 x R		
1	0	0	1	0	1	1.35 x R		
1	0	0	1	1	0	1.30 x R		
1	0	0	1	1	1	1.25 x R		
1	0	1	0	0	0	1.20 x R		
1	1	1	0	0	1	1.15x R		
1	1	1	1	0	0	0.20 x R		
1	1	1	1	0	1	0.15 x R		
1	1	1	1	1	0	0.10 x R		
1	1	1	1	1	1	0.05 x R	(Large)	(Deep)

8. Backlight Information

8.1 Specification

EL white / blue

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Voltage	Vrms	-	110 (AC)	-	-	-
Frequency	HZ	-	400	-	-	-
Brightness*	cd/m^2	48	60	-	-	110Vrms 400Hz
CIE Chromaticity Diagram	X	-	0.3019(white)	-	-	
			0.330 (blue)			
	Y	-	0.3929(white)	-	-	
			0.365 (blue)			
Current Dissipation	mA/cm^2	-	1.63	-	-	
Power Dissipation	mW/cm^2	-	26.29	-	-	
Color	Blue , white					

LED edge white

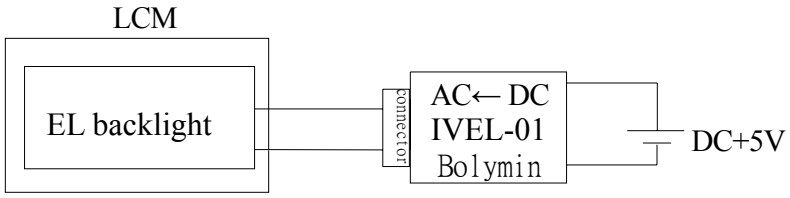
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	ILED	-	150	200	mA	V=3.2V
Supply Voltage	V	3.2	3.5	3.8	V	-
Reverse Voltage	VR	-	-	5	V	-
Luminous Intensity (backlight only)	IV	150	200	-	cd/m^2	ILED≦150mA
Luminous Intensity (measure on LCD)	IV	30	40	-	cd/m^2	ILED≦150mA
Wave Length	λp	-	-	-	nm	ILED≦150mA
Life Time	-	-	50000	-	Hr.	ILED≦150mA
Color	White					

LED edge amber/orange

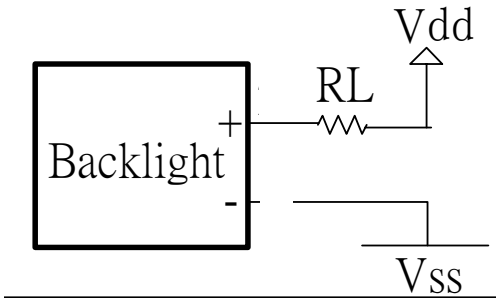
Parameter	Symbol		Min	Typ	Max	Unit	Test Condition
Supply Current	ILED		-	30	-	mA	-
Supply Voltage	V		-	1.9	-	V	-
Reverse Voltage	VR		-	-	TBD	V	-
Luminous Intensity (backlight only)	IV		-	TBD	-	cd/m^2	-
Luminous Intensity (measure on LCD)	IV		-	TBD	-	cd/m^2	-
Wave Length	λp	orange	-	635	-	nm	-
		amber	-	610	-	nm	
Life Time	-		-	50000	-	Hr.	-
Color	amber/orange						

8.2 Backlight driving methods

EL backlight



LED backlight



9. Quality Assurance

Screen Cosmetic Criteria

No.	Defect	Judgement Criterion	Partition
1	Spots	A)Clear Size:d mm / Acceptable Qty in active area d ≦0.1 Disregard 0.1<d≦0.2 6 0.2<d≦0.3 2 0.3<d 0 Note:Including pin holes and defective dots which must be within one pixel size. B)Unclear Size:d mm / Acceptable Qty in active area d ≦0.2 Disregard 0.2<d≦0.5 6 0.5<d≦0.7 2 0.7<d 0	Minor
2	Bubbles in Polarizer	Size:d mm / Acceptable Qty in active area d≦0.3 Disregard 0.3<d≦1.0 3 1.0<d≦1.5 1 1.5<d 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

10. Reliability

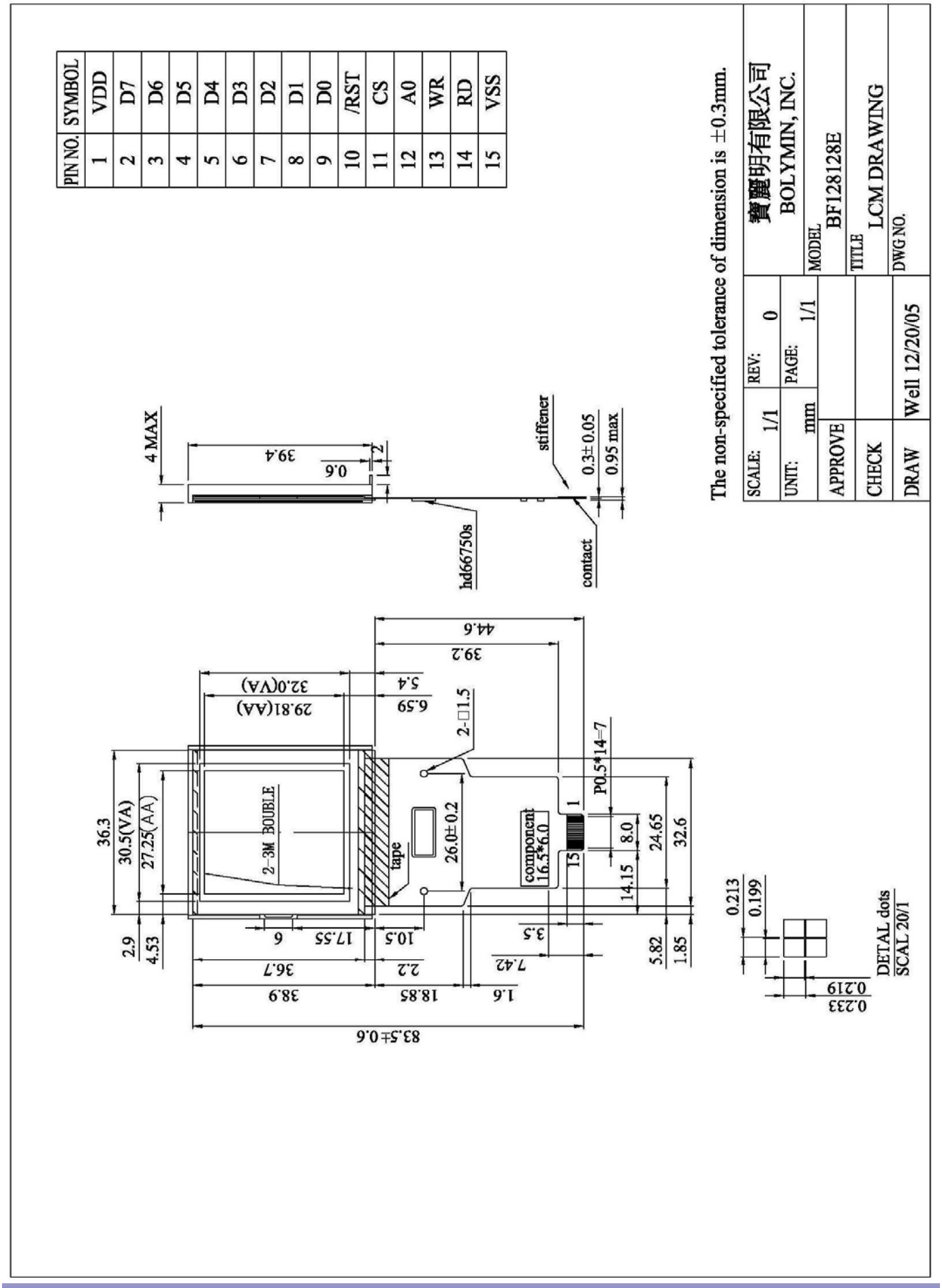
■Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 200hrs	-
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10℃ 200hrs	-
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	-
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	-
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	70℃,90%RH 96hrs	-
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40℃,90%RH 96hrs	-
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -10℃ 25℃ 60℃ 30min 5min 30min 1 cycle	-10℃/60℃ 10 cycles	-
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	-
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	-
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	-
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	-

***Supply voltage for logic system=5V. Supply voltage for LCD system = Operating voltage at 25℃

11. Appendix (Drawing , HD66750 controller data)

PIN NO.	SYMBOL
1	VDD
2	D7
3	D6
4	D5
5	D4
6	D3
7	D2
8	D1
9	D0
10	/RST
11	CS
12	A0
13	WR
14	RD
15	VSS



11-2 HD66750 controller data

11-2.1 Function description

Index (IR)

The index instruction specifies the RAM control indexes (R00 to R12). It sets the register number in the range of 00000 to 10010 in binary form.

R/W	RS
0	0
0	0

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	*	*	high 8bit
*	*	*	ID4	ID3	ID2	ID1	ID0	low 8bit

Status Read (SR)

The status read instruction reads the internal status of the HD66750S.

L6–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C5–0: Read the contrast setting values (CT5–0).

R/W	RS
1	0
1	0

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	L6	L5	L4	L3	L2	L1	L0	high 8bit
0	0	C5	C4	C3	C2	C1	C0	low 8bit

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	*	*	high 8bit
*	*	*	*	*	*	*	1	low 8bit

Driver Output Control (R01h)

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/128 shifts to COM1, and COM128/1 to COM128. When CMS = 1, COM1/128 shifts to COM128, and COM128/1 to COM1. Output position of a common driver shifts depending on the CN bit setting.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/128 shifts to SEG1, and SEG128/1 to SEG128. When SGS = 1, SEG1/128 shifts to SEG128, and SEG128/1 to SEG1.

CN: When CN = 1, the display position is shifted down by 32 raster-rows and display starts from COM33. When the liquid crystal is driven at a low duty ratio in the system wait state, it can be partially displayed at the center of the screen. For details, see the Partial-display-on Function section.

NL3-0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. CGRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	CMS	SGS	high 8bit
*	CN	*	*	NL3	NL2	NL1	NL0	low 8bit

LCD-Driving-Waveform Control (R02h)

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	CMS	SGS	high 8bit
*	B/C	EOR	NW4	NW3	NW2	NW1	NW0	low 8bit

Power Control (R03h)

BS2–0: The LCD drive bias value is set within the range of a 1/4 to 1/11 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

BT1-0: The output factor of VLOUT between two-times, five-times, six-times, and seven-times boost is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the booster consumes less current.

DC1-0: The operating frequency in the booster is selected. When the boosting operating frequency is high, the driving ability of the booster and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1-0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the driving ability of the booster and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and booster operation.

SLP: When SLP = 1, the HD66750S enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66750S enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)

b. Start oscillation

c. Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	BS2	BS1	BS0	BT1	BT0	high 8bit
*	*	DC1	DC0	AP1	AP0	SLP	STB	low 8bit

Contrast Control (R04h)

CT5–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 64-step contrast. For details, see the Contrast Adjuster section.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	*	*	high 8bit
*	*	CT5	CT4	CT3	CT2	CT1	CT0	low 8bit

Entry Mode (R05h)

Rotation (R06h)

The write data sent from the microcomputer is modified in the HD66750S and written to the CGRAM. The display data in the CGRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the CGRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the CGRAM.

AM1–0: Set the automatic update method of the AC after the data is written to the CGRAM. When AM1–0 = 00, the data is continuously written in parallel. When AM1–0 = 01, the data is continuously written vertically. When AM1–0 = 10, the data is continuously written vertically with two-word width (32-bit length).

LG1–0: Write again the data read from the CGRAM and the data written from the microcomputer to the CGRAM by a logical operation. When LG1–0 = 00, replace (no logical operation) is done. ORed when LG1–0 = 01, ANDed when LG1–0 = 10, and EORed when LG1–0 = 11.

RT2–0: Write the data sent from the microcomputer to the CGRAM by rotating in a bit unit. RT3–0 specify rotation. For example, when RT2–0 = 001, the data is rotated in the upper side by two bits. When RT2–0 = 111, the data is rotated in the upper side by 14 bits. The upper bit overflown in the most significant bit (MSB) side is rotated in the least significant bit (LSB) side.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	*	*	*	*	*	*	*	*	high 8bit
0	1	*	*	*	I/D	AM1	AM0	LG1	LG0	low 8bit

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	*	*	*	*	*	*	*	*	high 8bit
0	1	*	*	*	*	*	RT2	RT1	RT0	low 8bit

Display Control (R07h)

PS1–0: When PS1–0 = 01, only the upper eight raster-rows (COM1–COM8) are fixed-displayed in vertical smooth scrolling, and the other display raster-rows are smooth-scrolled. When PS1–0 = 10, the upper 16 raster-rows (COM1–COM16) are fixed-displayed. When PS1–0 = 11, the upper 24 raster-rows (COM1–COM24) are fixed-displayed. For details, see the Partial Smooth Scroll Display Function section.

DHE: When DHE = 1, the double height between raster-rows specified in the Double-height Display Position section is displayed. For details, see the Double-height Display section.

GS: When GS = 0, the grayscale level at a weak-colored display (DB = 01) is 1/3. When GS = 1, the grayscale level at weak-colored display is 1/2, and at strong-colored display (when DB = 10) it is 2/3.

REV: Displays all character and graphics display sections with black-and-white reversal when REV = 1. For details, see the Reversed Display Function section.

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG128 outputs and COM1 to COM128 outputs set to the GND level. Because of this, the HD66750S can control the charging current for the LCD with AC driving.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	*	*	*	*	*	*	*	*	high 8bit
0	1	*	*	PS1	PS0	DHE	GS	REV	D	low 8bit

Cursor Control (R08h)

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1–0 bits, and the display area is specified in a dot unit by the horizontal cursor position register (HS6–0 and HE6–0 bits) and vertical cursor position register (VS6–0 and VE6–0 bits). For details, see the Window Cursor Display section.

CM1–0: The display mode of the window cursor is selected. These bits can display a white-blink cursor, black-blink cursor, black-and-white reversed cursor, and black-and-white-reversed blink cursor.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	*	*	*	*	*	*	*	*	high 8bit
0	1	*	*	*	*	*	C	CM1	CM0	low 8bit

Double-height Display Position (R09h)

DS6–0: Specify any common raster-row position where the double-height display starts. Note that no scrolling is done by vertical scrolling. For details, see the Double-height Display section.

DE6-0: Specify any common raster-row position where the double-height display ends. Set the end position of the double-height display after the start position of the double-height display, satisfying the relationship DS6–0 ≦ DE6–0. When the area specifying the double height has an odd number of raster-rows,

the double-height display is done for the DE6–0 + 1 raster-rows.

When the double-height display is not used, set the DHE bit in the display-control instruction register to 0.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	DE6	DE5	DE4	DE3	DE2	DE1	DE0	high 8bit
*	DS6	DS5	DS4	DS3	DS2	DS1	DS0	low 8bit

Vertical Scroll Control (R0Ah)

SL6–0: Specify the display start raster-row for vertical smooth scrolling. Any raster-row from the first to 128th can be selected (table 14). After the 128th raster-row is displayed, the display restarts from the first raster-row. For details, see the Vertical Smooth Scroll section.

In partial smooth scrolling, these bits specify the display start raster-row of the next fixed-display raster-row.

For details, see the Partial Smooth Scroll Display Function section.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	*	*	high 8bit
*	SL6	SL5	SL4	SL3	SL2	SL1	SL0	low 8bit

Horizontal Cursor Position (R0Bh)

Vertical Cursor Position (R0Ch)

HS6-0: Specify the start position for horizontally displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that HS6–0 ≦ HE6–0.

HE6-0: Specify the end position for horizontally displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that HS6–0 ≦ HE6–0.

VS6-0: Specify the start position for vertically displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that VS6–0 ≦ VE6–0.

VE6-0: Specify the end position for vertically displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that VS6–0 ≦ VE6–0. In vertical scrolling, rewrite VS6–0 and

VE6–0 since this window cursor does not move vertically.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	HE6	HE5	HE4	HE3	HE2	HE1	HE0	high 8bit
*	HS6	HS5	HS4	HS3	HS2	HS1	HS0	low 8bit

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	VE6	VE5	VE4	VE3	VE2	VE1	VE0	high 8bit
*	VS6	VS5	VS4	VS3	VS2	VS1	VS0	low 8bit

RAM Write Data Mask (R10h)

WM15-0: In writing to the CGRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the CGRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. However, when AM = 10, the write data is masked with the set values of VM15–0 for the odd-times CGRAM write. It is also masked automatically with the reversed set values of VM15–0 for the even-times CGRAM write. For details, see the Graphics Operation Function section.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
VM15	VM14	VM13	VM12	VM11	VM10	VM9	VM8	high 8bit
VM7	VM6	VM5	VM4	VM3	VM2	VM1	VM0	low 8bit

RAM Address Set (R11h)

AD10-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the AM1–0 and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is not automatically updated. CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	AD10	VM9	VM8	high 8bit
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	low 8bit

Write Data to CGRAM (R12h)

WD15-0 : Write 16-bit data to the CGRAM. After a write, the address is automatically updated according to the AM1–0 and I/D bit settings. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS
0	1
0	1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	high 8bit
WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	low 8bit

Read Data from CGRAM (R12h)

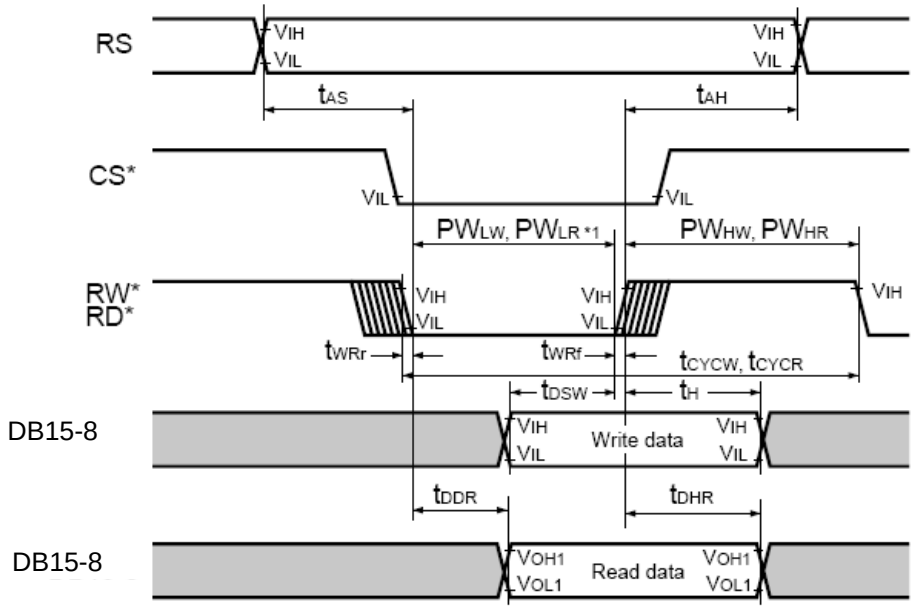
RD15-0 : Read 16-bit data from the CGRAM. When the data is read to the microcomputer, the firstword read immediately after the CGRAM address setting is latched from the CGRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed within the HD66750S, only one read can be processed since the latched data in the first word is used.

R/W	RS
1	1
1	1

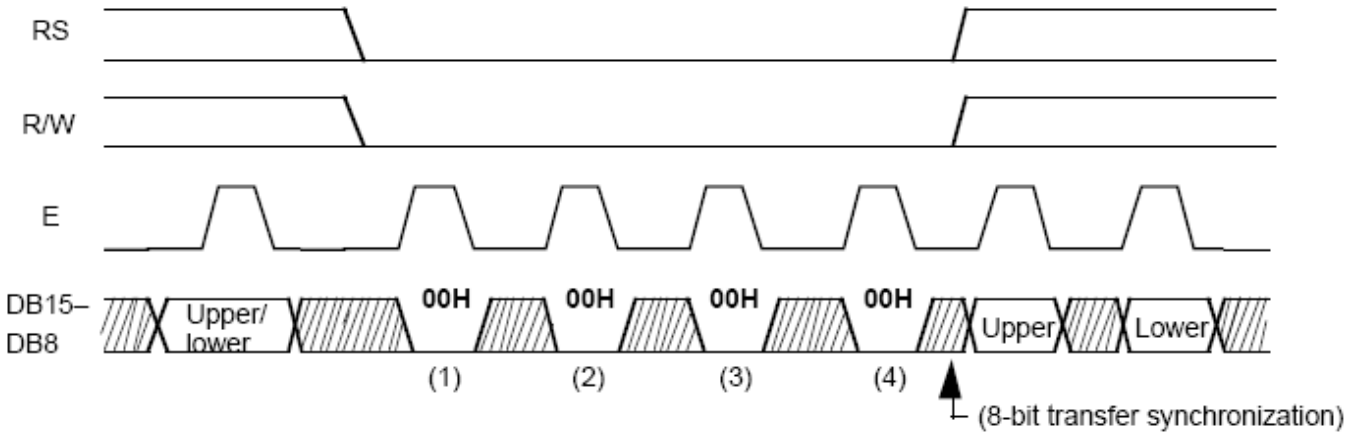
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	high 8bit
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	low 8bit

11-2.2 Timing characteristics

Item		Symbol	Min	Typ	Max	Unit
Bus cycle time	Write	t_{CYCW}	600	—	—	ns
	Read	t_{CYCR}	800	—	—	ns
Write low-level pulse width		PW_{LW}	120	—	—	ns
Read low-level pulse width		PW_{LR}	350	—	—	ns
Write high-level pulse width		PW_{HW}	300	—	—	ns
Read high-level pulse width		PW_{HR}	400	—	—	ns
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns
Address hold time		t_{AH}	20	—	—	ns
Write data setup time		t_{DSW}	60	—	—	ns
Write data hold time		t_{H}	20	—	—	ns
Read data delay time		t_{DDR}	—	—	300	ns
Read data hold time		t_{DHR}	5	—	—	ns



Note : PWLW and PWLR are specified in the overlapped period when CS* is low and WR* or RD* is low.


RS
R/W
E
DB15–
DB8
Upper/
lower
00H
00H
00H
00H
Upper
Lower
(1)
(2)
(3)
(4)
(8-bit transfer synchronization)