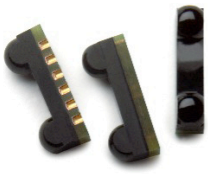
ASDL-3212

IrDA® Data Compliant Low Power 1.152 Mbit/s Infrared Transceiver

Data Sheet



Description

The ASDL-3212 is a new generation ultra small low cost infrared transceiver module which is compliance to IrDA Physical Layers specifications version 1.4 low power from 9.6Kbits/s to 1.152Mbit/s (MIR) with extended link distance. It is IEC825-Class 1 eye safe and designed for very low power consumption which is ideal for battery operated handheld devices. ASDL-3212 features lower pin count through integrated input-output function for interfacing with low voltage 1.5V

Applications

- Mobile data communication
  - Mobile Phones
  - PDAs
  - Digital Still Cameras
  - Printer
  - Handy Terminals
  - Industrial and Medical Instrument

Application Support Information

The Application Engineering Group is available to assist you with the application design associated with ASDL-3212 infrared transceiver module. You can contact them through your local sales representatives for additional details.

General Features

- Operating temperature from -25°C ~ 85°C
  - Critical parameters are guaranteed over temperature and supply voltage
- Vcc Supply 2.4 to 3.6 V
- Interface to Various Super I/O and Controller Devices
  - Support Integrated Input/Output Interface Voltage of 1.5 V
- Miniature Package
  - Height : 1.64 mm
  - Width : 7.00mm
  - Depth : 2.73mm
- Moisture Level 3
- No Programming required
- LED Stuck-High Protection
- High EMI Performance
- Designed to Accommodate Light Loss with Cosmetic Windows
- IEC 825-Class 1 Eye Safe

IrDA® Features

- Fully Compliant to IrDA 1.4 Physical Layer Low Power Specifications from 9.6 kbit/s to 1.15 Mbit/s
  - Typical Link Distance > 50cm
- Complete shutdown
- Low Power Consumption
  - Low shutdown current
  - Low idle current

Order Information

Part Number	Packaging Type	Package	Quantity
ASDL-3212-021	Tape and Reel	Front Option	2500

Marking Information

The unit is marked with '.PYWWLL'

P = Product code

Y = 1 digit numeric code for year

WW = 2 digits numeric code for work week

LL = 2 digits hexadecimal code for lot information

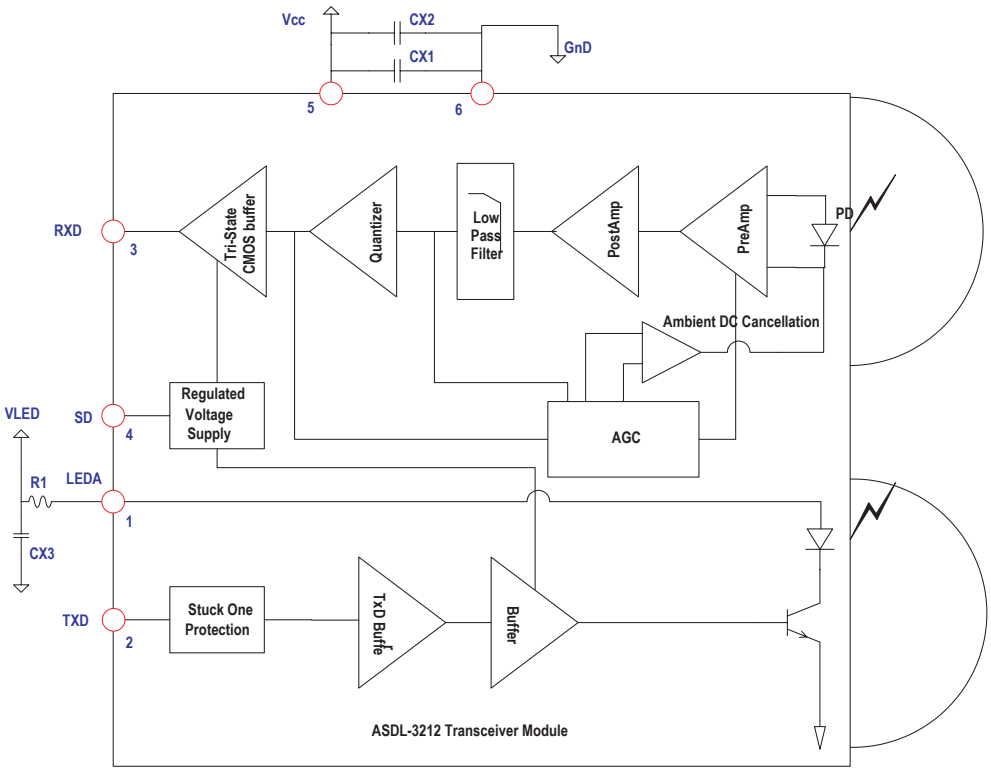


Figure 1. Functional Block Diagram

Recommended Application Circuit Components

	Recommended Value	Note
R1	2.7Ω ± 5%,0.25 watt for 2.4 ≤ VLED < 2.6	
	3.3Ω ± 5%,0.25 watt for 2.6 ≤ VLED < 2.8	
	3.9Ω ± 5%,0.25 watt for 2.8 ≤ VLED < 3.0	
	4.7Ω ± 5%,0.25 watt for 3.0 ≤ VLED < 3.3	
	5.6Ω ± 5%,0.25 watt for 3.3 ≤ VLED < 3.5	
	6.8Ω ± 5%,0.25 watt for 3.5 ≤ VLED < 3.8	
	8.2Ω ± 5%,0.25 watt for 3.8 ≤ VLED < 4.2	
	10Ω ± 5%,0.25 watt for 4.2 ≤ VLED < 4.7	
	12Ω ± 5%,0.25 watt for 4.7 ≤ VLED < 5.0	
CX2	100 nF, ± 20%, X7R Ceramic	7
CX1, CX3	6.8 μF, ± 20%, Tantalum	7

Note:
7. CX1 & CX2 must be placed within 0.7cm of ASDL-3212 to obtain optimum noise immunity

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Notes
1	LEDA	LED Anode		Note 1
2	TxD	IrDA transmitter data input.	Input, Active High	Note 2
3	RxD	IrDA receive data	Output, Active Low	Note 3
4	SD	Shutdown	Input, Active High	Note 4
5	Vcc	Supply Voltage		Note 5
6	GND	Ground		Note 6

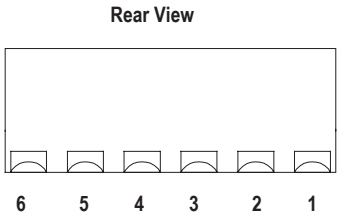


Figure 2. Pin out

Note:
1. Tied through external resistor, R1, to Vled. Refer to the table below for recommended series resistor value.
2. This pin is used to transmit serial data when SD pin is low. If held high for longer than 50 μs, the LED is turned off. Do NOT float this pin.
3. This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. The pin is in tri-state when the transceiver is in shutdown mode
4. Complete shutdown of IC and PIN diode. Do NOT float this pin.
5. Regulated, 2.4V to 3.6V
6. Connect to system ground.

CAUTION: The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Conditions	Ref
Storage Temperature	T_S	-40	+100	℃		
Junction Temperature	T_J		+100	℃		
Operating Temperature	T_A	-25	+85	℃		
LED Anode Voltage	V_{LEDA}	0	6	V		
Supply Voltage	V_{CC}	0	6	V		
Input Voltage : TXD, SD/Mode	V_I	0	6	V		
Output Voltage : RXD	V_O	0	6	V		
Peak LED Current	$I_{LED\ (PK)}$		300	mA	≤ 20% duty cycle, ≤ 217ns pulse width	Fig. 5
DC LED Current	$I_{LED\ (DC)}$		60	mA		Fig. 6

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature		T_A	-25		+85	℃	
Supply Voltage		V_{CC}	2.4		3.6	V	
Logic Input Voltage for TXD, SD/Mode		V_{IH}	1.3		1.8	V	
		V_{IL}	0		0.5	V	
Receiver Input Irradiance	Logic High	EI_H	0.0090		500	mW/cm^2	For in-band signals≤ 115.2kbit/s [8]
			0.0225		500		0.576 Mbit/s ≤ in-band signals ≤1.152 Mbit/s [8]
	Logic Low	EI_L			0.3	$\mu W/cm^2$	For in-band signals [8]
LED (Logic High) Current Pulse Amplitude		I_{LEDA}		250		mA	$V_{LED} = 3.0V$, $R_{LED} = 4.7\Omega$, $V_I(TxD) \geq V_{IH}$
Receiver Data Rate			0.0096		1.152	Mbit/s	
Ambient Light							See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels

Note : [8] An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 ≤ μp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical and Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C and Vcc set to 3.0V unless otherwise noted.

Receiver

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Viewing Angle		$2\theta_{1/2}$	30			°	
Peak Sensitivity Wavelength		λ_P		875		nm	
RxD_IrDA Output Voltage	Logic High	V_{OH}	1.3		1.8	V	I_{OH} = -100 μA, EI ≤ 0.3 μW/cm2
	Logic Low	V_{OL}	0		0.4	V	
RxD_IrDA Pulse Width (SIR) [9, 10]		$t_{RPW(SIR)}$		1.5		μs	$\theta_{1/2} \leq 15°$, C_L=9pF, EI = 10 mW/cm2
RxD_IrDA Pulse Width (MIR) [9, 11]		$t_{RPW(MIR)}$		250		ns	$\theta_{1/2} \leq 15°$, C_L=9pF, EI = 10 mW/cm2
RxD_IrDA Rise & Fall Times		t_r, t_f		60		ns	CL=9pF
Receiver Latency Time [12]		t_L			120	μs	EI = 9.0 μW/cm2
Receiver Wake Up Time [13]		t_{RW}			200	μs	EI = 10 μW/cm2

Infrared (IR) Transmitter

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
IR Radiant Intensity		I_{EH}	9	80		mW/sr	I_{LEDA} = 250mA, $\theta_{1/2} \leq 15°$, VI (TxD) ≤ VIH,
IR Viewing Angle		$2\theta_{1/2}$	30		60	°	
IR Peak Wavelength		λ_P		870		nm	
TxD_IrDA Logic Levels	High	V_{IH}	1.3		1.8	V	
	Low	V_{IL}	0		0.5	V	
TxD_IrDA Input Current	High	I_H			10	μA	$V_I \geq V_{IH}$
	Low	I_L			10	μA	$0 \leq V_I \leq V_{IL}$
Wake Up Time [14]		t_{TW}		200		ns	
Maximum Optical Pulse Width [15]		$t_{PW(Max)}$		70		μs	
TXD Pulse Width (SIR)		$t_{PW(SIR)}$		1.6		μs	$t_{PW\ (TXD)}$ =1.6μs at 115.2 kbit/s
TXD Pulse Width (MIR)		$t_{PW(MIR)}$		217		ns	$t_{PW\ (TXD)}$ =217ns at 1.152 Mbit/s
TxD Rise & Fall Times (Optical)		t_r, t_f			600 40	ns ns	$t_{PW(TXD)}$ =1.6μs at 115.2 kbit/s $t_{PW(TXD)}$ =217ns at 1.15 Mbit/s
IR LED Anode On-State Voltage		$V_{ON\ (LEDA)}$		2.0		V	I_{LEDA} = 250mA, $V_{I(TxD)} \geq V_{IH}$

Transceiver

Parameters		Symbol	Min.	Typ.	Max.	Units	Conditions
Input Current	High	I_H			1	μA	$V_I \geq V_{IH}$
	Low	I_L			1	μA	$0 \leq V_I \leq V_{IL}$
Supply Current	Shutdown	I_{CC1}			1	μA	$V_{SD} > V_{CC}$-1.3, T_A=25°C, no DC ambient
	Idle (Standby)	I_{CC5}		445	570	μA	$V_{I(TxD)} \leq V_{IL,\ EI=0}$

Note:

[9] An in-band optical signal is a pulse/sequence where the peak wavelength, λ_P, is defined as 850 nm ≤ λ_P ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification version 1.4.

[10] For in-band signals 115.2 kbit/s where 9 μW/cm2 ≤ EI ≤ 500 mW/cm2.

[11] For in-band signals 1.152 Mbit/s where 22 μW/cm2 ≤ EI ≤ 500 mW/cm2.

[12] Latency is defined as the time from the last TxD light output pulse until the receiver has recovered full sensitivity.

[13] Receiver Wake Up Time is measured from Vcc power ON to valid RxD output.

[14] Transmitter Wake Up Time is measured from Vcc power ON to valid light output in response to a TxD pulse.

[15] The Max Optical PW is defined as the maximum time which the IR LED will turn on, this, is to prevent the long Turn On time for the IR LED.

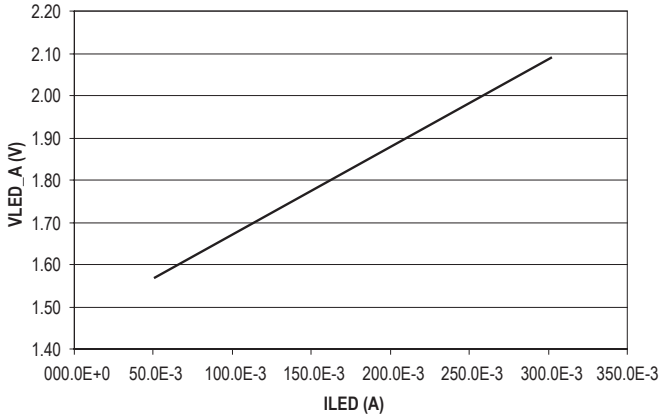


Figure 3. VLED_A vs. ILED

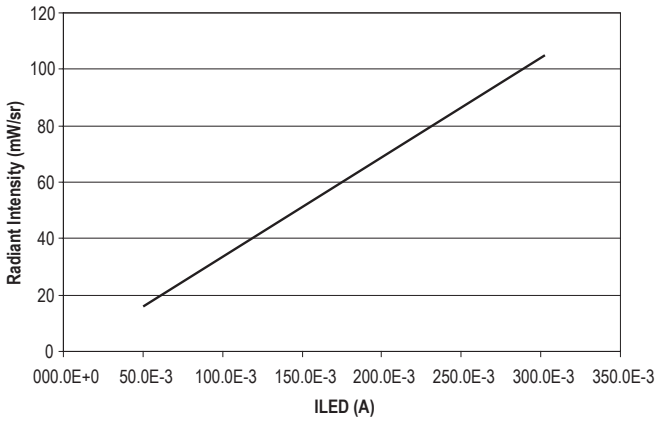


Figure 4. Radiant Intensity vs ILED

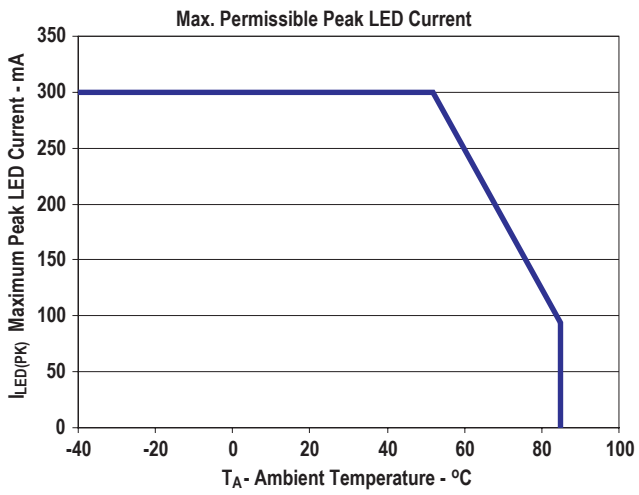


Figure 5. Maximum Peak LED current vs. ambient temperature. Derated based on T_{JMAX} = 100°C.

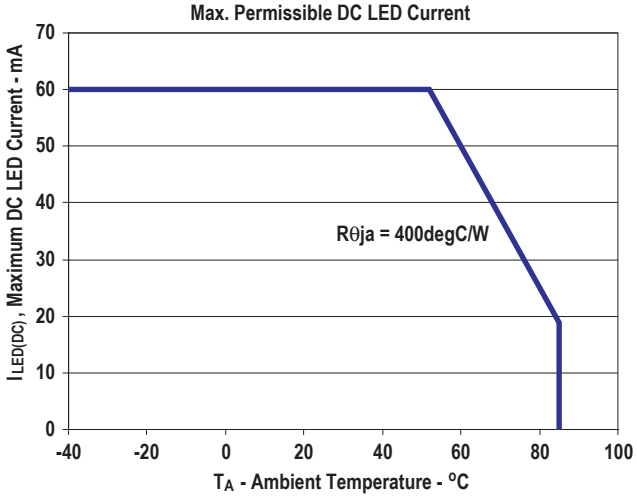


Figure 6 Maximum DC LED current vs. ambient temperature. Derated based on T_{JMAX} = 100°C.

ASDL-3212 (Option -021) Package Dimensions

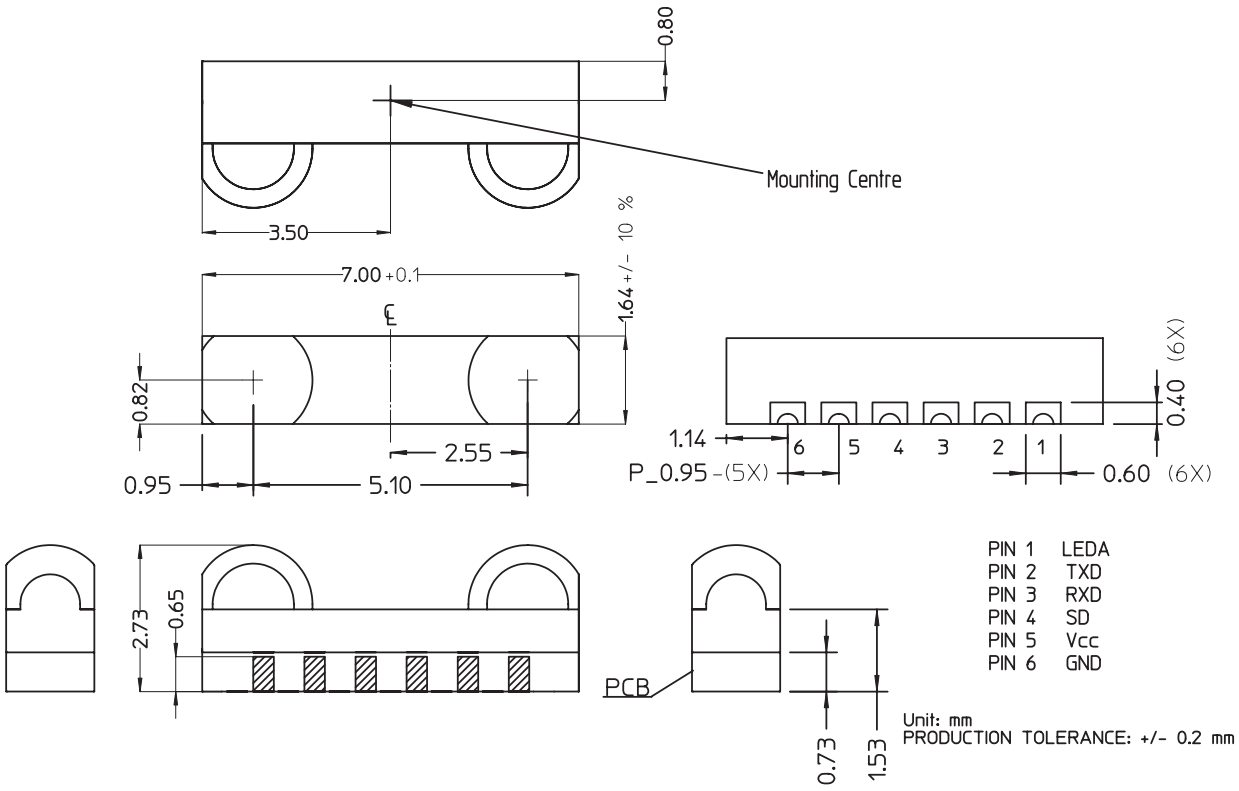


Figure 7. Package Dimension for ASDL-3212-021

ASDL-3212 (Option -021) Tape & Reel Dimensions

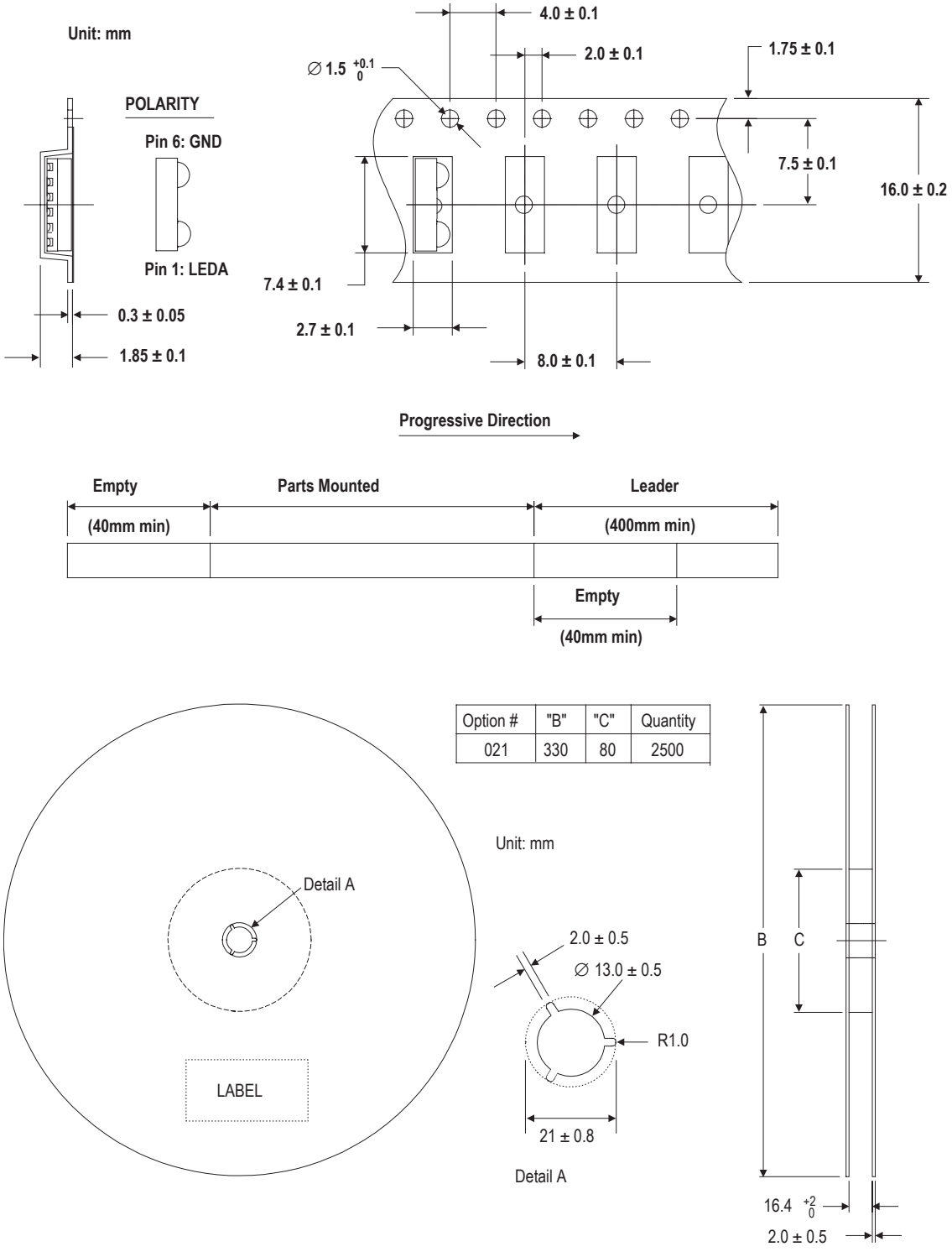


Figure 8. Tape and Reel dimensions

Moisture Proof Packaging

ASDL-3212 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.

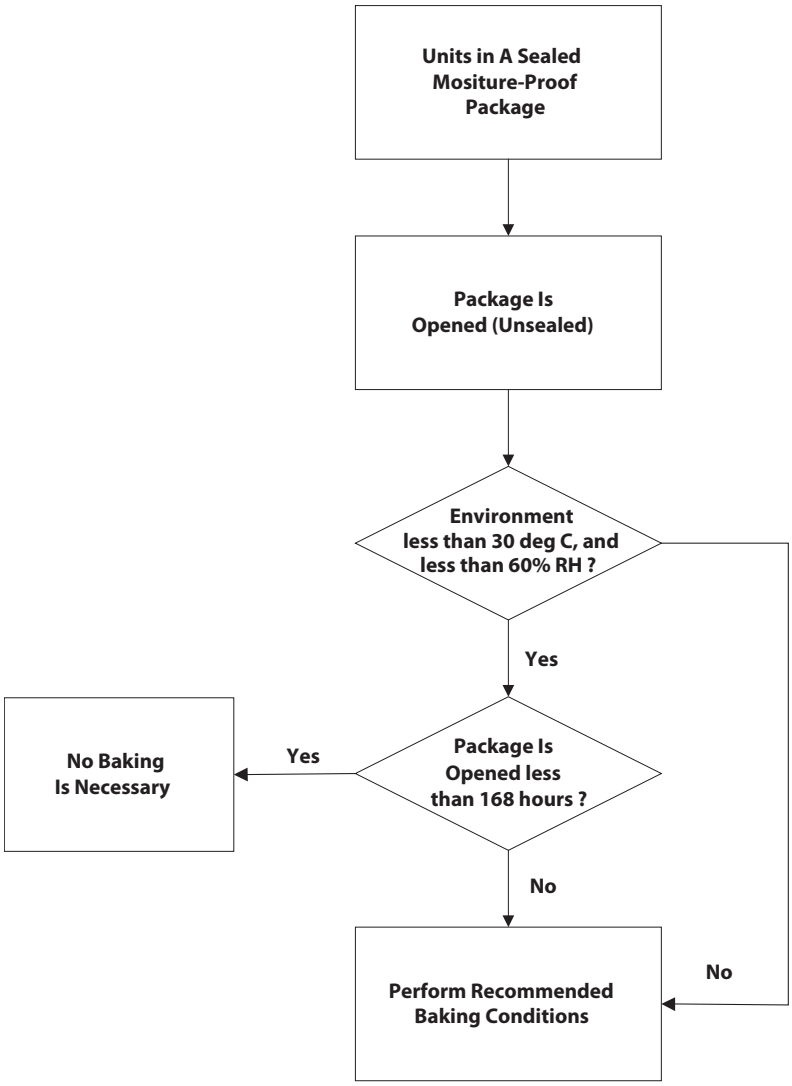


Figure 9. Baking Conditions Chart

Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp	Time
In reels	60 °C	≥ 48hours
In bulk	100 °C	≥ 4hours

Baking should only be done once.

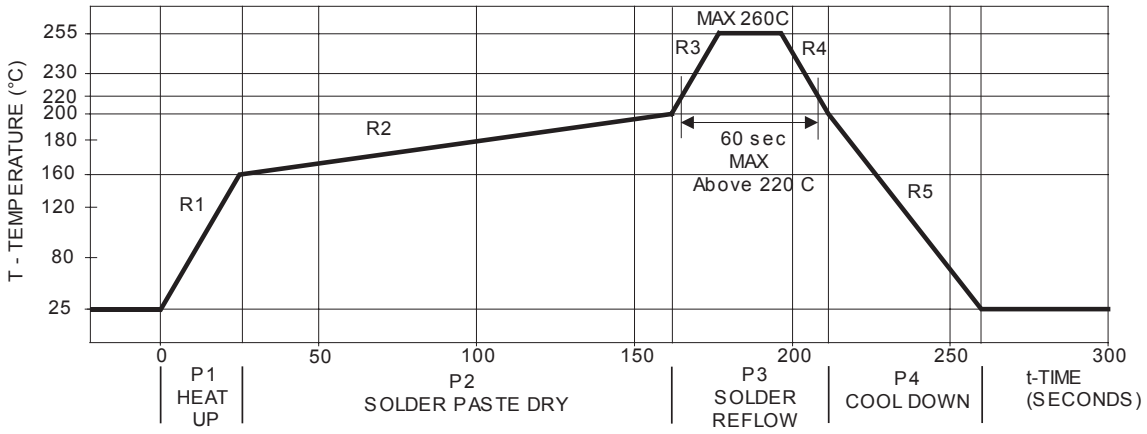
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 7 days if stored at the recommended storage conditions. If times longer than 7 days are needed, the parts

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	3°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3	200°C to 255°C (260°C at 10 seconds max)	4°C/s
	P3, R4	255°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and ASDL-3212 castellation pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and ASDL-3212 castellations.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and ASDL-3212 castellations to change dimensions evenly, putting minimal stresses on the ASDL-3212 transceiver.

Appendix A: ASDL-3212 (Option -021) SMT Assembly Application Note

Solder Pad, Mask and Metal Stencil

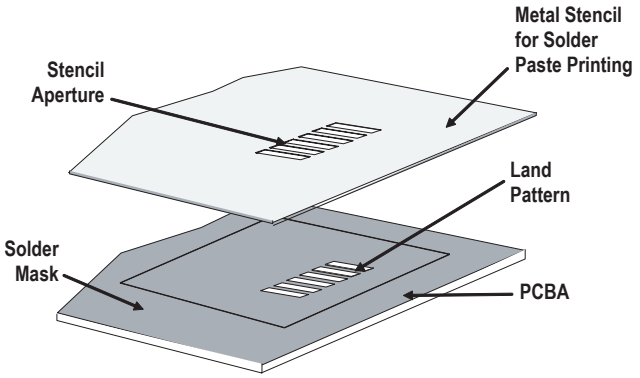


Figure A1. Stencil and PCBA

Recommended land pattern

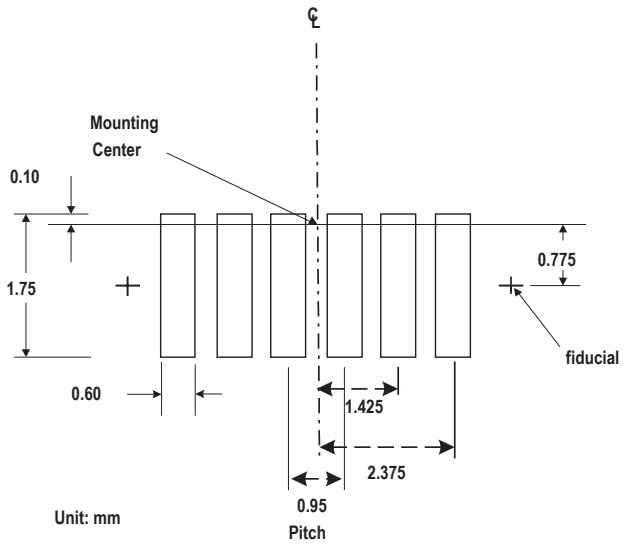


Figure A2. Land Pattern

Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.11mm (0.004 inch) or a 0.127mm (0.005 inch) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used. Compared to 0.127mm stencil thickness 0.11mm stencil thickness has longer length in land pattern. It is extended outwardly from transceiver to capture more solder paste volume. See figure 3.

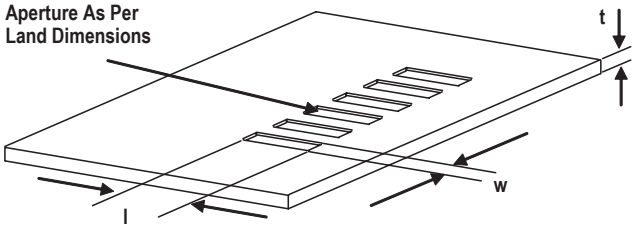
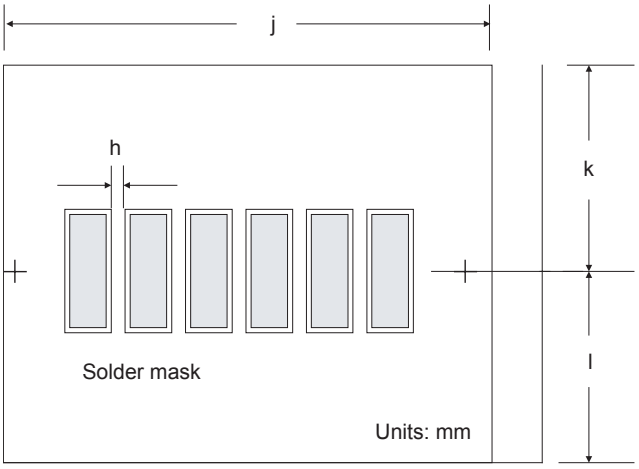


Figure A3. Solder stencil aperture

Stencil thickness, t (mm)	Aperture size (mm)	
	Length, l	Width, w
0.127mm	1.75 +/- 0.05	0.55 +/- 0.05
0.110mm	2.40 +/- 0.05	0.55 +/- 0.05

Adjacent Land Keepout and Solder Mask Areas

Adjacent land keepout is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area. The minimum solder resist strip width required to avoid solder bridging adjacent pads is 0.2mm. It is recommended that two fiducially crosses be placed at mid length of the pads for unit alignment.



Dimension	mm
h	0.2
l	3.0
k	3.0
j	8.6

Note: Wet/Liquid Photo-imaginable solder resist/mask is recommended.

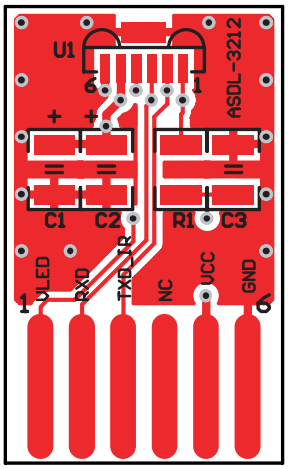
Figure A4. Adjacent Land Keepout and solder mask areas

Appendix B: PCB Layout Suggestion

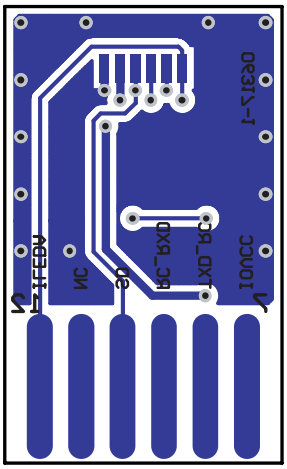
The ASDL-3212 is a shieldless part and hence does not contain a shield trace unlike the other transceivers. The effects of EMI and power supply noise can potentially reduce the sensitivity of the receiver, resulting in reduced link distance. The following PCB layout guidelines should be followed to obtain a good PSRR and EM immunity resulting in good electrical performance. Things to note:

1. The ground plane should be continuous under the part.
2. VLED and Vcc can be connected to either unfiltered or unregulated power supply. If VLED and Vcc share the same power supply, CX3 need not be used. The connections for CX1 and CX2 should be connected before the current limiting resistor R1.
3. CX2 is generally a ceramic capacitor of low inductance providing a wide frequency response while CX1 and CX3 are tantalum capacitor of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the VLED line, which carries a high current.
4. Preferably a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as Vcc, and sandwich that layer between ground connected board layers. The diagrams below demonstrate an example of a 4-layer board :

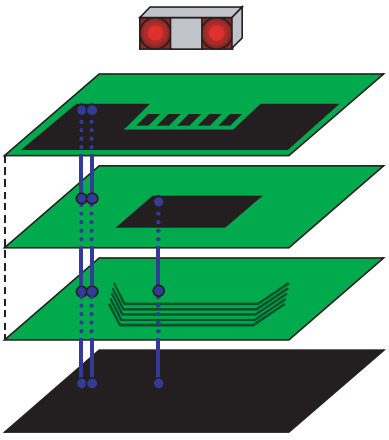
The area underneath the module at the second layer, and 3cm in all direction around the module is defined as the critical ground plane zone. The ground plane should be maximized in this zone. The layout below is based on a 2-layer PCB.



Top Layer



Bottom Layer



Top layer
Connect the module ground pin to bottom ground layer

Layer 2
Critical ground plane zone. Do not connect directly to the module ground pin

Layer 3
Keep data bus away from critical ground plane zone

Bottom layer (GND)

Appendix C: General Application Guide for the ASDL-3212 Infrared IrDA® Compliant 1.15Mb/s Transceiver

Description

The ASDL-3212 is a low-cost and ultra small infrared transceiver module that provides the interface between logic and infrared (IR) signals for through air, serial, half duplex IR data link. The device is designed to address the mobile computing market such as PDAs, as well as small embedded mobile products such as digital cameras and cellular phones. It is fully compliant to IrDA 1.4 low power specification from 9.6kb/s to 1.15Mb/s. The design of ASDL-3212 also includes the following unique features:

- Low passive component count;
- Shutdown mode for low power consumption requirement;
- Direct interface with Super I/O logic circuit.

Selection of Resistor R1

Resistor R1 should be selected to provide the appropriate peak pulse LED current at different ranges of Vcc as shown under "Recommended Application Circuit Components".

Interface to the Recommended I/O chip

The ASDL-3212's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required. Data rate from 9.6kb/s up to 1.15Mb/s is available at RXD pin.

Figures C1 and C2 show how ASDL-3212 fits into a mobile phone and PDA platform respectively.

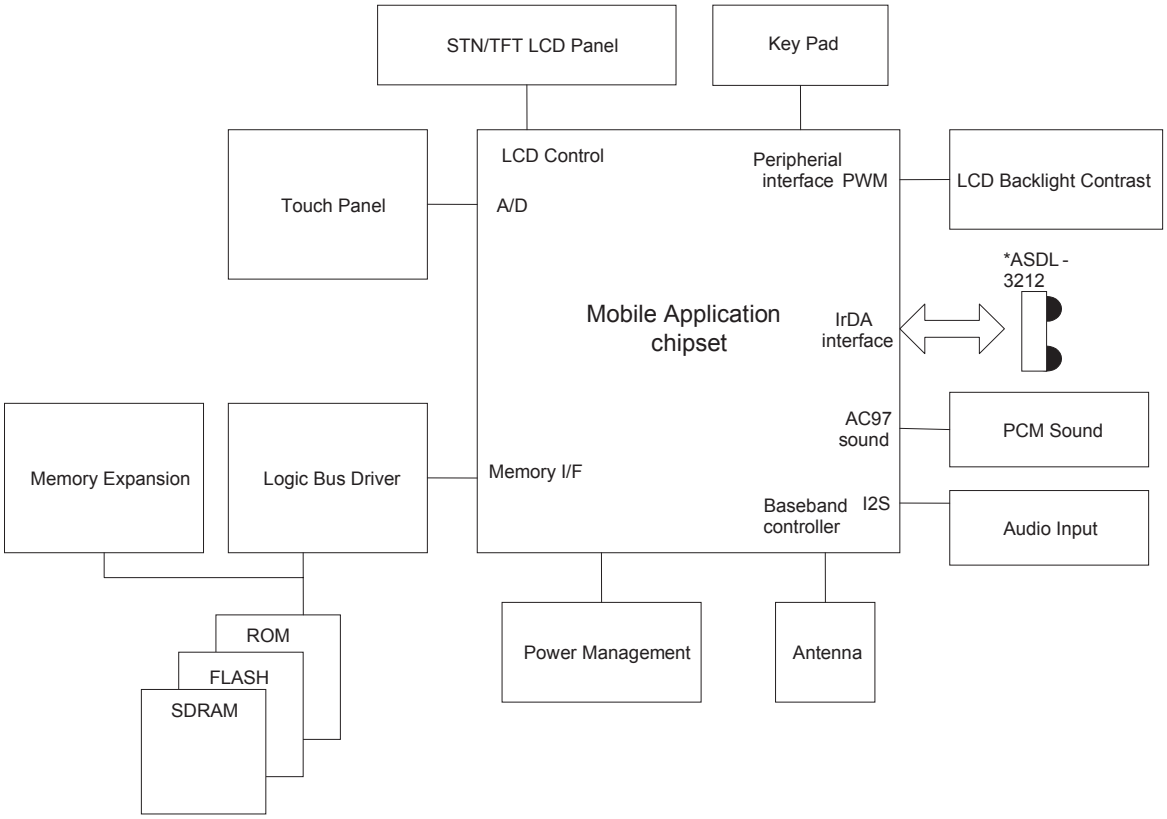


Figure C1. Mobile Application Platform

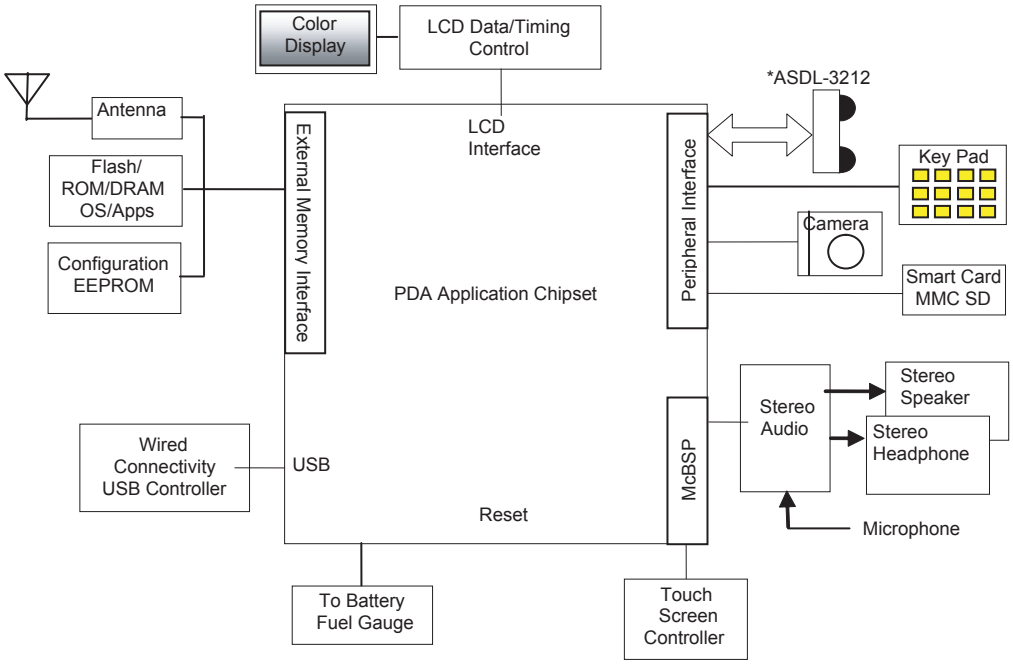


Figure C2. PDA Platform

The link distance testing was done using typical ASDL-3212 units with SMC's FDC37C669 and FDC37N769 Super I/O controllers. An IR link distance of up to 50 cm was demonstrated.

Appendix D: Window Design for ASDL-3212

Window Dimension

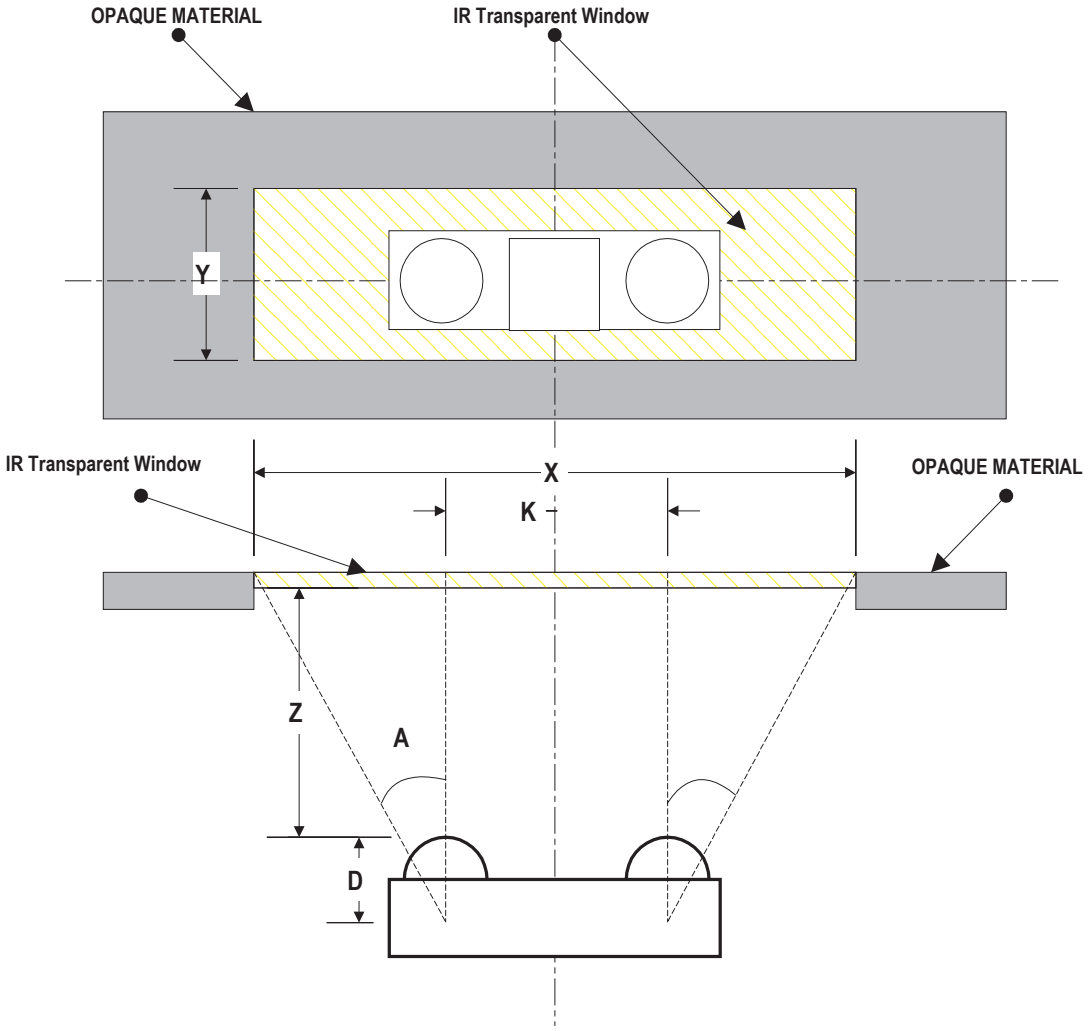


Figure D1. Window Design for ASDL-3212

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cones angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 300 and the maximum size corresponds to a cone angle of 600.

In figure D1, X is the width of the window, Y is the height of the window and Z is the distance from the ASDL-3212 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.1mm. The equations for computing the window dimensions are as follows:

$X = K + 2*(Z+D)*\tan A$

$Y = 2*(Z+D)*\tan A$

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

$Z' = Z + t/n$

where 't' is the thickness of the window and 'n' is the refractive index of the window material.

The depth of the LED image inside the ASDL-3212, D, is 4.32mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 150 and the maximum is 300. Assuming the thickness of the window to be negligible, the equations result in the following table and figures:

Module Depth

	Aperture Width (x, mm)		Aperture height (y, mm)	
(z) mm	Max	min	Max	Min
0	10.09	7.42	4.99	2.32
1	11.24	7.95	6.14	2.85
2	12.40	8.49	7.30	3.39
3	13.55	9.02	8.45	3.92
4	14.71	9.56	9.61	4.46
5	15.86	10.09	10.76	4.99
6	17.02	10.63	11.92	5.53
7	18.17	11.17	13.07	6.07
8	19.33	11.70	14.23	6.60
9	20.48	12.24	15.38	7.14

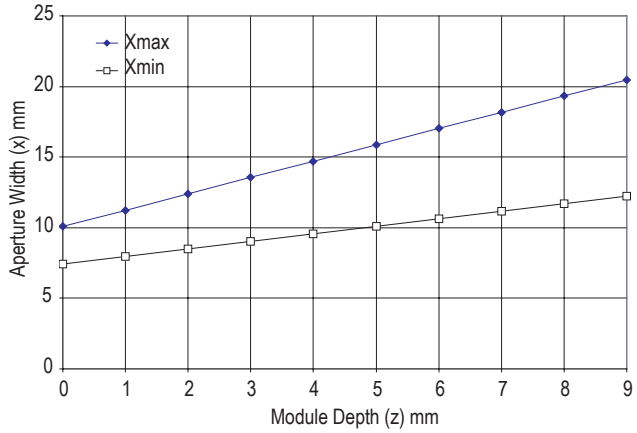


Figure D2. Aperture Height (x) vs. Module Depth (z)

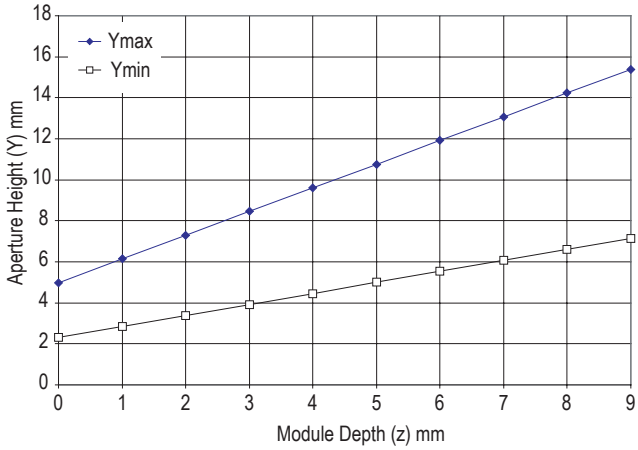


Figure D3. Aperture Height (y) vs. Module Depth (z)

The recommended minimum aperture width and height is based on the assumption that the center of the window and the center of the module are the same. It is recommended that the tolerance for assembly be considered as well. The minimum window size which will take into account of the assembly tolerance is defined as:

X (min + assembly tolerance) = Xmin + 2*(assembly tolerance) (Dimensions are in mm)

Y (min + assembly tolerance) = Ymin + 2*(assembly tolerance) (Dimensions are in mm)

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 885 nm. The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Recommended Plastic Materials:

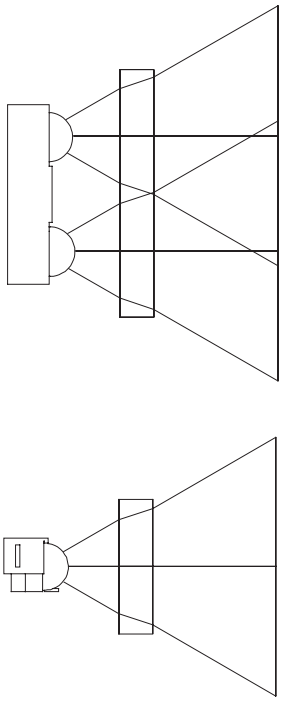
Material #		Haze	Refractive Index
Lexan 141	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

Note: 920A and 940A are more flame retardant than 141.

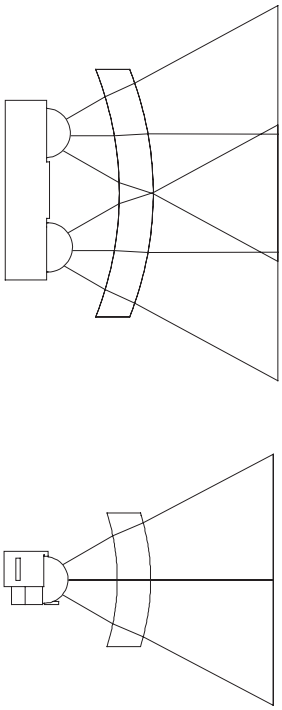
Recommended Dye: Violet #21051 (IR transmissant above 625mm)

Shape of the Window

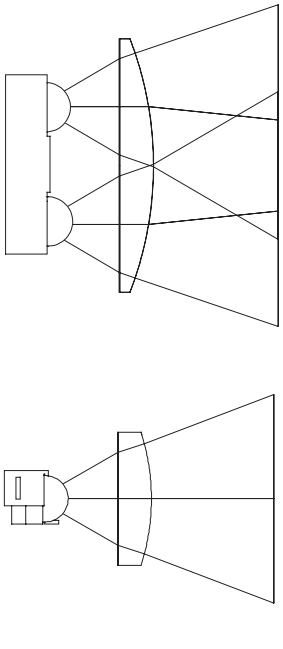
From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode. If the window must be curved for mechanical or industrial design reasons, place the same curve on the backside of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve. The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



Flat Window, (First Choice)



Curved Front and Back, (Second Choice)



Curved Front, Flat Back, (Do not use)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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