# HFBR-5701L/5710L/5720L/5730L and HDMP-1687 Reference Design for 1.25 GBd Gigabit Ethernet and 1.0625 GBd Fiber Channel Applications

## Application Note 1242

### Introduction

Avago's objective in creating this 1.25 GBd Gigabit Ethernet/1.0625 GBd Fiber Channel physical layer reference design is to generate a ready-to-use physical layer solution to assist our customers in verifying the performance of our optical transceivers and SerDes as part of the system design process. This particular reference design is the principle application example for our new HFBR-5701L/5710L/5720L/5730L Small Form-Factor Pluggable (SFP) Optical Transceivers, and our current HDMP-1687 Quad-Channel Serializer/DeSerializer (SerDes).

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2. Reference design functional topology and utilization description
3. Summary of test results
4. Conclusions and recommendations
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A. Test configuration
B. Detailed schematics

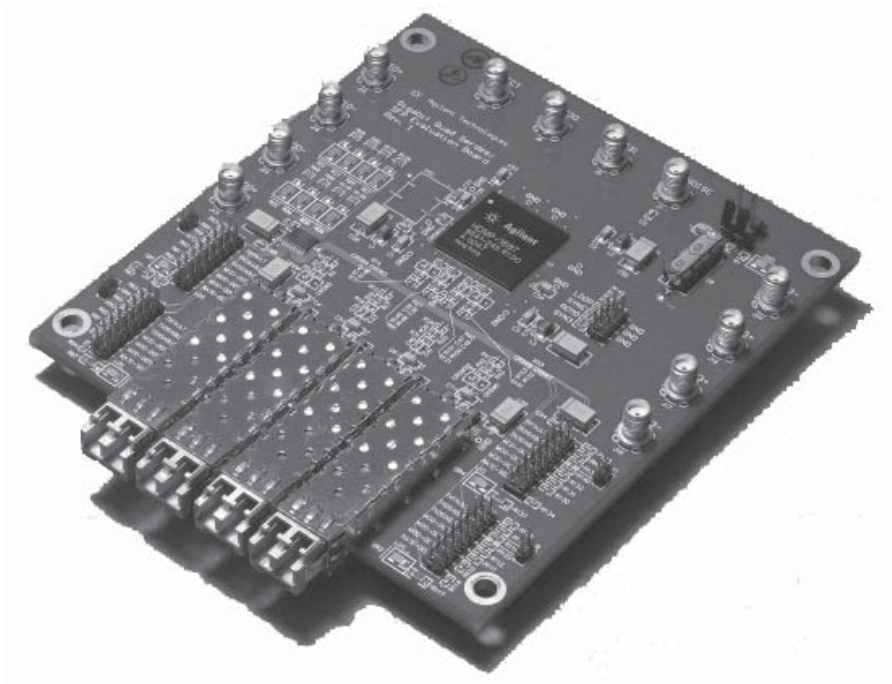

**Figure 1. 1.25 GBd reference design PCB including HFBR-5701L/5710L/5720L/5730L (SFP) and HDMP-1687 (Quad SerDes)**

## 1. A Brief Introduction to GigaBit Ethernet

GigaBit Ethernet (GBE) is a high speed, network and physical layer specification for Local Area Network (LAN) applications. It is defined in the IEEE 802.3 2000 Edition specification. A typical LAN may include Switch to Switch Interfaces, Switched Backplane Applications, and File Server Interfaces. A conceptual LAN application with multi-rate switching from 10BASE-X, to 100BASE-X, to 1000BASE-SX (i.e., GBE) is shown in *Figure 2* from Reference [1].

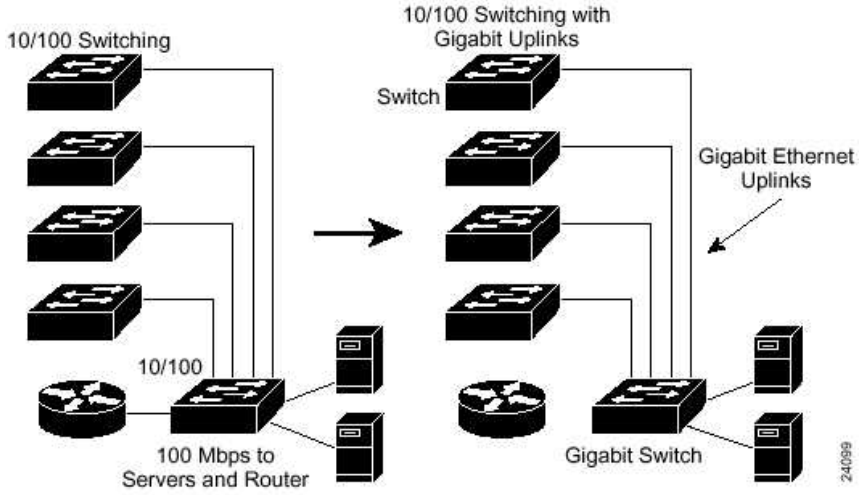


**Figure 2. Representative GigaBit Ethernet (GBE) application**

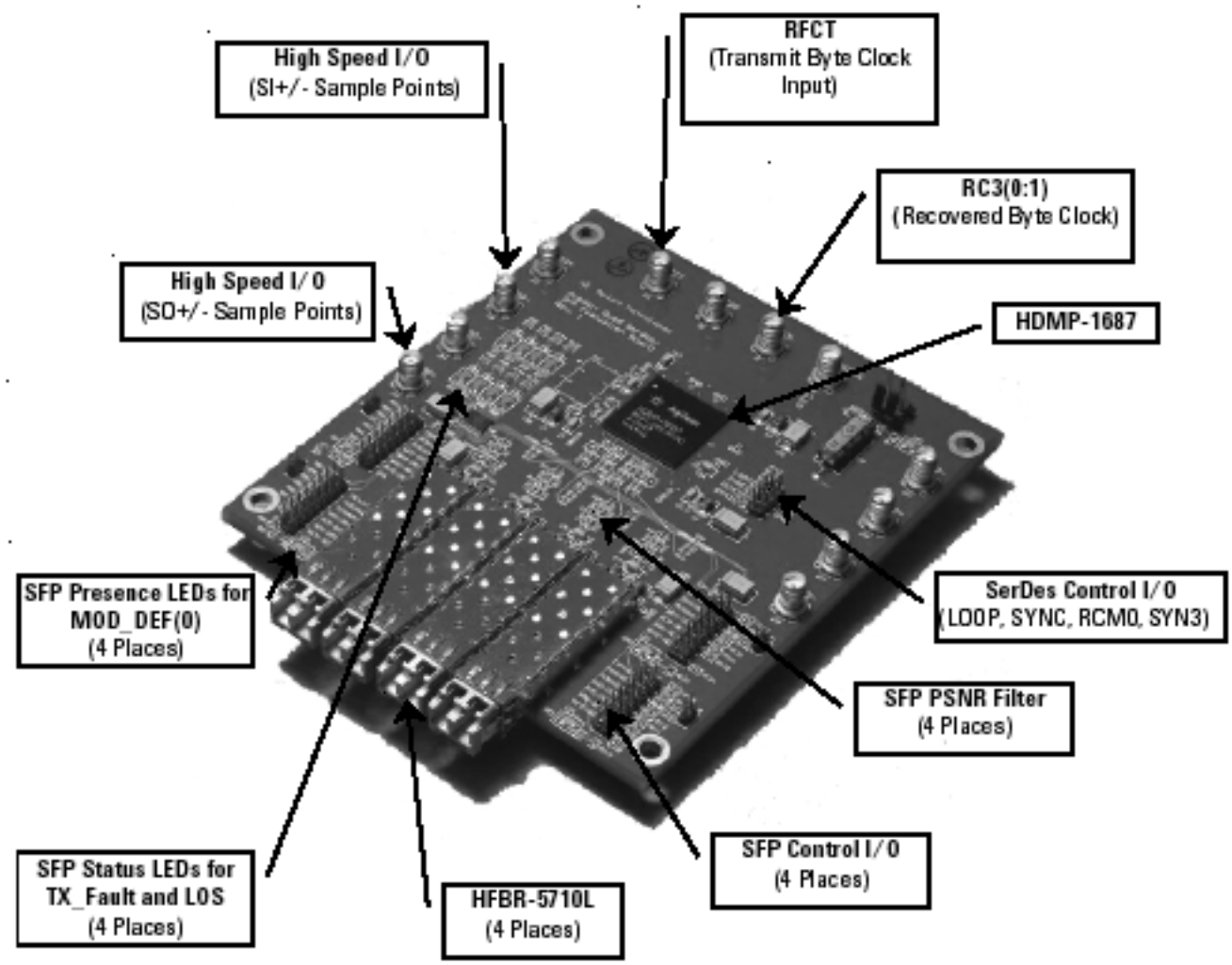


**Figure 3. Basic topology of 1.25 GBd reference design**

## 2. Reference Design Functional Topology and Utilization Description

As shown in *Figure 3*, this reference design demonstrates Avago's HFBR-5710L transceiver and HDMP-1687 Quad SerDes. Up to four HFBR-5710L SFPs can be utilized simultaneously demonstrating each of the SerDes serial channels. This reference design is also compatible with HFBR-5701L/5710L/5720L/5730L.

### SFP

Each of the SFP ports is supported by (1) a Cage and Connector, (2) High Speed I/O, (3) Control I/O, (4) Power Supply Filtering, and (5) LED Status Indicators. A schematic depicting these functions is shown in *Figure 4*. A topological layout of reference designators is shown in *Figure 5*.

1. *Cage and Connector*
The surface mounted cage and connector are derived directly from the SFP MSA definition. The footprints required on the host PCB can be found in the product data-sheet for the HFBR-5710L.

2. *High Speed I/O*
The SFP Receiver (RD+/–) and Transmitter (TD+/-) data signaling transmission lines are implemented by use of vertically stacked, broadside coupled, striplines buried in the internal planes of the PCB which route these signals to and from the SerDes Transmitter (SO+/–) and Receiver (SI+/–) pins respectively. This design could have equivalently been done with edge-coupled striplines which would minimize the PCB thickness, but increase the number of cross-over points between HSIO lines due to the orientation of pins on the SFP and the SerDes.

They can also be routed to external sampling SMA connectors for SFPs U2 and U5 by virtue of switches CRSW1 through CRSW8 as described in *Table 1*. These switches are manually enabled by soldering a series coupling capacitor in one of two positions simulating a SPDT switch.

These differential signaling transmission lines achieve the required 50 Ohm characteristic impedance for both the even and odd mode signal propagation. The SFP is internally ac coupled and internally terminated with a 100 Ohm differential load, thus no external matching, coupling, nor biasing components are required on the host PCB.

3. *Control I/O*
All Control I/O signals defined in the SFP MSA are implemented on the reference board. These are described in detail in *Table 1*. There are four headers H4, H6, H8, and H10 which service each of four SFPs U2, U3, U4, and U5 respectively with Control I/O. All control signals are LVTTL (3.3 V) compliant.

Each header can be used either by an external ribbon cable to a customer application or by implementing standard jumpers between the two rows of pins on the header. When using a ribbon cable (e.g., to verify SFP timing) standard LVTTL signals should be used noting that the required pull-up resistors are already implemented on the reference board. When the jumpers are used, the output TX_FAULT, LOS, and MOD-DEF0 are indicated by LEDs. Also, one of the TX_DISABLE jumpers can be used as a manual switch to control the SFP transmitter by enabling or disabling the laser output as desired. Both of the default and optional jumper settings are described in more detail in *Table I*.

4. *Power Supply Filtering*
The SFP MSA specified power supply noise rejection (PSNR) filter is present for each of the four SFP ports. This filter is required on any host PCB. It serves to significantly attenuate any power supply noise with frequency content above 100 kHz.

5. *LED Status Indicators*
There are LEDs on the reference design to indicate TX_FAULT, LOS, and MOD-DEF(0) for each of the four SFPs. RD1, RD3, RD5, and RD7 are red LEDs associated with U2, U3, U4, and U5 respectively. These illuminate only when the SFP TX_FAULT output is exercised due to an eye safety condition event involving the SFP transmitter. RD2, RD4, RD6, and RD8 are red LEDs associated with U2, U3, U4, and U5 respectively. These illuminate only when the SFP LOS output is exercised due to a broken fiber or remote disabled laser event involving the SFP receiver. GR1, GR2, GR3, and GR4 are green LEDs associated with U2, U3, U4, and U5. These illuminate only when the SFP is plugged into the surface mounted connector and utilize the MOD-DEF(0) output which is grounded when the SFP module is inserted.

### SerDes

The SerDes functionality is supported by (1) High Speed I/O, (2) Control I/O, and (3) Power Supply Filtering. A schematic depicting these functions is shown in *Figure 4.* A topological layout reference designators is shown in *Figure 5*.

1. *High Speed I/O (HSIO)*
The SerDes HSIO serial data signaling for transmitter (SI+/–) and receiver (SO+/–) is implemented as described in the previous SFP HSIO section. However, the SerDes SI+/– input does require a differential 100 Ohm termination on the host PCB.

The SerDes parallel data signaling is implemented by a series of 40 equal-length loopback transmission lines buried in the internal planes of the PCB. Thus, the Quad SerDes is always in a loopback configuration for the parallel I/O. These signal lines are single ended striplines compatible with the LVTTL levels required for the SerDes.

The required 125 MHz transmit byte clock and receiver PLL frequency reference must be supplied externally via the RFCT SMA port. It is important that the HDMP-1687 product data sheet is reviewed to ensure that the proper timing relationship between RFCT and the parallel data setup and hold times be established. Either a clock derived from the data pattern generator or from a Clock and Data Recovery (CDR) circuit can be used to ensure that the appropriate timing relationships between clock and data are achieved. A frequency divide by 10 circuit is required to provide the required 125 MHz clock derived from the 1.25 Gbd data.

Finally, the recovered byte clock from the fourth SerDes channel [0:3] is available via the RC3[0:1] SMA connectors.

2. *Control I/O*

Four primary Control I/O signals defined in the HDMP-1687 product data sheet are implemented via the H3 header. These include LOOP, SYNC, RCMO, and SYN3, which are all LVTTL signals as described in *Table 1* as well as the SerDes data sheet.

The H2 header can be used either by an external ribbon cable to a customer application or by implementing standard jumpers between the two rows of pins on the header. When using a ribbon cable (e.g., to monitor comma detection) standard LVTTL signals should be used noting that the required pull-up resistors are implemented on the reference board. When the jumpers are used, typically the LOOP and SYNC are disabled by attaching the appropriate jumpers whereas RCMO and SYN3 may be left unconnected.

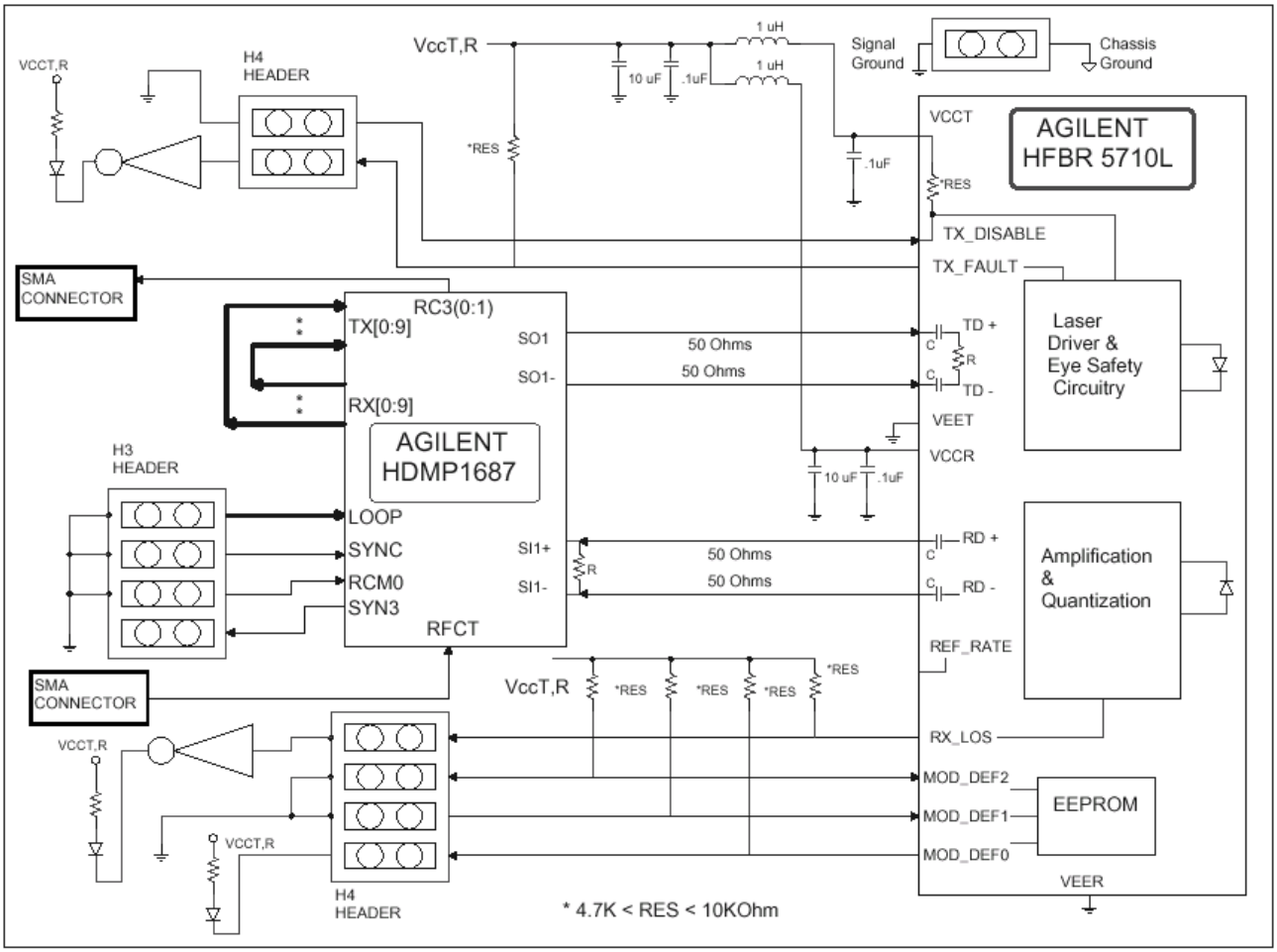


**Figure 4. Reference design schematic (single channel depicted) in typical configuration**

3. *Power Supply Filtering*
A number of bypass capacitors implement power supply filtering for the SerDes as shown in the detailed schematic in *Appendix B*. These capacitors are placed on virtually all $V_{CC}$ pins. In particular, the power supplies for the transmitter and receiver PLLs incorporate a single stage L-C filter as well since these inputs are particularly sensitive to noise. The details of the recommended power supply filtering for the SerDes and optimal placement (i.e., as close to the pins as possible) can be found in the HDMP-1687 product data sheet.

## 3. Summary of Test Results

Significant testing was performed in order to determine compliance to IEEE 802.3 (GBE) specifications of the HFBR-5710L and HDMP-1687 in the reference design. A summary of typical data is demonstrated in *Figures 6* and *7*. The basic test configuration is shown in *Figure 8* in *Appendix B* where it should be noted that the divide by 10 circuit required to provide the transmit byte clock for the SerDes can be obtained by contacting your local Avago field sales office. Also, an additional application note detailing the technical issues with this reference design as well as the comprehensive test results is available.

*Figure 6* shows a typical optical eye pattern at test point (TPO2) after the signal has traversed the entire physical layer and been looped back through the SerDes as shown in *Figure 8*. In this case, a PRBS $2^7$-1 pattern at 1.25 GBd was used to perform this test. It can be seen that the eye mask margin to the standard GBE optical eye mask is greater than 55%. Also, rise time of 231 Picoseconds and the total jitter of 92 Picoseconds provide significant margin to GBE specifications.

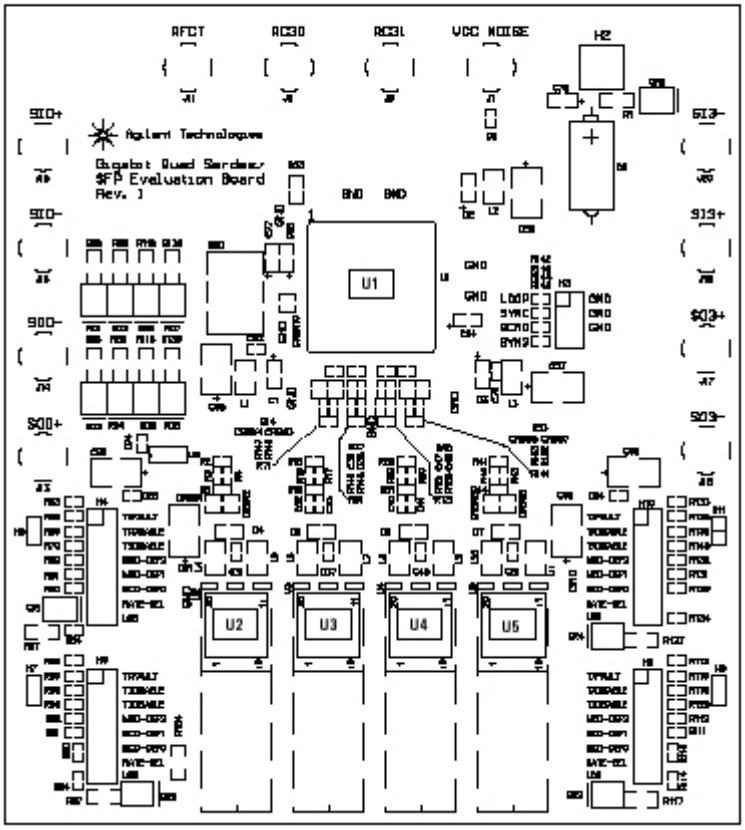


**Figure 5. Detailed topology of reference design**

**Table 1. Detailed Topology of Reference Design Connection Definitions**

| Reference Designator | Function | Description | Notes |
|---|---|---|---|
| H2 | VCC/GND | Power Supply<br>VCC - Left; GND - Right | 3.3 ± 5% Volts |
| GR5 | Power Supply Indicator | Green LED illuminates when power supply is energized | |
| $V_{CC}$ Noise | Power Supply Noise Injection | Optional Test point for injecting power supply noise and AC coupling to the VCC supply | |
| U1 | Quad SerDes | HDMP-1687 GBE Quad SerDes | See Product Data Sheet for detailed description |
| H3 | LOOP | Normal operation when this jumper is ON; Option connects SI+/– to SO+/– in a loop-back configuration when this jumper is OFF | LVTTL(3.3 V) Input |
| H3 | SYNC | Normal operation when this jumper is ON enables synchronization of the SerDes to the incoming serial data stream upon receipt of a comma character; Option disables this feature when this jumper is OFF | LVTTL(3.3 V) Input |
| H3 | RCM0 | Normal operation when this jumper is ON selects the clock rate for RFCT at 125 MHz; Option when this jumper is OFF selects 62.5 MHz | LVTTL(3.3 V) Input |
| H3 | SYN3 | Comma Detect Output for the fourth channel of the Quad SerDes no jumper required | LVTTL(3.3 V) Output |
| RFCT | Transmit Byte Clock | 125 MHz Clock for both Tx and Rx PLLs on SerDes; Must bear appropriate timing relationship to data data (see HDMP-1687 Product Data Sheet) | LVTTL(3.3 V) Input<br>Cannot be used for RFCT input |
| RC30 | Recovered Byte Clock | 125 MHz Recovered Clock | LVTTL(3.3 V) |
| RC31 | Recovered Byte Clock | 125 MHz Recovered Clock Bar | LVTTL(3.3 V) |
| U2 | SFP Cage & Connector | SFP MSA Transceiver Module is inserted here GR1, RD1, RD2, H4, H5, SI0+/– (CRSW1/2), SO0+/– (CRSW3/4) | Any SFP MSA compatible DUT |
| U3 | SFP Cage & Connector | SFP MSA Transceiver Module is inserted here GR2, RD3, RD4, H6, H7 | Any SFP MSA compatible DUT |
| U4 | SFP Cage & Connector | SFP MSA Transceiver Module is inserted here GR3, RD5, RD6, H8, H9 | Any SFP MSA compatible DUT |
| U5 | SFP Cage & Connector | SFP MSA Transceiver Module is inserted here GR4, RD7, RD8, H10, H11, SI3+/– (CRSW5/6), SO3+/– (CRSW7/8) | Any SFP MSA compatible DUT |
| U6 | Logic Inverter | Control I/O Logic Level Inverter TX_LOS & TX_FAULT for each SFP module | Controls RED LED indicators RD1-RD8 |
| H5, H7, H9, H11 | Jumper Pull-up | Jumper for Optional TX_DISABLE pull-up resistor only for SFPs without an internal pull-up resistor | Normally Not Connected |
| H4, H6, H8, H10 | TX_FAULT | Fault monitor output from SFP, High when a laser fault condition exists and Low otherwise. Jumper is Normally ON enabling LED indicator. | LVTTL(3.3 V) |
| H4, H6, H8, H10 | TX_DISABLE | Jumper which is Normally OFF. Used only with SFP modules that do not have an internal pull-up resistor for TX_DISABLE | LVTTL(3.3 V) |
| H4, H6, H8, H10 | TX_DISABLE | Jumper which Enables or Disables the Optical Transmitter: ON (TX Enabled) or OFF (TX Disabled) | LVTTL(3.3 V) |

**Table 1. Detailed Topology of Reference Design Connection Definitions** (continued)

| Reference Designator | Function | Description | Notes |
|---|---|---|---|
| H4, H6, H8, H10 | MOD-DEF (2) | Module definition and presence bit (2) input/output. Serial Data transfer from/to EEPROM. Jumper is Normally OFF. | LVTTL(3.3 V) |
| H4, H6, H8, H10 | MOD-DEF (1) | Module definition and presence bit (1) Input. Clock for reading/writing to EEPROM. Jumper is Normally OFF. | LVTTL(3.3 V) |
| H4, H6, H8, H10 | MOD-DEF (0) | Module definition and presence bit (0) Output. High without module, Low when module is present. Jumper is Normally ON. | LVTTL(3.3 V) |
| H4, H6, H8, H10 | RATE-SEL | Optional Rate_Select input per SFP MSA definition | Not connected |
| H4, H6, H8, H10 | LOS | Rx Optical Loss of Signal Indicator, Low when a valid optical signal is present, High otherwise. Jumper is Normally ON. | |
| CRSW1/2 | HSIO Switch | HSIO Switch which can be selected to route the SerDes SO0+/– pins either to the SFP TD+/– pins or to the SMA connectors labeled SO0+/– for testing | This switch is determined by soldering a PCB mounted capacitor on one of two pads |
| CRSW3/4 | HSIO Switch | HSIO Switch which can be selected to route the SFP RD+/– pins either to the SerDes SI0+/– pins or to the SMA connectors labeled SI0+/- for testing | This switch is determined by soldering a PCB mounted capacitor on one of two pads |
| CRSW5/6 | HSIO Switch | HSIO Switch which can be selected to route the SerDes SO3+/– pins either to the SFP TD+/– pins or to the SMA connectors labeled SO3+/– for testing | This switch is determined by soldering a PCB mounted capacitor on one of two pads |
| CRSW7/8 | HSIO Switch | HSIO Switch which can be selected to route the SFP RD+/– pins either to the SerDes SI3+/– pins or to the SMA connectors labeled SI3+/- for testing | This switch is determined by soldering a PCB mounted capacitor on one of two pads |
| GR1, GR2, GR3, GR4 | Module Presence Indicators | Green LEDs that indicate the presence of a module in the SFP surface mount connector | Green LED illuminates when module is present |
| RD1, RD3, RD5, RD7 | TX_FAULT Indicators | Red LEDs that indicate the occurrence of an Eye-Safety Condition via the TX_FAULT output pin of the SFP | LEDs are placed left to right in association with the respective SFPs |
| RD2, RD4, RD6, RD8 | LOS Indicators | Red LEDs that indicate the occurrence of a LOS event via the LOS output pin of the SFP. These LEDs illuminate when there is no received signal due to LOS being asserted high | LEDs are placed left to right in association with the the respective SFPs |
| R154 | Chassis Ground | Optional Zero Ohm resistor that connects the PCB chassis ground (e.g., SFP EMI Cage & PCB Mounting holes) to the SFP Signal Ground | SFP Housing and Signal grounds are isolated from one another |

## 3. Summary of Test Results

Significant testing was performed in order to determine compliance to IEEE 802.3 (GBE) specifications of the HFBR-5710L and HDMP-1687 in the reference design. A summary of typical data is demonstrated in *Figures 6* and *s*. The basic test configuration is shown in *Figure 8* in *Appendix A* where it should be noted that the divide by 10 circuit required to provide the transmit byte clock for the SerDes can be obtained by contacting your local Avago field sales office. Also, an additional application note detailing the technical issues with this reference design as well as the comprehensive test results is available.

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*Figure 7* shows the same optical eye diagram from *Figure 6* (top trace) along with the electrical eye diagram of the SerDes SO+ (bottom trace) eye diagram. This was taken with an active probe instead of the SO+ SMA port on the reference board for expediency.

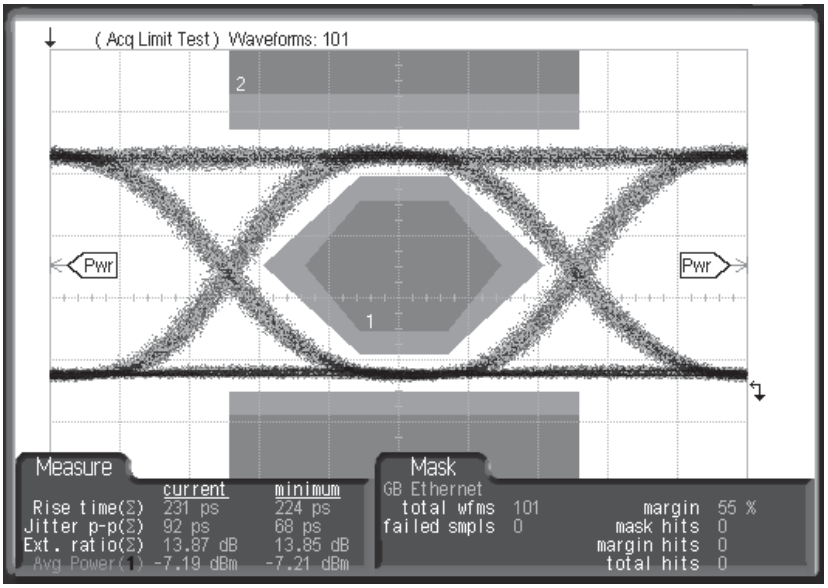



**Figure 6. TPO2 eye diagram with PRBS $2^7$-1 pattern at 1.25 GBd**

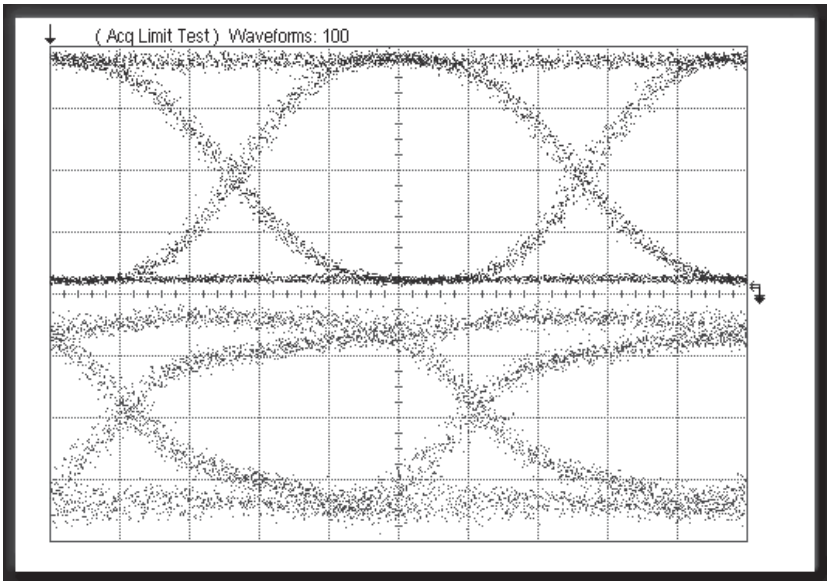



**Figure 7. TPO2 optical eye diagram and SerDes SO+ electrical eye diagram**

## 4. Conclusions and Recommendations

A successful application implementation of a reference design for HFBR-5710L and HDMP-1687 has been demonstrated ensuring interoperability of these components. Detailed testing and application design specifications will be documented in a separate application note. Further the artwork for manufacturing the reference design described herein is available by contacting your local Avago Field Sales Office.

## 5. References


1. Cisco Systems e-Training Materials, Internetworking Technology Overview, June 1999, Chapter 7 "Ethernet Technologies"
   **http://www.cisco.com**
2. Small Form Factor Pluggable (SFP) Multi-Source Agreement
   **http://www.avagotech.com**
3. IEEE 802.3Z
   **http://www.ieee.org**
4. Application Note HFBR-0571
   **http://www.avagotech.com**
5. Application Note 1243 for HFBR-5701L/5710L
   **http://www.avagotech.com**

## Appendix A

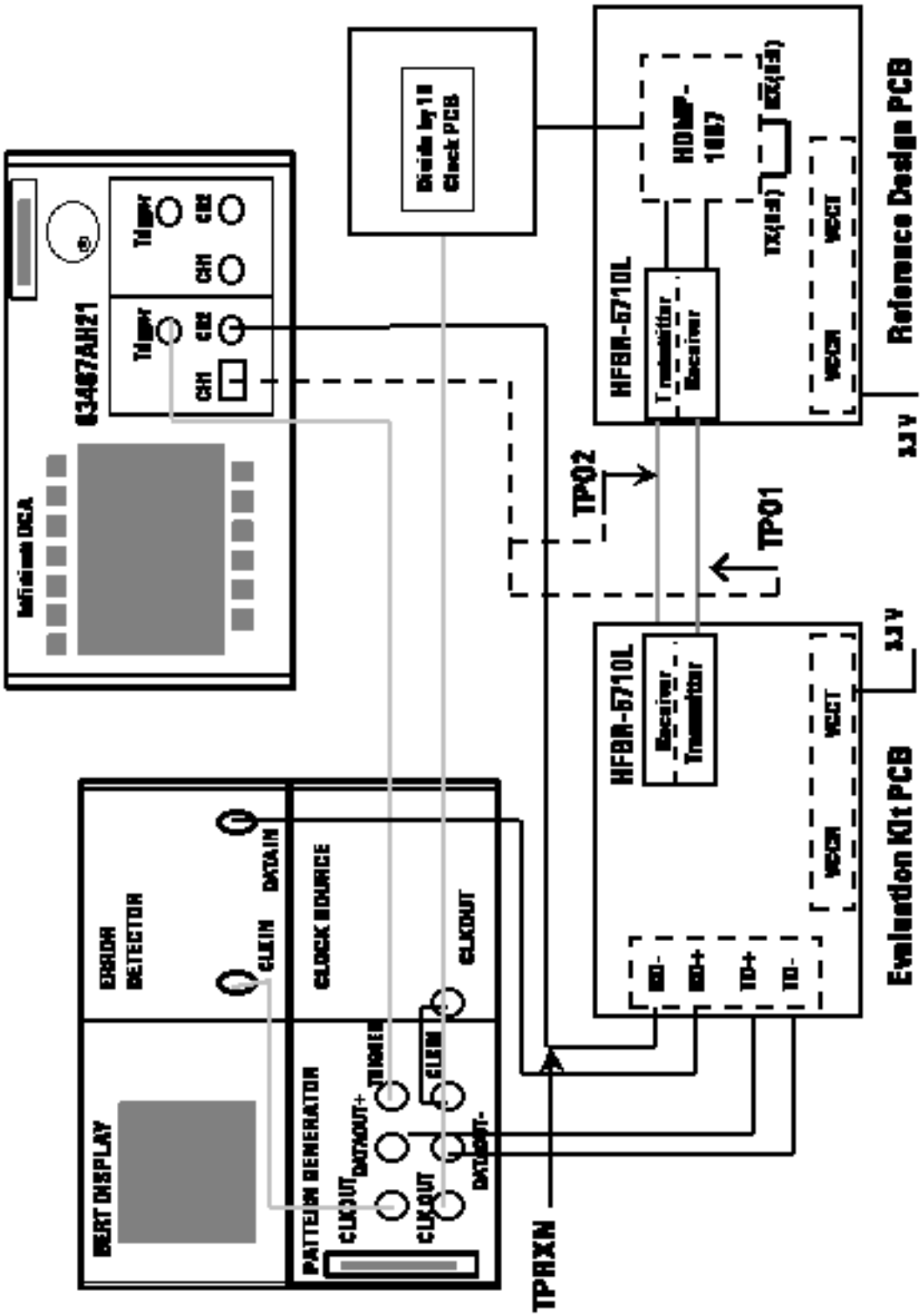
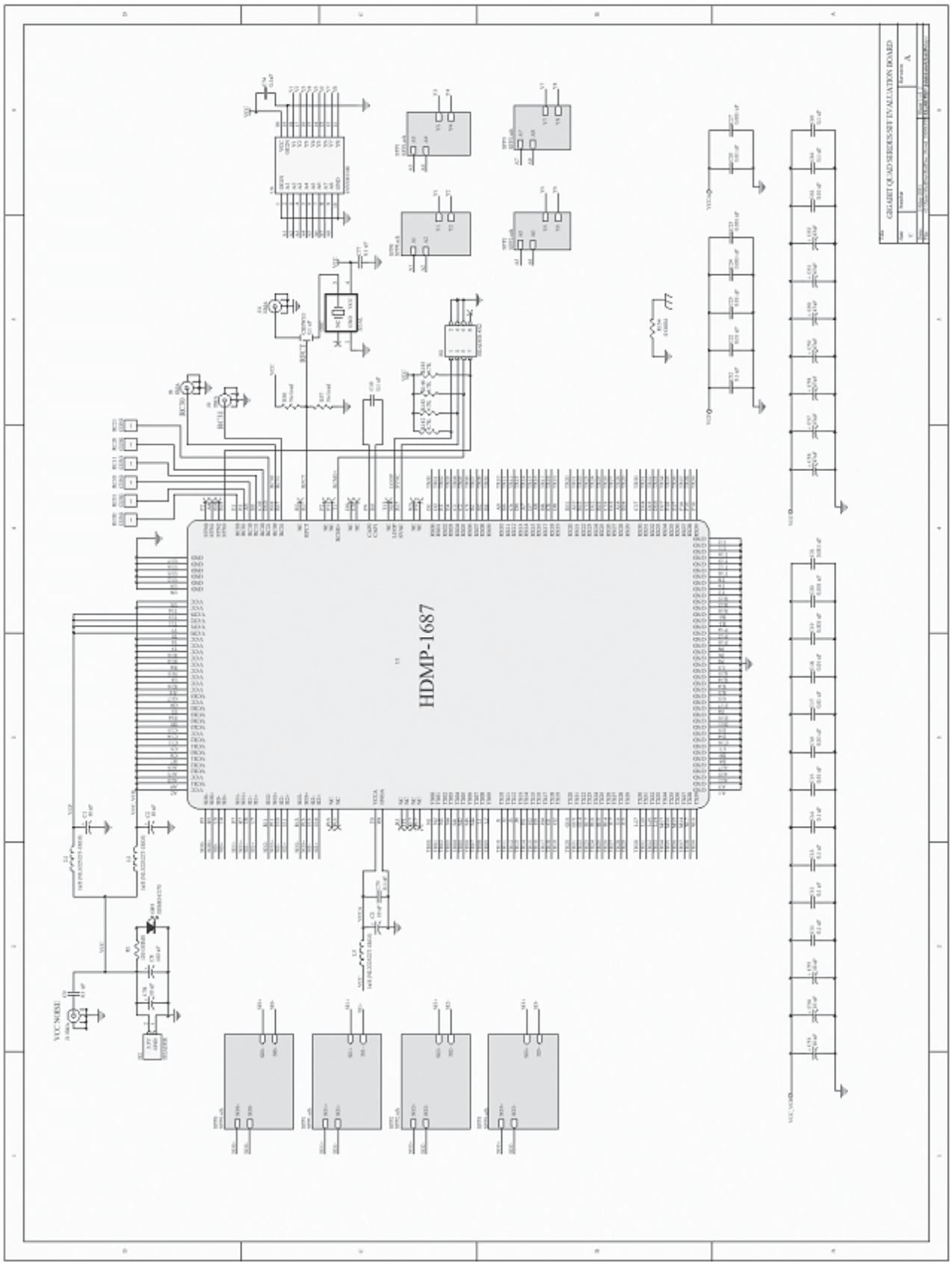



**Figure 8. Test configuration(s) for reference design**

## Appendix B



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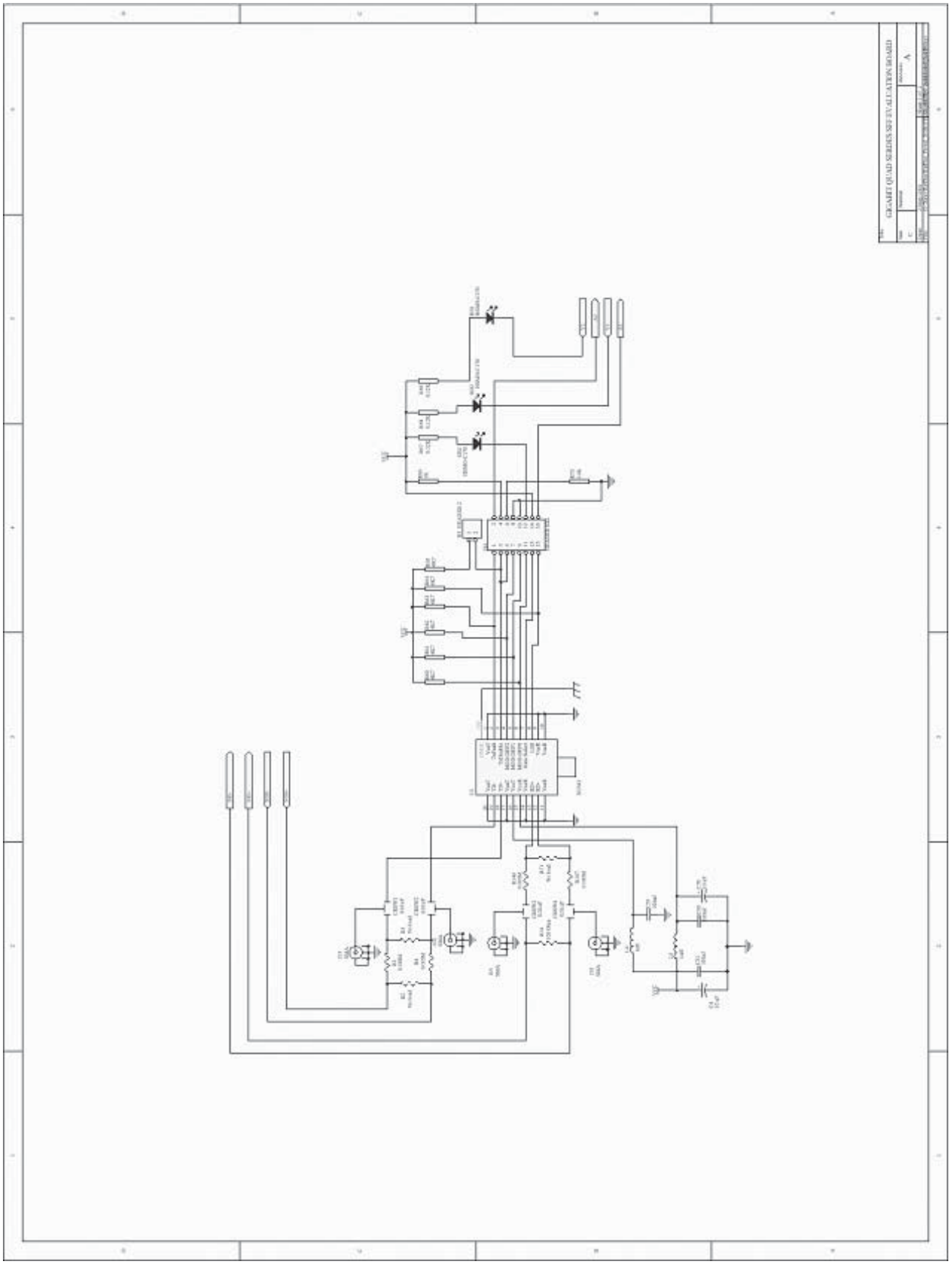

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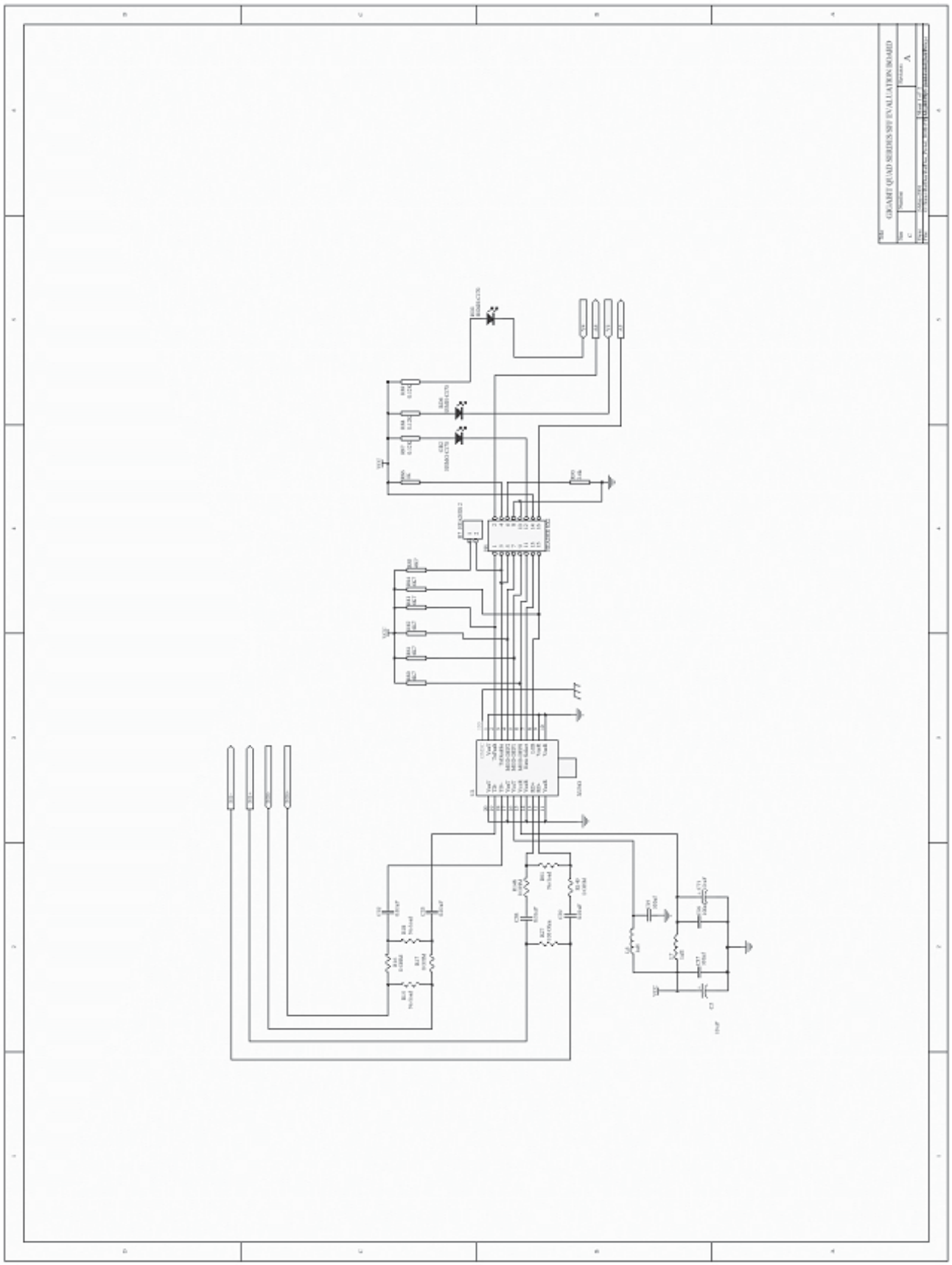

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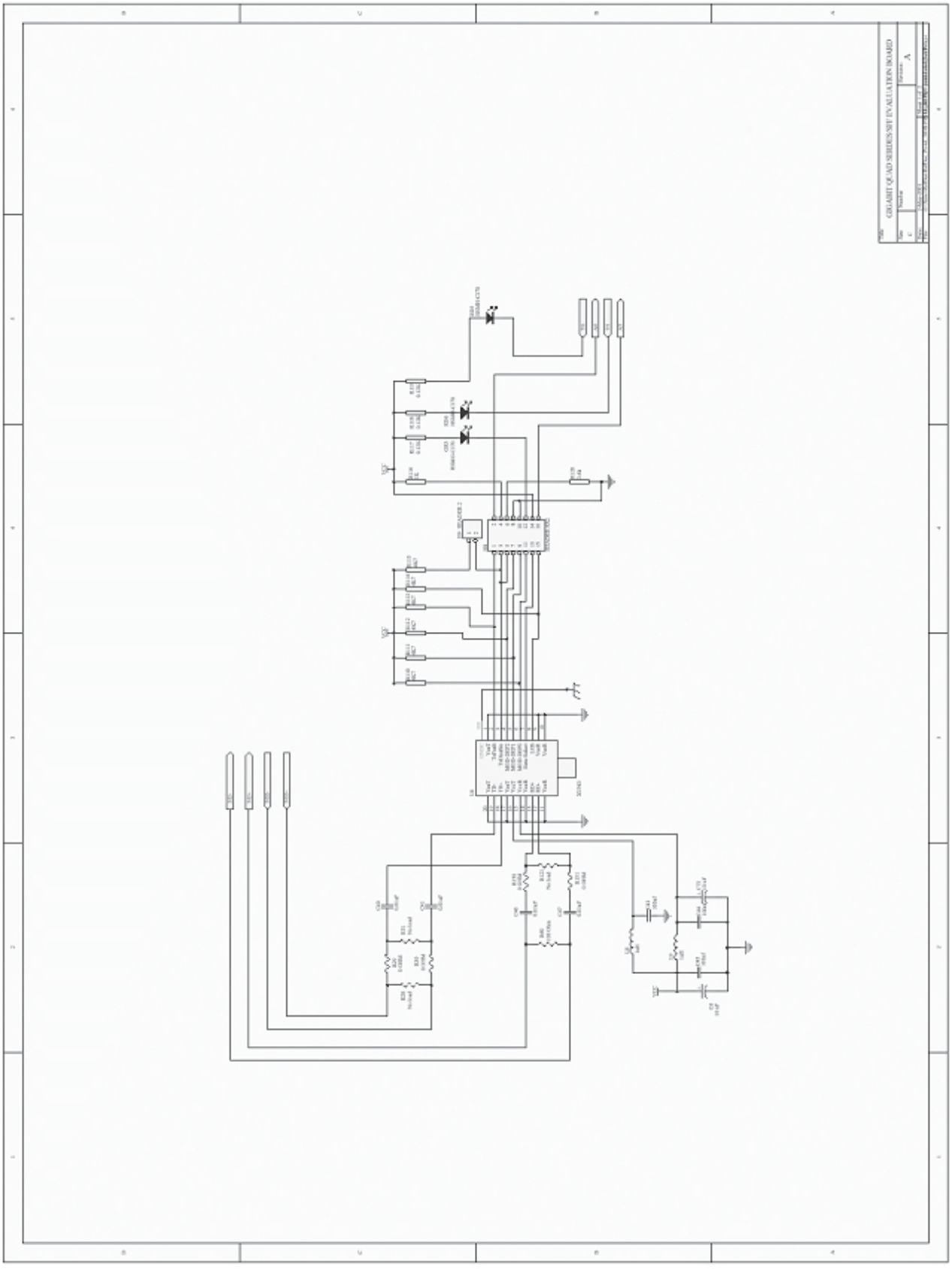

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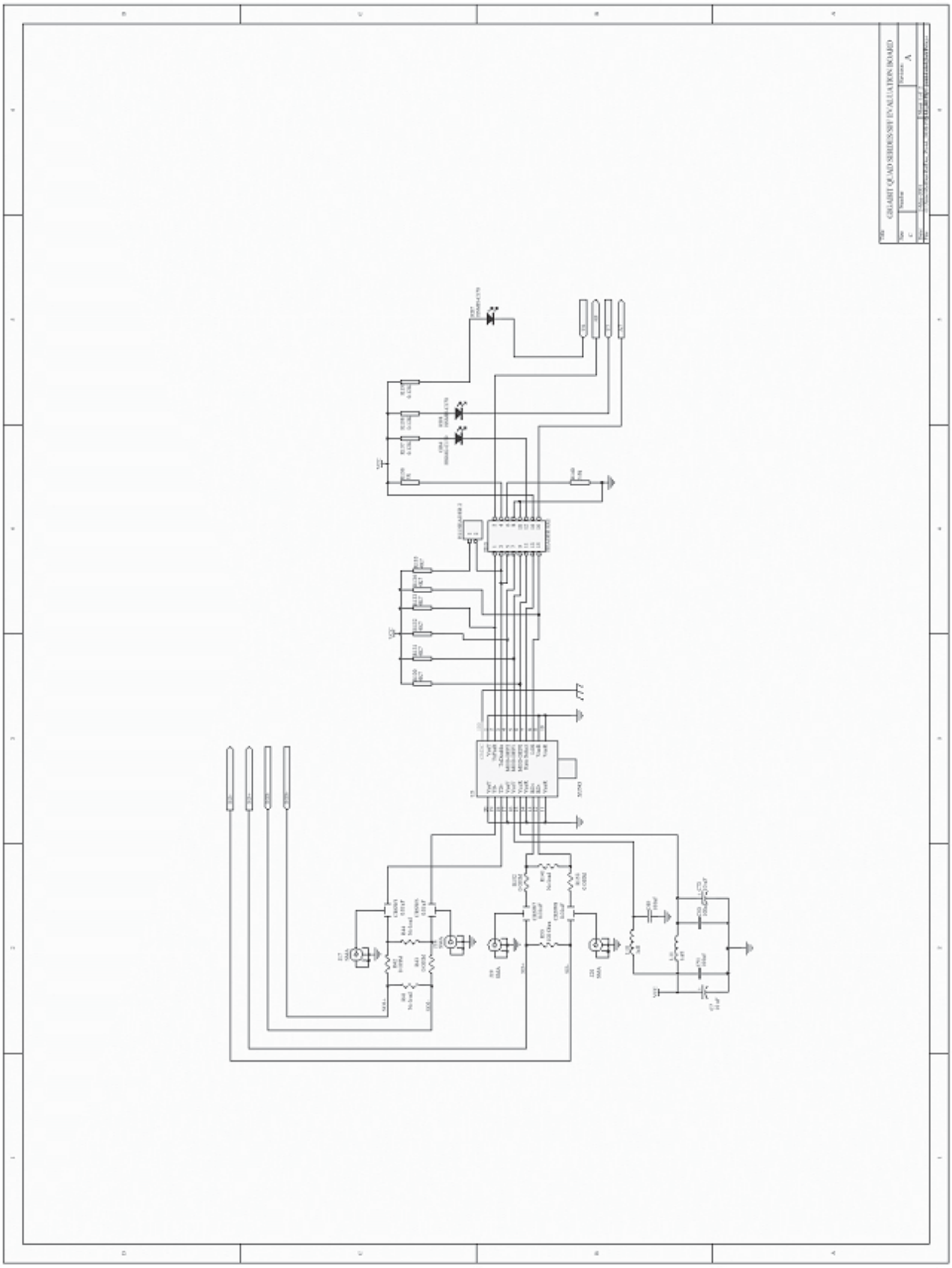

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5988-7286EN April 25, 2007

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