

# R1LV0414D Series

4M SRAM (256-kword × 16-bit)

REJ03C0312-0100

Rev.1.00

May.24.2007

## Description

The R1LV0414D is a 4-Mbit static RAM organized 256-kword × 16-bit, fabricated by Renesas's high-performance 0.15μm CMOS and TFT technologies. R1LV0414D Series has realized higher density, higher performance and low power consumption. The R1LV0414D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 44-pin TSOP II.

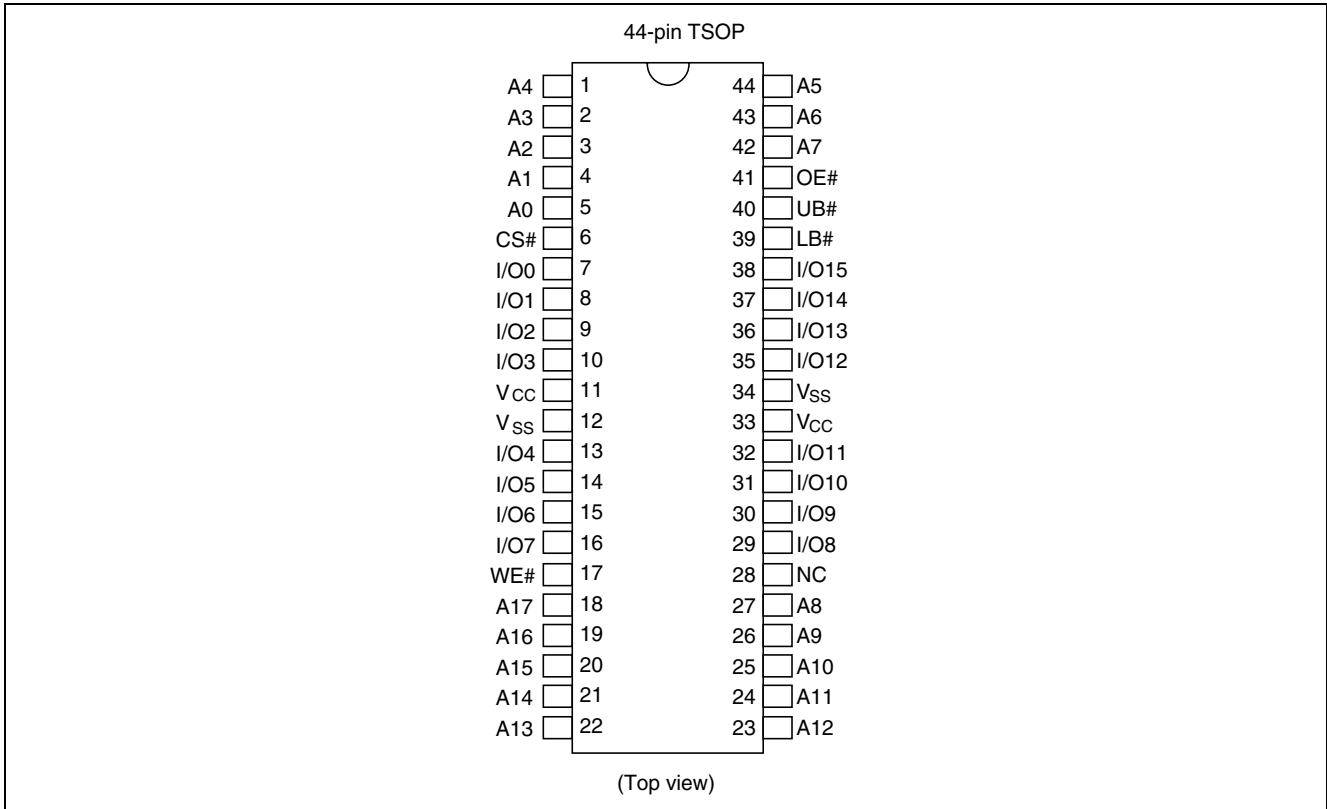
## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
  - Standby: 3 μW (typ) ( $V_{CC} = 3.0$  V)
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
- Temperature range: -40 to +85°C

## Ordering Information

Type No.	Access time	Package
R1LV0414DSB-5SI	55 ns	400-mil 44-pin plastic TSOP II (44P3W-H)
R1LV0414DSB-7LI	70 ns	

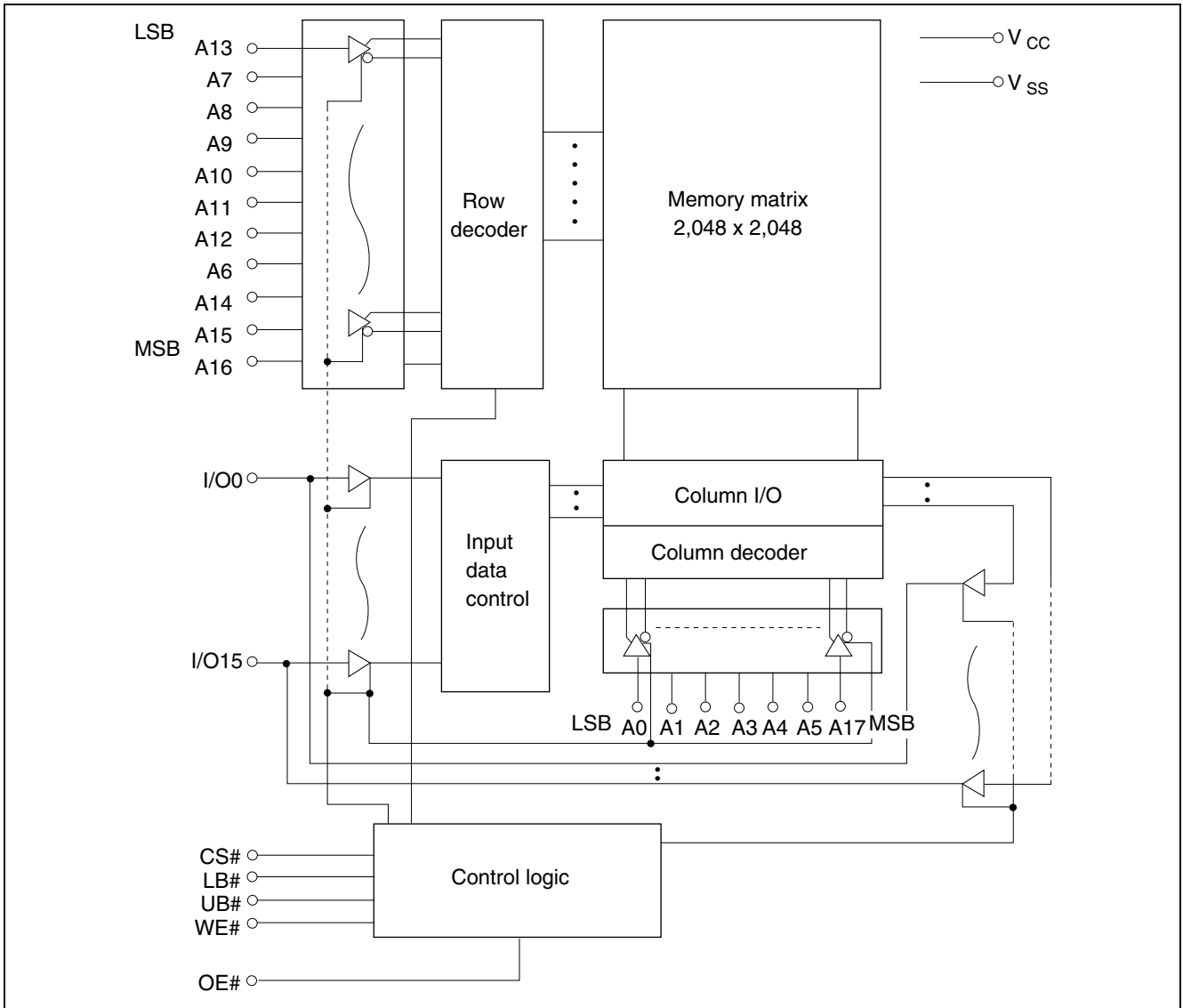
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS# ( $\overline{\text{CS}}$ )	Chip select
OE# ( $\overline{\text{OE}}$ )	Output enable
WE# ( $\overline{\text{WE}}$ )	Write enable
LB# ( $\overline{\text{LB}}$ )	Lower byte select
UB# ( $\overline{\text{UB}}$ )	Upper byte select
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

Block Diagram



## Operation Table

CS#	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
×	×	×	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	×	L	L	Din	Din	Write
L	L	×	H	L	Din	High-Z	Lower byte write
L	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	×	×	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	0.7	W
Operating temperature	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to +150	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq 30$  ns.  
2. Maximum voltage is +4.6 V.

## DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	$T_a$	-40	—	+85	°C	

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq 30$  ns.

## DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current			$ I_{LO} $	—	—	1	$\mu\text{A}$	$CS\# = V_{IH}$ or $OE\# = V_{IH}$ or $WE\# = V_{IL}$ or $LB\# = UB\# = V_{IH}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$
Operating current			$I_{CC}$	—	—	20	$\text{mA}$	$CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0 \text{ mA}$
Average operating current			$I_{CC1}$	—	—	25	$\text{mA}$	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}$ , $CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$
			$I_{CC2}$	—	—	5	$\text{mA}$	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{I/O} = 0 \text{ mA}$ , $CS\# \leq 0.2 \text{ V}$ , $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$
Standby current			$I_{SB}$	—	$0.1^{*1}$	0.3	$\text{mA}$	$CS\# = V_{IH}$
Standby current	-5SI	to +85°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	$V_{in} \geq 0 \text{ V}$ (1) $CS\# \geq V_{CC} - 0.2 \text{ V}$ (2) $LB\# = UB\# \geq V_{CC} - 0.2 \text{ V}$ , $CS\# \leq 0.2 \text{ V}$ Average values
		to +70°C	$I_{SB1}$	—	—	8	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	3	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	$1^{*1}$	2.5	$\mu\text{A}$	
	-7LI	to +85°C	$I_{SB1}$	—	—	20	$\mu\text{A}$	
		to +70°C	$I_{SB1}$	—	—	16	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	$1^{*1}$	10	$\mu\text{A}$	
Output high voltage			$V_{OH}$	2.4	—	—	$\text{V}$	$I_{OH} = -1 \text{ mA}$
			$V_{OH2}$	$V_{CC} - 0.2$	—	—	—	$\text{V}$
Output low voltage			$V_{OL}$	—	—	0.4	$\text{V}$	$I_{OL} = 2 \text{ mA}$
			$V_{OL2}$	—	—	0.2	$\text{V}$	$I_{OL} = 100 \mu\text{A}$

Notes: 1. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0 \text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	$\text{pF}$	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	$\text{pF}$	$V_{I/O} = 0 \text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

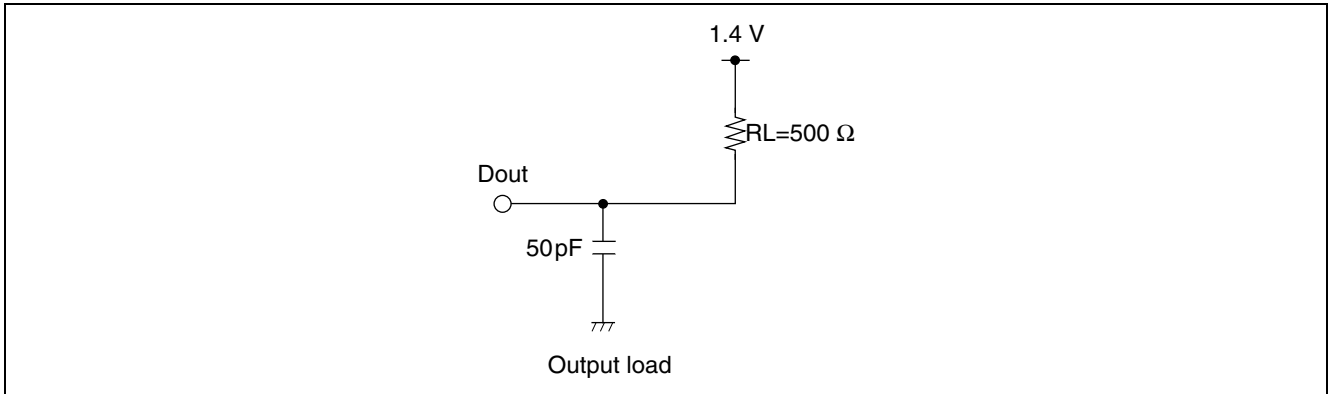
( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns

Input/output timing reference levels: 1.4 V

- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	R1LV0414D				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	55	—	70	—	ns	
Address access time	$t_{AA}$	—	55	—	70	ns	
Chip select access time	$t_{ACS}$	—	55	—	70	ns	
Output enable to output valid	$t_{OE}$	—	35	—	40	ns	
Output hold from address change	$t_{OH}$	10	—	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	55	—	70	ns	
Chip select to output in low-Z	$t_{CLZ}$	10	—	10	—	ns	2, 3
LB#, UB# disable to low-Z	$t_{BLZ}$	5	—	5	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	$t_{CHZ}$	0	20	0	25	ns	1, 2, 3
LB#, UB# disable to high-Z	$t_{BHZ}$	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 3

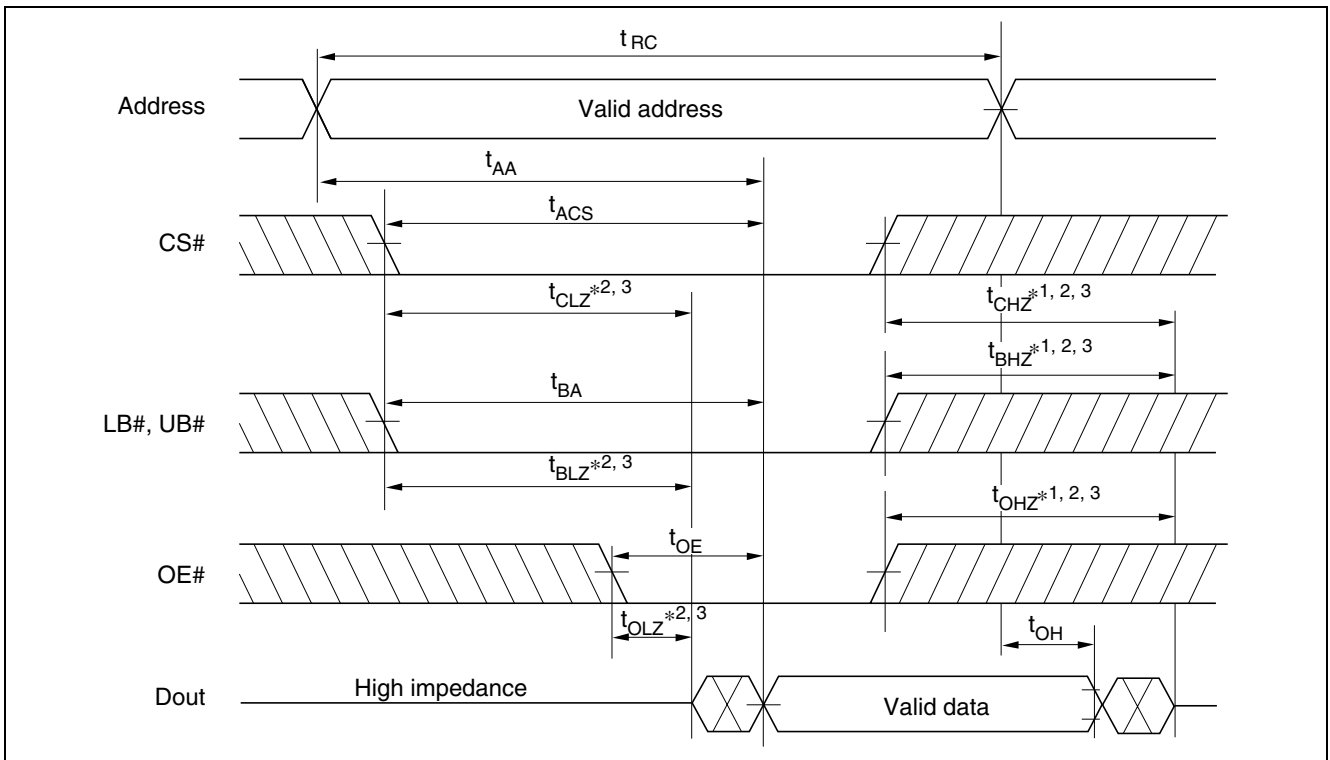
## Write Cycle

Parameter	Symbol	R1LV0414D				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	ns	
Address valid to end of write	$t_{AW}$	50	—	60	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	ns	5
Write pulse width	$t_{WP}$	40	—	50	—	ns	4
LB#, UB# valid to end of write	$t_{BW}$	50	—	55	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	30	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 3
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1, 2

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from CS# going low to the end of write.
  6.  $t_{AS}$  is measured from the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earlier of CS# or WE# going high to the end of write cycle.

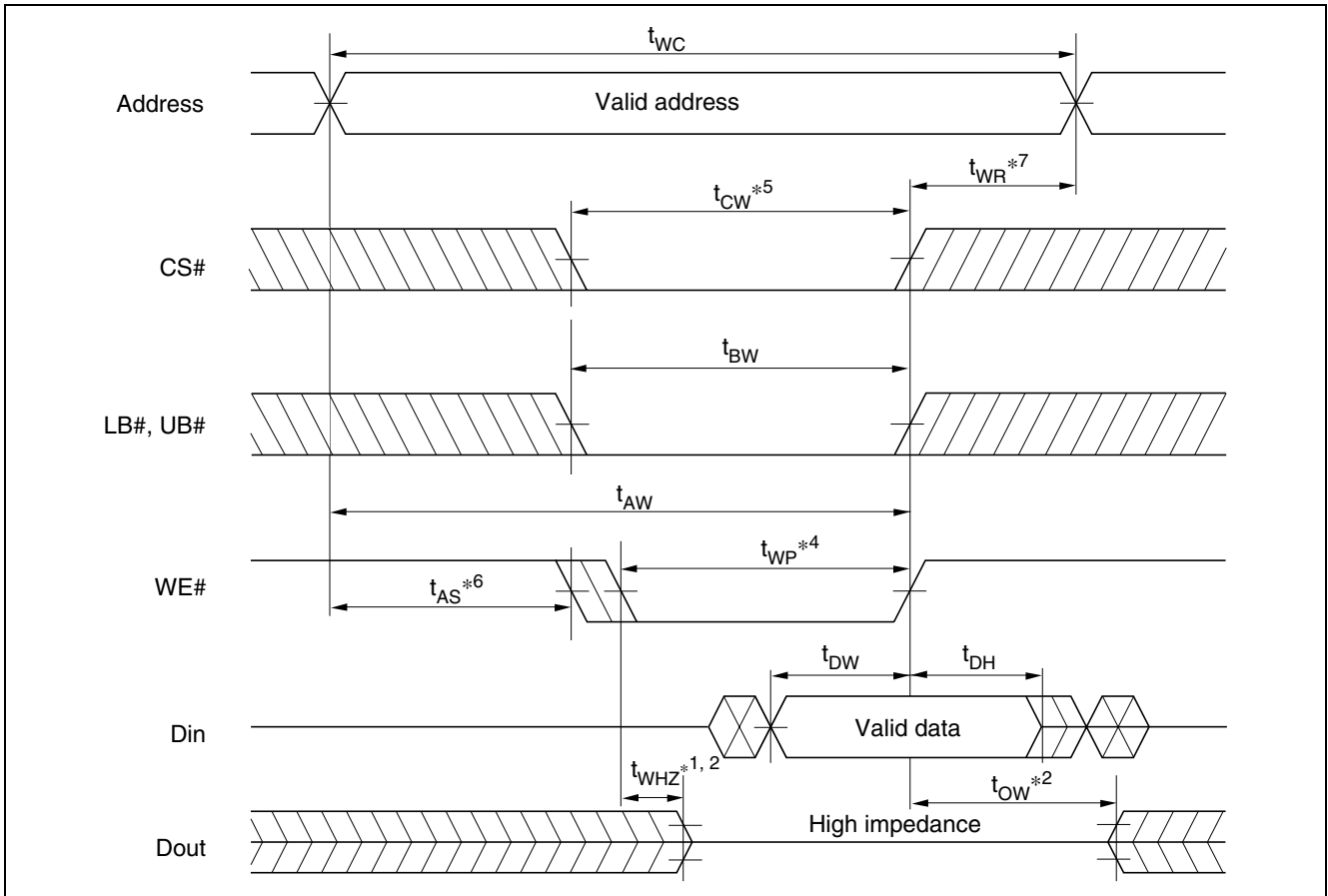
## Timing Waveform

Read Timing Waveform (WE# = V<sub>IH</sub>)

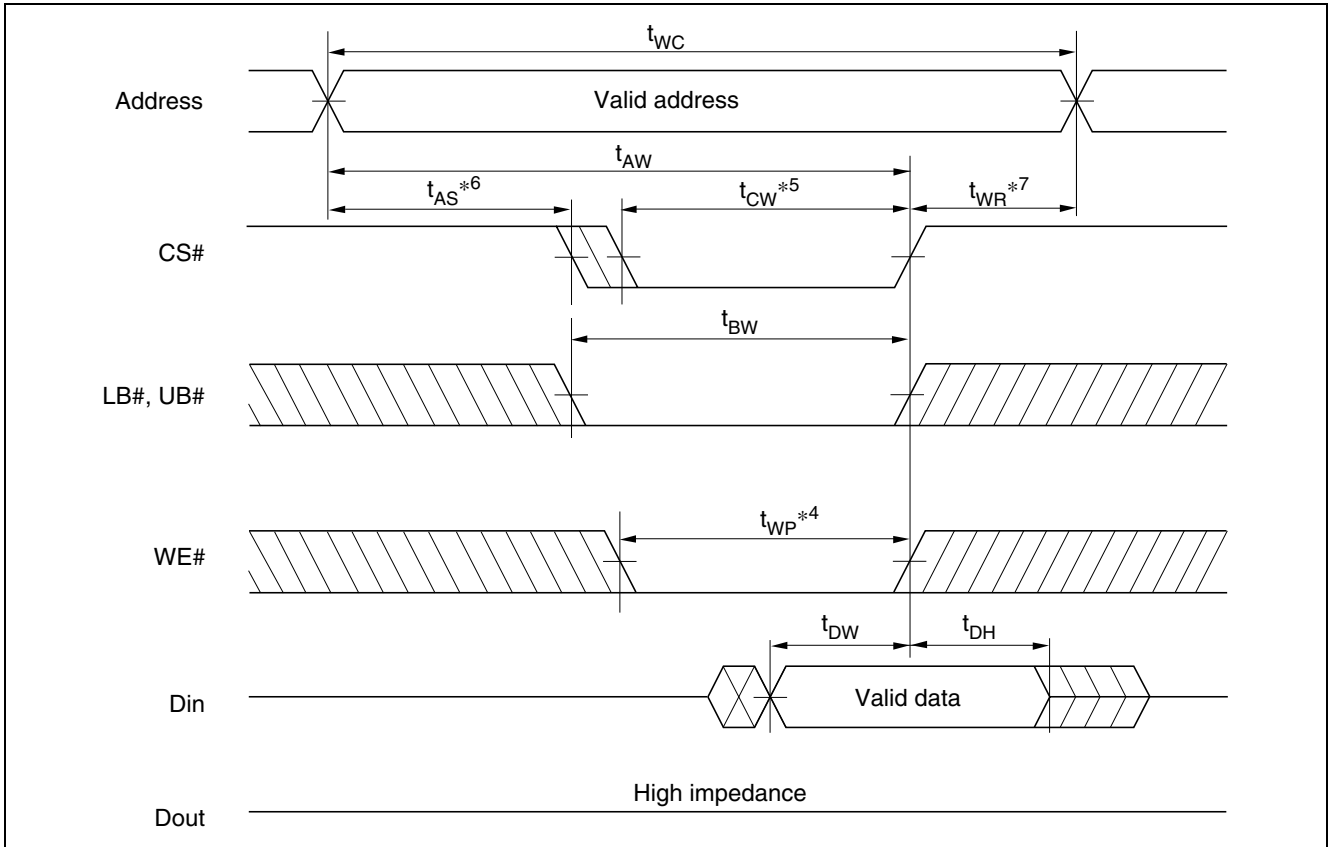




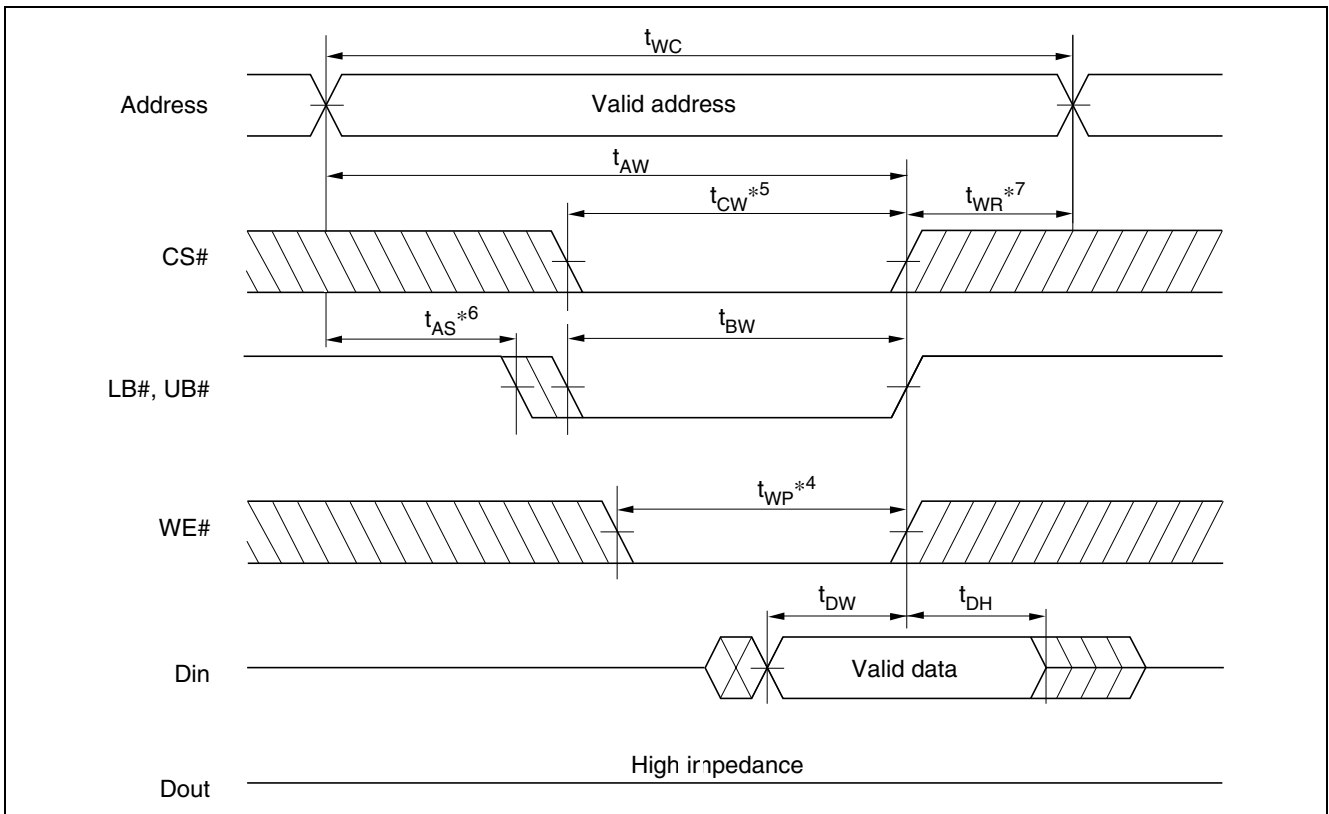
Write Timing Waveform (1) (WE# Clock)



Write Timing Waveform (2) (CS# Clock, OE# = V<sub>IH</sub>)



Write Timing Waveform (3) (LB#, UB# Clock, OE# = V<sub>IH</sub>)



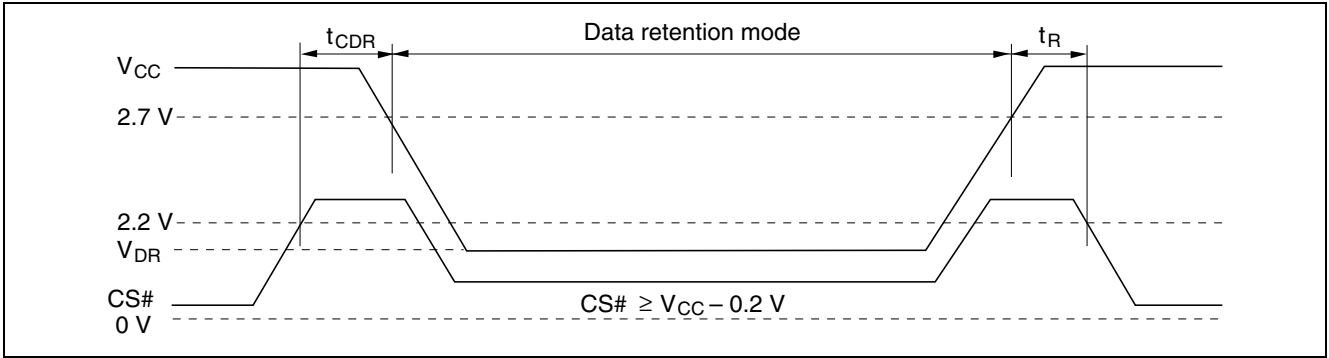
Low  $V_{CC}$  Data Retention Characteristics

(Ta = -40 to +85°C)

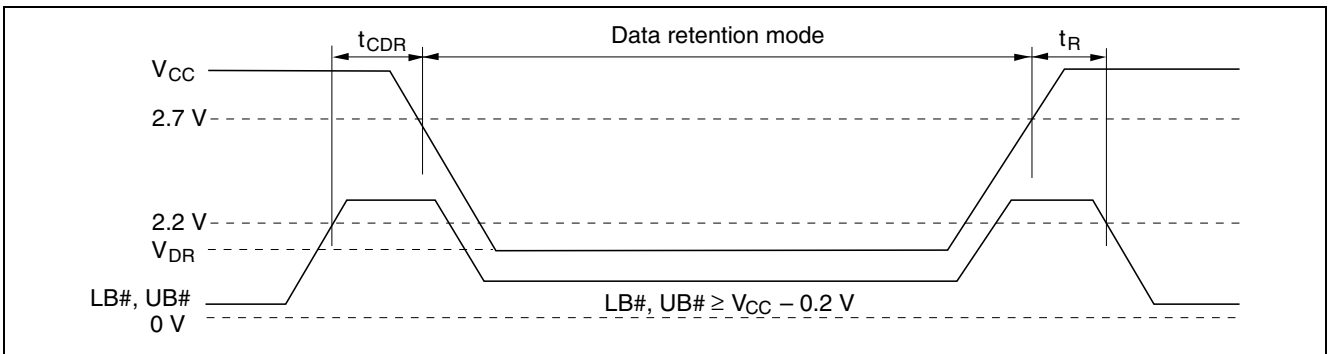
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
$V_{CC}$ for data retention		$V_{DR}$	2	—	—	V	$V_{in} \geq 0V$ (1) $CS\# \geq V_{CC} - 0.2V$ or (2) $LB\# = UB\# \geq V_{CC} - 0.2V$ , $CS\# \leq 0.2V$	
Data retention current	-5SI	to +85°C	$I_{CCDR}$	—	—	10	$\mu A$	$V_{CC} = 3.0V$ , $V_{in} \geq 0V$ (1) $CS\# \geq V_{CC} - 0.2V$ or (2) $LB\# = UB\# \geq V_{CC} - 0.2V$ , $CS\# \leq 0.2V$ Average values
		to +70°C	$I_{CCDR}$	—	—	8	$\mu A$	
		to +40°C	$I_{CCDR}$	—	—	3	$\mu A$	
		to +25°C	$I_{CCDR}$	—	1* <sup>1</sup>	2.5	$\mu A$	
	-7LI	to +85°C	$I_{CCDR}$	—	—	20	$\mu A$	
		to +70°C	$I_{CCDR}$	—	—	16	$\mu A$	
		to +40°C	$I_{CCDR}$	—	—	10	$\mu A$	
		to +25°C	$I_{CCDR}$	—	1* <sup>1</sup>	10	$\mu A$	
Chip deselect to data retention time		$t_{CDR}$	0	—	—	ns	See retention waveform	
Operation recovery time		$t_R$	5	—	—	ms		

Note: 1. Typical values are at  $V_{CC} = 3.0V$ ,  $T_a = +25^\circ C$  and specified loading, and not guaranteed.

Low  $V_{CC}$  Data Retention Timing Waveform (1) (CS# Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) (LB#, UB# Controlled)



## Revision History

## R1LV0414D Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Dec. 25, 2006	—	Initial issue
1.00	May. 24, 2007	2	Ordering Information R1LV0414DSB-5S% to R1LV0414DSB-5SI R1LV0414DSB-7L% to R1LV0414DSB-7LI
		2	Pin Arrangement A6 to A13, A13 to A6
		3	Change of Block Diagram
		4	Absolute Maximum Ratings: Deletion of R ver. specification
		4	DC Operating Conditions: Deletion of R ver. specification
		5	DC Characteristics $I_{SB1}$ (-5SI) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A
		6	AC Characteristics: Change of Test Conditions
		11	Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ (-5SI) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A Deletion of note 2

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