Octal, 12-Bit, 40/50/65 MSPS Serial LVDS 1.8 V A/D Converter

AD9222

FEATURES

8 ADCs integrated into 1 package
114 mW ADC power per channel at 65 MSPS
SNR = 70 dB (to Nyquist)
ENOB = 11.3 bits
SFDR = 80 dBc
Excellent linearity: DNL = ±0.3 LSB (typical),
INL = ±0.4 LSB (typical)
Serial LVDS (ANSI-644, default)
Low power, reduced signal option (similar IEEE 1596.3)
Data and frame clock outputs
325 MHz full-power analog bandwidth
2 V p-p input voltage range
1.8 V supply operation
Serial port control
Full-chip and individual-channel power-down modes
Flexible bit orientation
Built-in and custom digital test pattern generation
Programmable clock and data alignment
Programmable output resolution
Standby mode

APPLICATIONS

Medical imaging and nondestructive ultrasound
Portable ultrasound and digital beam-forming systems
Quadrature radio receivers
Diversity radio receivers
Tape drives
Optical networking
Test equipment

GENERAL DESCRIPTION

The AD9222 is an octal, 12-bit, 40/50/65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 65 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9222 is available in an RoHS compliant, 64-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

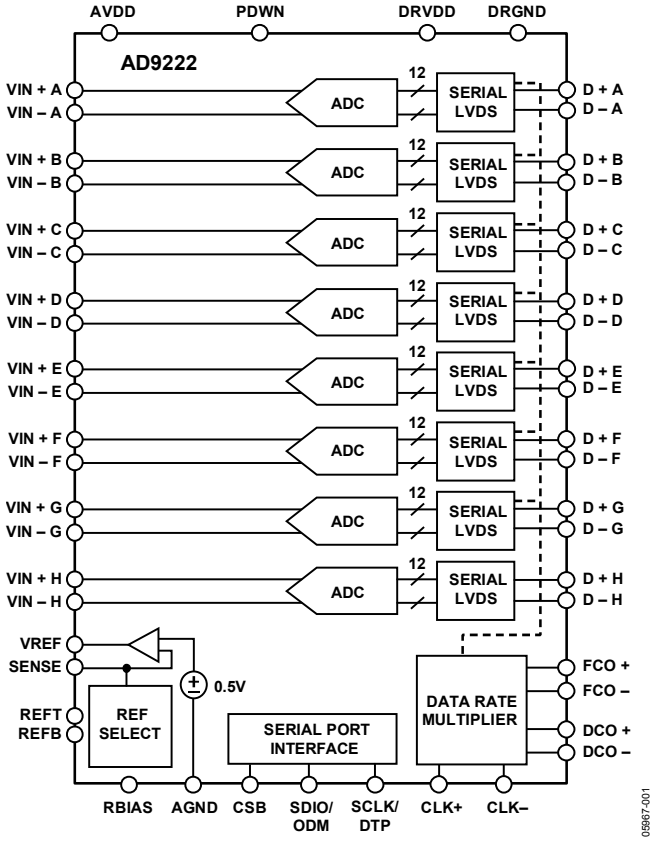

Figure 1.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small, space-saving package.
2. Low power of 114 mW/channel at 65 MSPS.
3. Ease of Use. A data clock output (DCO) is provided that operates at frequencies of up to 390 MHz and supports double data rate (DDR) operation.
4. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible Family. This includes the AD9212 (10-bit) and AD9252 (14-bit).

Rev. C

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SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 1.

		AD9222-40			AD9222-50			AD9222-65			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			12			12			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±1	±8		±1	±8		±1	±8	mV
Offset Matching	Full		±3	±8		±3	±8		±3	±8	mV
Gain Error	Full		±0.4	±1.2		±1.5	±2.5		±3.5	±5	% FS
Gain Matching	Full		±0.3	±0.7		±0.3	±0.7		±0.4	±0.8	% FS
Differential Nonlinearity (DNL)	Full		±0.25	±0.5		±0.3	±0.65		±0.25	±0.6	LSB
Integral Nonlinearity (INL)	Full		±0.4	±1		±0.4	±1		±0.4	±1	LSB
TEMPERATURE DRIFT											
Offset Error	Full		±2			±2			±2		ppm/°C
Gain Error	Full		±17			±17			±17		ppm/°C
Reference Voltage (1 V Mode)	Full		±21			±21			±21		ppm/°C
REFERENCE											
Output Voltage Error (VREF = 1 V)	Full		±2	±30		±2	±30		±2	±30	mV
Load Regulation @ 1.0 mA (VREF = 1 V)	Full		3			3			3		mV
Input Resistance	Full		6			6			6		kΩ
ANALOG INPUTS											
Differential Input Voltage Range (VREF = 1 V)	Full		2			2			2		V p-p
Common-Mode Voltage	Full		AVDD/2			AVDD/2			AVDD/2		V
Differential Input Capacitance	Full		7			7			7		pF
Analog Bandwidth, Full Power	Full		325			325			325		MHz
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
IAVDD	Full		338	348.5		357.5	367.5		450	470	mA
IDRVDD	Full		51	53.6		53.5	56.2		56.6	60.5	mA
Total Power Dissipation (Including Output Drivers)	Full		700	722		740	760		910	950.5	mW
Power-Down Dissipation	Full		2	11		2	11		2	11	mW
Standby Dissipation[2]	Full		83			89			100		mW
CROSSTALK	Full		−90			−90			−90		dB
CROSSTALK (Overrange Condition)[3]	Full		−90			−90			−90		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This can be controlled via SPI.
[3] Overrange condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 2.

		AD9222-40			AD9222-50			AD9222-65			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 2.4 MHz	Full		70.3			70.4			70.3		dB
f_{IN} = 19.7 MHz	Full	69.5	70.3		69.5	70.3		68.5	70.0		dB
f_{IN} = 35 MHz	Full		69.9			70.0			69.8		dB
f_{IN} = 70 MHz	Full		68.8			69.0			69.5		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)											
f_{IN} = 2.4 MHz	Full		70.0			70.0			69.5		dB
f_{IN} = 19.7 MHz	Full	68.7	70.0		68.5	70.0		66.8	69.4		dB
f_{IN} = 35 MHz	Full		69.5			69.8			69.3		dB
f_{IN} = 70 MHz	Full		68.0			68.5			69		dB
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 2.4 MHz	Full		11.38			11.4			11.4		Bits
f_{IN} = 19.7 MHz	Full	11.25	11.38		11.25	11.38		11.1	11.34		Bits
f_{IN} = 35 MHz	Full		11.32			11.33			11.30		Bits
f_{IN} = 70 MHz	Full		11.14			11.17			11.25		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 2.4 MHz	Full		85			85			83		dBc
f_{IN} = 19.7 MHz	Full	73	85		73	84		70.5	80		dBc
f_{IN} = 35 MHz	Full		80			83			80		dBc
f_{IN} = 70 MHz	Full		76			77			75		dBc
WORST HARMONIC (Second or Third)											
f_{IN} = 2.4 MHz	Full		−85			−85			−83		dBc
f_{IN} = 19.7 MHz	Full		−85	−74		−84	−73		−80	−70.5	dBc
f_{IN} = 35 MHz	Full		−80			−83			−80		dBc
f_{IN} = 70 MHz	Full		−76			−77			−75		dBc
WORST OTHER (Excluding Second or Third)											
f_{IN} = 2.4 MHz	Full		−92			−92			−90		dBc
f_{IN} = 19.7 MHz	Full		−92	−80		−92	−80		−90	−80	dBc
f_{IN} = 35 MHz	Full		−92			−92			−90		dBc
f_{IN} = 70 MHz	Full		−90			−90			−85		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS											
f_{IN1} = 15 MHz, f_{IN2} = 16 MHz	25°C		80.0			80.0			80.0		dBc
f_{IN1} = 70 MHz, f_{IN2} = 71 MHz	25°C		77.0			77.0			75.0		dBc

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 3.

		AD9222-40			AD9222-50			AD9222-65			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK−)											
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			250			250			mV p-p
Input Common-Mode Voltage	Full		1.2			1.2			1.2		V
Input Resistance (Differential)	25°C		20			20			20		kΩ
Input Capacitance	25°C		1.5			1.5			1.5		pF
LOGIC INPUTS (PDWN, SCLK/DTP)											
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3			0.3	V
Input Resistance	25°C		30			30			30		kΩ
Input Capacitance	25°C		0.5			0.5			0.5		pF
LOGIC INPUT (CSB)											
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3			0.3	V
Input Resistance	25°C		70			70			70		kΩ
Input Capacitance	25°C		0.5			0.5			0.5		pF
LOGIC INPUT (SDIO/ODM)											
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	1.2		DRVDD + 0.3	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	0		0.3	0		0.3	V
Input Resistance	25°C		30			30			30		kΩ
Input Capacitance	25°C		2			2			2		pF
LOGIC OUTPUT (SDIO/ODM)[3]											
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79			1.79			1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05			0.05			0.05	V
DIGITAL OUTPUTS (D + x, D − x), (ANSI-644)[1]											
Logic Compliance			LVDS			LVDS			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	247		454	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	1.125		1.375	1.125		1.375	V
Output Coding (Default)			Offset binary			Offset binary			Offset binary		
DIGITAL OUTPUTS (D + x, D − x), (Low Power, Reduced Signal Option)[1]											
Logic Compliance			LVDS			LVDS			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	150		250	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	1.10		1.30	1.10		1.30	V
Output Coding (Default)			Offset binary			Offset binary			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 4.

		AD9222-40			AD9222-50			AD9222-65			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK[2]											
Maximum Clock Rate	Full	40			50			65			MSPS
Minimum Clock Rate	Full			10			10			10	MSPS
Clock Pulse Width High (t_{EH})	Full		12.5			10.0			7.5		ns
Clock Pulse Width Low (t_{EL})	Full		12.5			10.0			7.5		ns
OUTPUT PARAMETERS[2, 3]											
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	1.5	2.3	3.1	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300			300			300		ps
Fall Time (t_F) (20% to 80%)	Full		300			300			300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	1.5	2.3	3.1	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)			t_{FCO} + (t_{SAMPLE}/24)			t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200		±50	±200		±50	±200	ps
Wake-Up Time (Standby)	25°C		600			600			600		ns
Wake-Up Time (Power-Down)	25°C		375			375			375		µs
Pipeline Latency	Full		8			8			8		CLK cycles
APERTURE											
Aperture Delay (t_A)	25°C		750			750			750		ps
Aperture Uncertainty (Jitter)	25°C		<1			<1			<1		ps rms
Out-of-Range Recovery Time	25°C		1			1			1		CLK cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.

TIMING DIAGRAMS

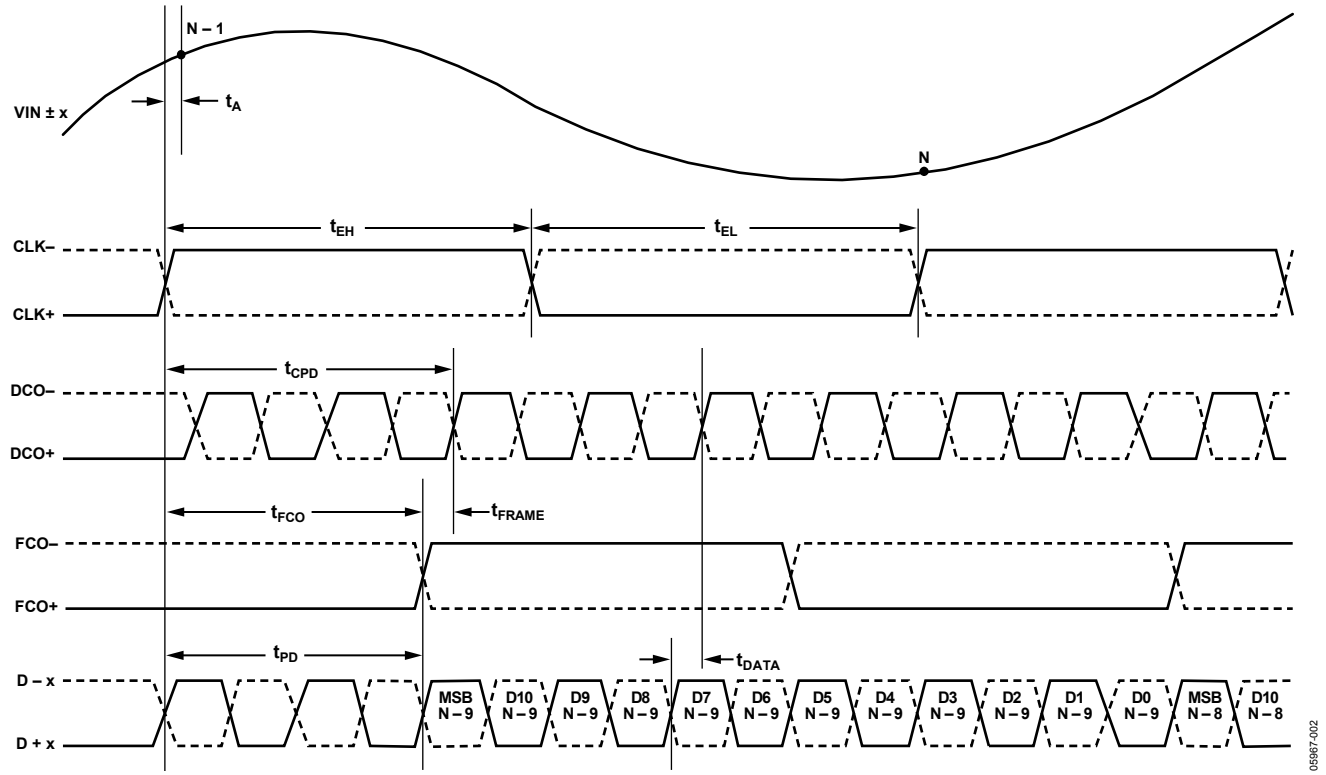

Figure 2. 12-Bit Data Serial Stream, MSB First (Default)

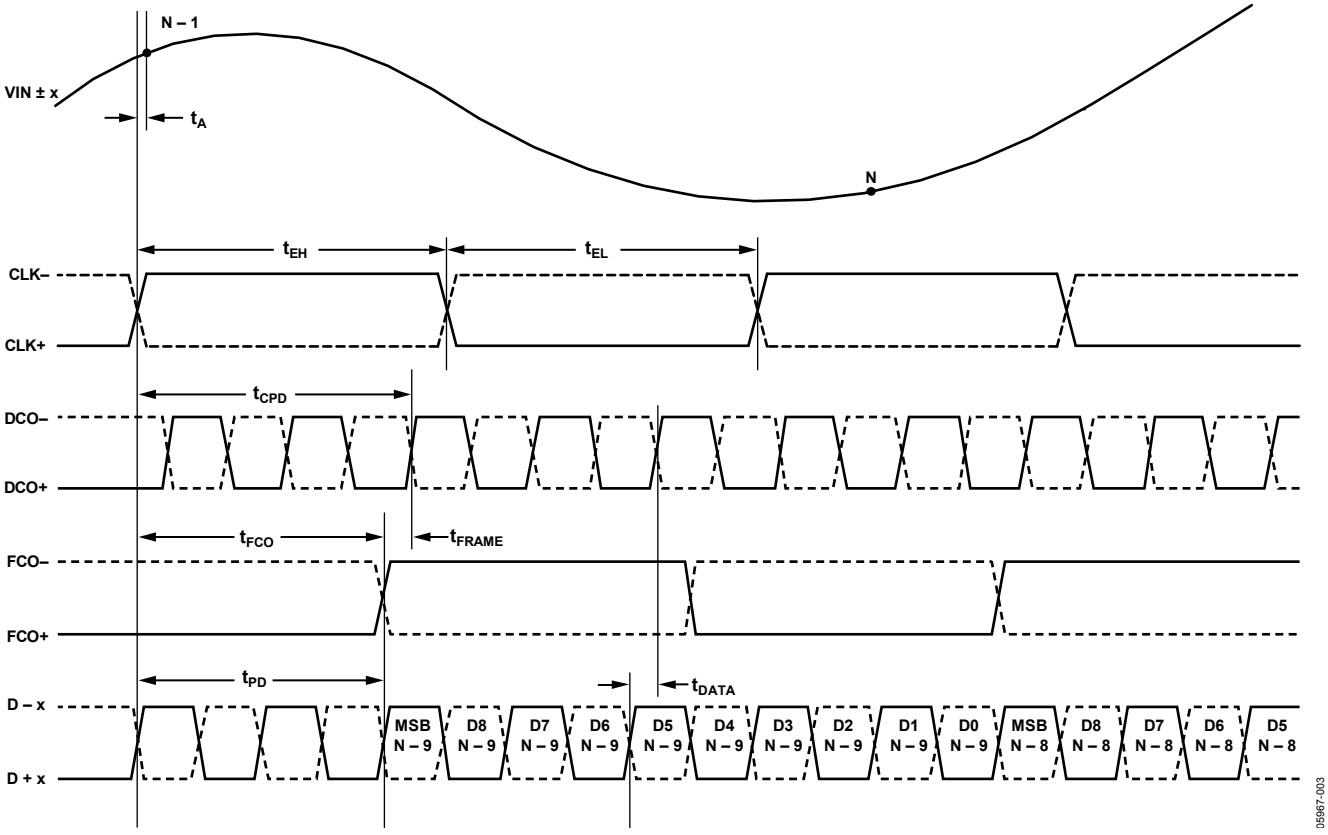

Figure 3. 10-Bit Data Serial Stream, MSB First

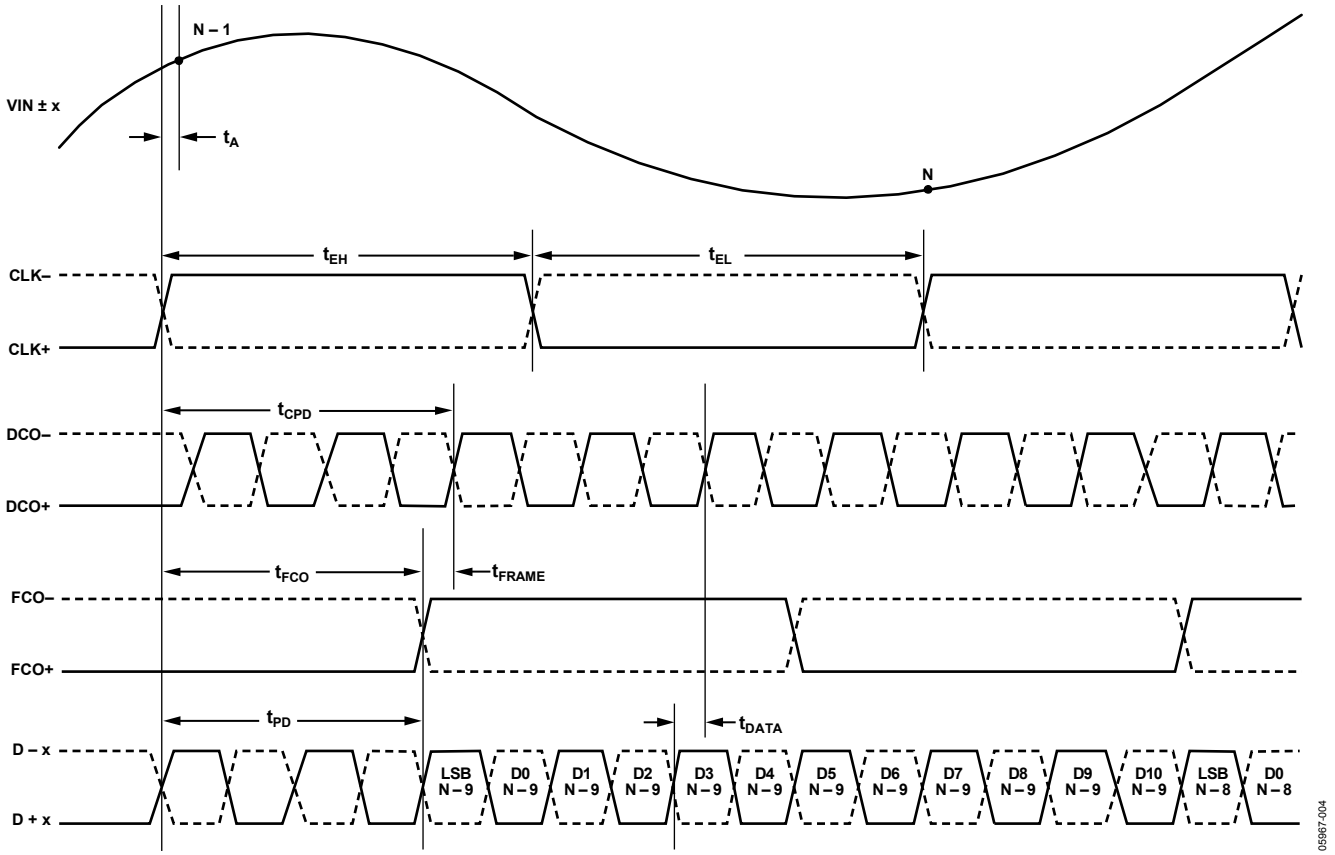

Figure 4. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	AGND	−0.3 V to +2.0 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD	DRVDD	−2.0 V to +2.0 V
Digital Outputs (D + x, D − x, DCO+, DCO−, FCO+, FCO−)	DRGND	−0.3 V to +2.0 V
CLK+, CLK−	AGND	−0.3 V to +3.9 V
VIN + x, VIN − x	AGND	−0.3 V to +2.0 V
SDIO/ODM	AGND	−0.3 V to +2.0 V
PDWN, SCLK/DTP, CSB	AGND	−0.3 V to +3.9 V
REFT, REFB, RBIAS	AGND	−0.3 V to +2.0 V
VREF, SENSE	AGND	−0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		−40°C to +85°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/s)	θ_{JA}[1]	θ_{JB}	θ_{JC}
0.0	17.7°C/W		
1.0	15.5°C/W	8.7°C/W	0.6°C/W
2.5	13.9°C/W		

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

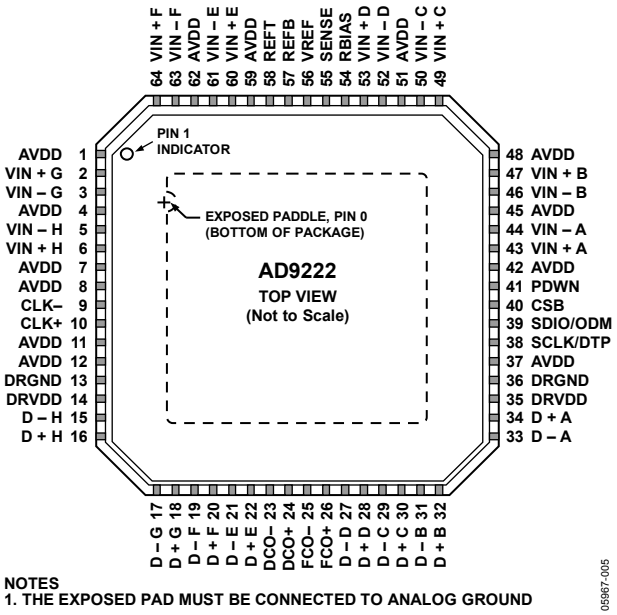

Figure 5. 64-Lead LFCSP Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle)
1, 4, 7, 8, 11, 12, 37, 42, 45, 48, 51, 59, 62	AVDD	1.8 V Analog Supply
13, 36	DRGND	Digital Output Driver Ground
14, 35	DRVDD	1.8 V Digital Output Driver Supply
2	VIN + G	ADC G Analog Input True
3	VIN – G	ADC G Analog Input Complement
5	VIN – H	ADC H Analog Input Complement
6	VIN + H	ADC H Analog Input True
9	CLK–	Input Clock Complement
10	CLK+	Input Clock True
15	D – H	ADC H Digital Output Complement
16	D + H	ADC H Digital Output True
17	D – G	ADC G Digital Output Complement
18	D + G	ADC G Digital Output True
19	D – F	ADC F Digital Output Complement
20	D + F	ADC F Digital Output True
21	D – E	ADC E Digital Output Complement
22	D + E	ADC E Digital Output True
23	DCO–	Data Clock Digital Output Complement
24	DCO+	Data Clock Digital Output True
25	FCO–	Frame Clock Digital Output Complement
26	FCO+	Frame Clock Digital Output True
27	D – D	ADC D Digital Output Complement
28	D + D	ADC D Digital Output True
29	D – C	ADC C Digital Output Complement
30	D + C	ADC C Digital Output True
31	D – B	ADC B Digital Output Complement
32	D + B	ADC B Digital Output True

Pin No.	Mnemonic	Description
33	D − A	ADC A Digital Output Complement
34	D + A	ADC A Digital Output True
38	SCLK/DTP	Serial Clock/Digital Test Pattern
39	SDIO/ODM	Serial Data Input-Output/Output Driver Mode
40	CSB	Chip Select Bar
41	PDWN	Power Down
43	VIN + A	ADC A Analog Input True
44	VIN − A	ADC A Analog Input Complement
46	VIN − B	ADC B Analog Input Complement
47	VIN + B	ADC B Analog Input True
49	VIN + C	ADC C Analog Input True
50	VIN − C	ADC C Analog Input Complement
52	VIN − D	ADC D Analog Input Complement
53	VIN + D	ADC D Analog Input True
54	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
55	SENSE	Reference Mode Selection
56	VREF	Voltage Reference Input/Output
57	REFB	Differential Reference (Negative)
58	REFT	Differential Reference (Positive)
60	VIN + E	ADC E Analog Input True
61	VIN − E	ADC E Analog Input Complement
63	VIN − F	ADC F Analog Input Complement
64	VIN + F	ADC F Analog Input True

EQUIVALENT CIRCUITS

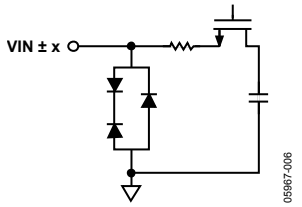

Figure 6. Equivalent Analog Input Circuit

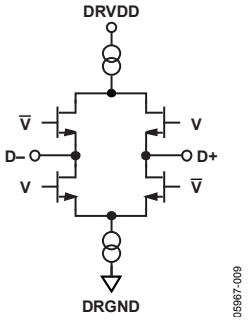

Figure 9. Equivalent Digital Output Circuit

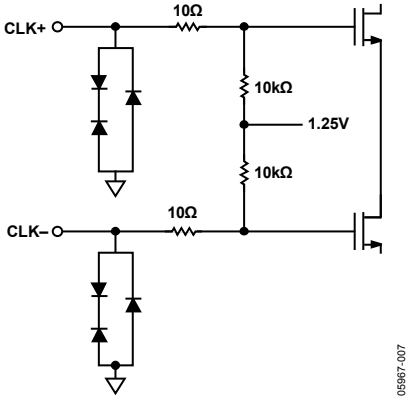

Figure 7. Equivalent Clock Input Circuit

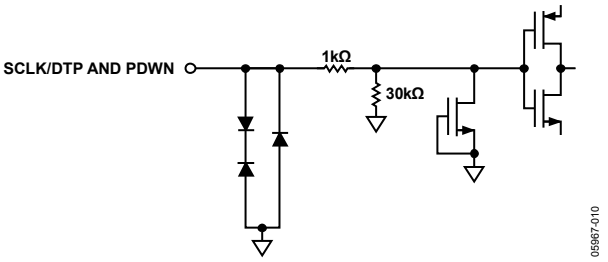

Figure 10. Equivalent SCLK/DTP and PDWN Input Circuit

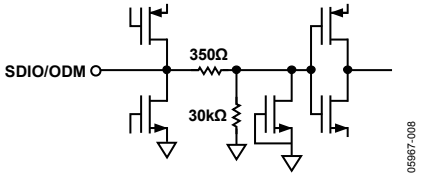

Figure 8. Equivalent SDIO/ODM Input Circuit

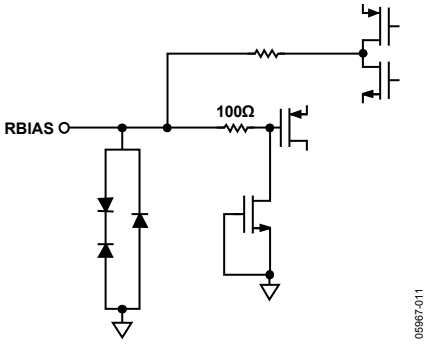

Figure 11. Equivalent RBIAS Circuit

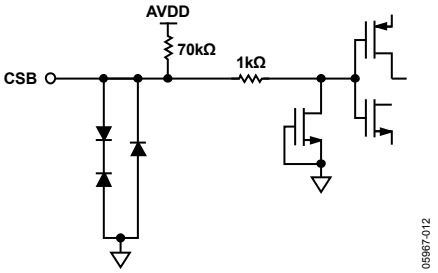

Figure 12. Equivalent CSB Input Circuit

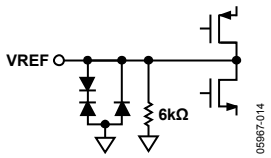

Figure 14. Equivalent VREF Circuit

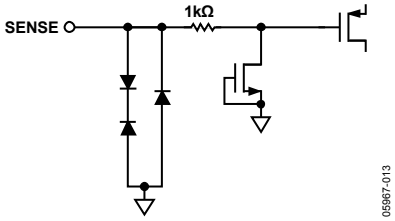

Figure 13. Equivalent SENSE Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

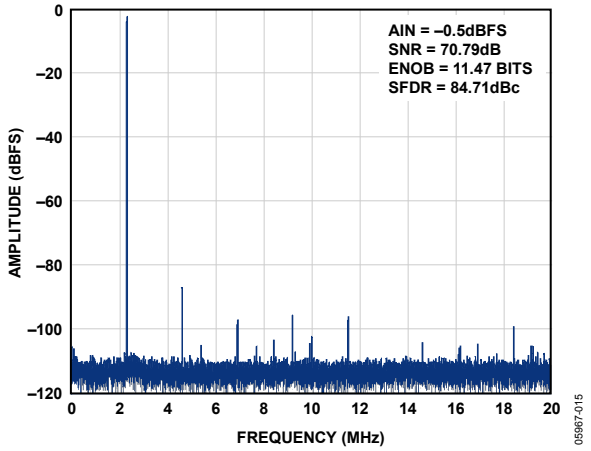

Figure 15. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, AD9222-40

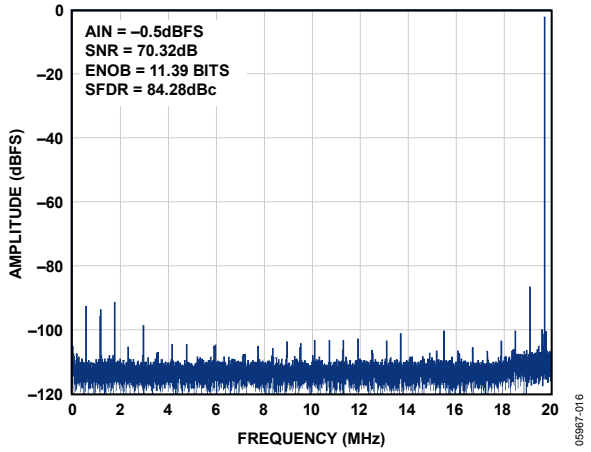

Figure 16. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, AD9222-40

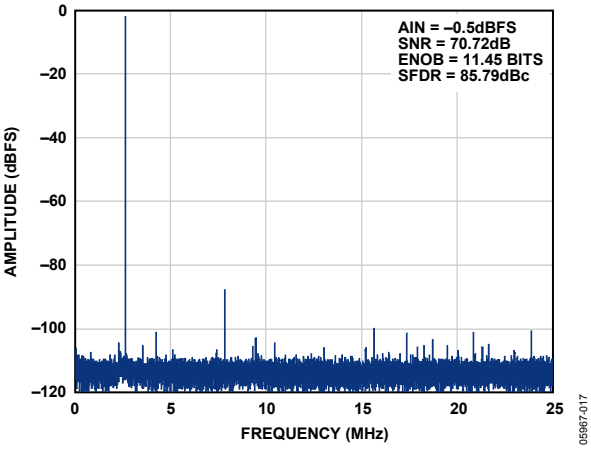

Figure 17. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, AD9222-50

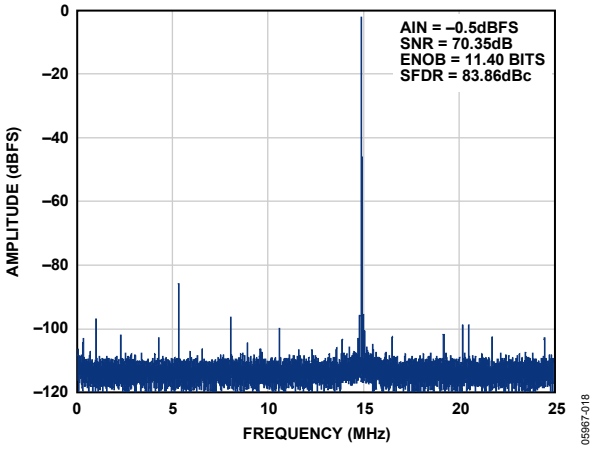

Figure 18. Single-Tone 32k FFT with f_{IN} = 35 MHz, AD9222-50

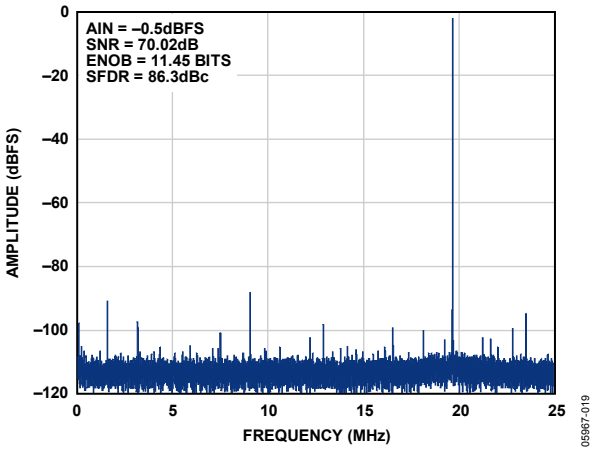

Figure 19. Single-Tone 32k FFT with f_{IN} = 70 MHz, AD9222-50

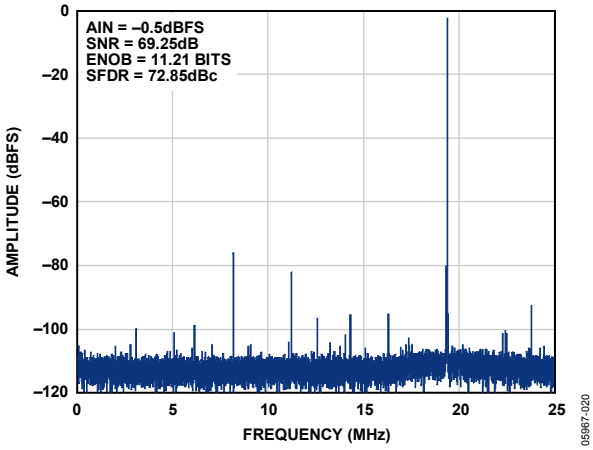

Figure 20. Single-Tone 32k FFT with f_{IN} = 120 MHz, AD9222-50

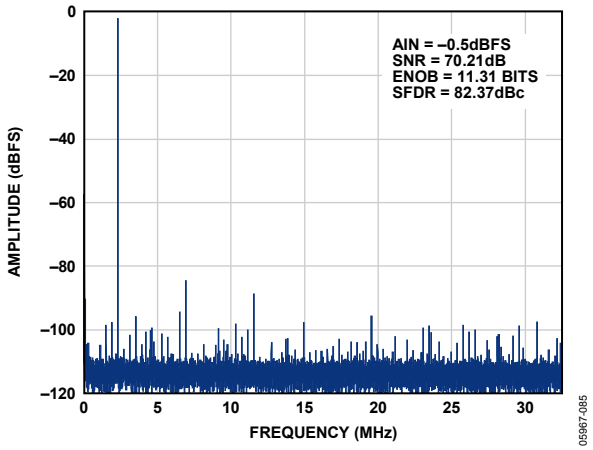

Figure 21. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, AD9222-65

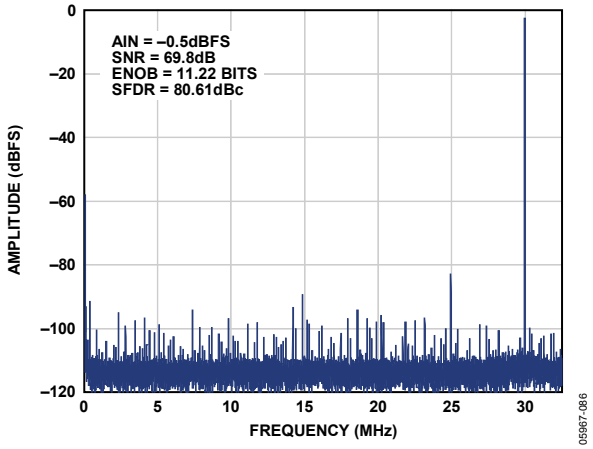

Figure 22. Single-Tone 32k FFT with f_{IN} = 35 MHz, AD9222-65

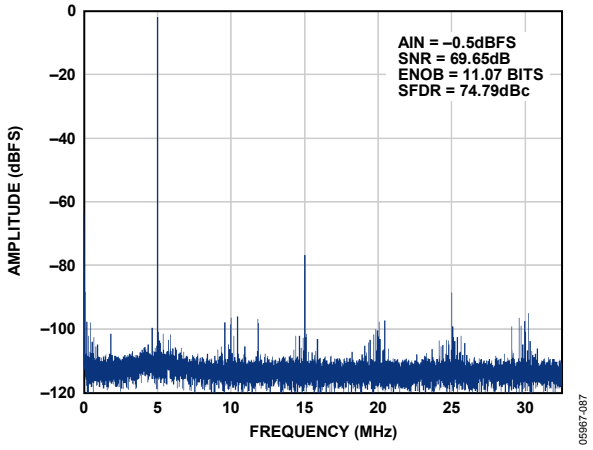

Figure 23. Single-Tone 32k FFT with f_{IN} = 70 MHz, AD9222-65

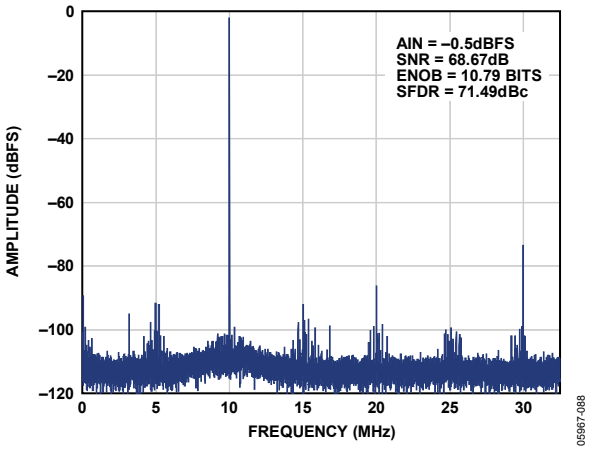

Figure 24. Single-Tone 32k FFT with f_{IN} = 120 MHz, AD9222-65

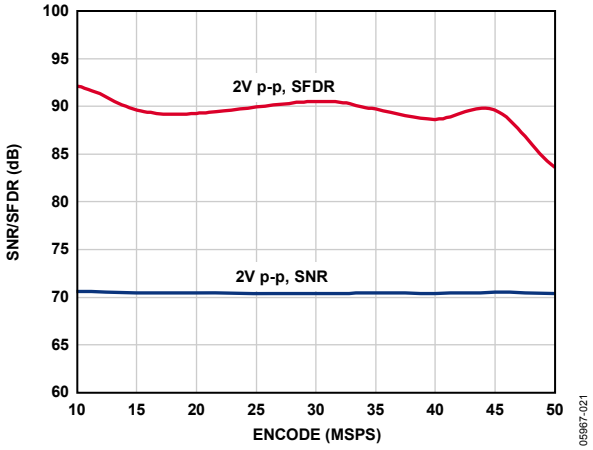

Figure 25. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 2.61 MHz, AD9222-50

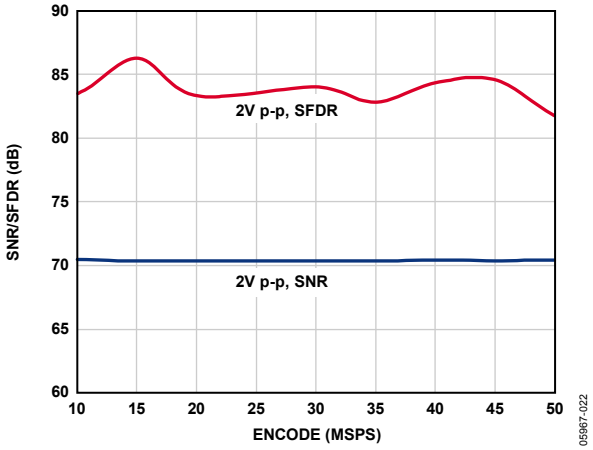

Figure 26. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 20.1 MHz, AD9222-50

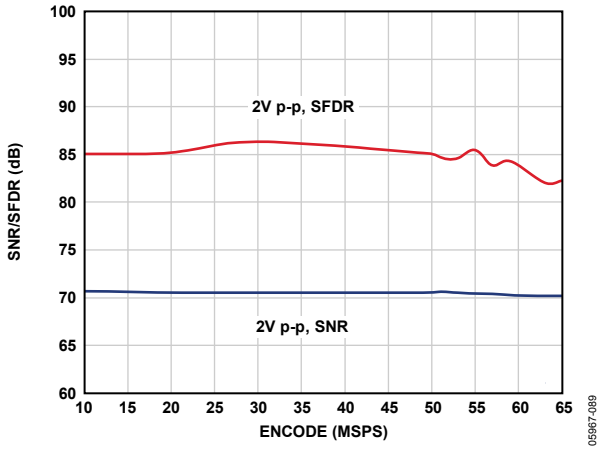

Figure 27. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 2.3 MHz, AD9222-65

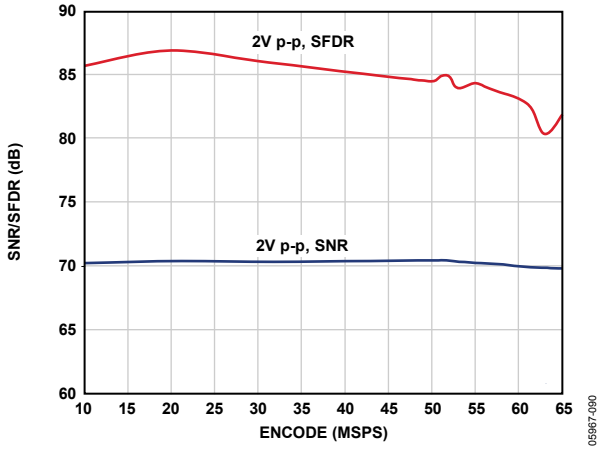

Figure 28. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 19.7 MHz, AD9222-65

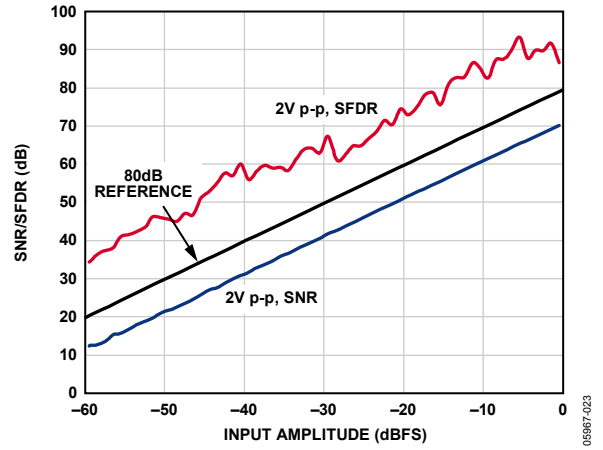

Figure 29. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, AD9222-50

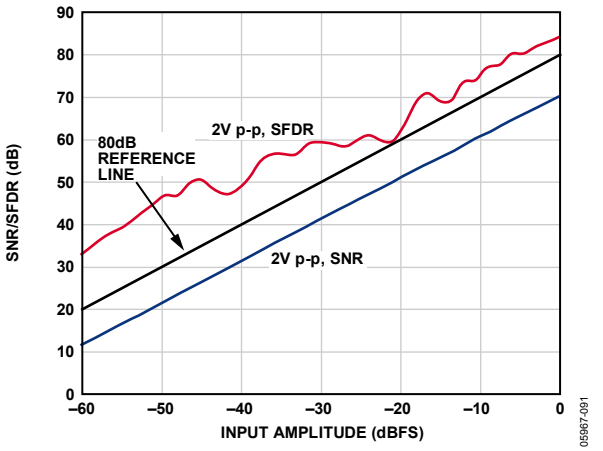

Figure 30. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, AD9222-65

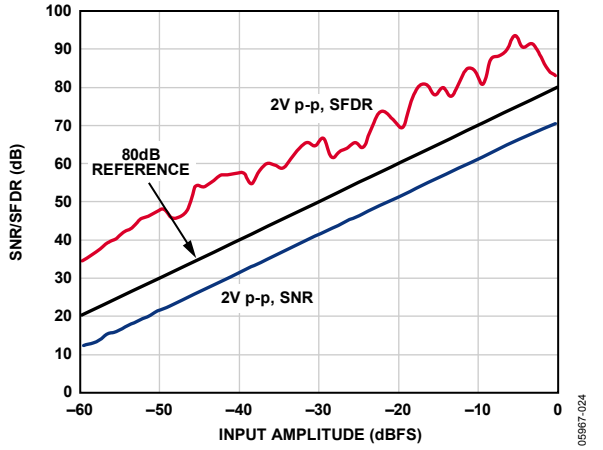

Figure 31. SNR/SFDR vs. Analog Input Level, f_{IN} = 35 MHz, AD9222-50

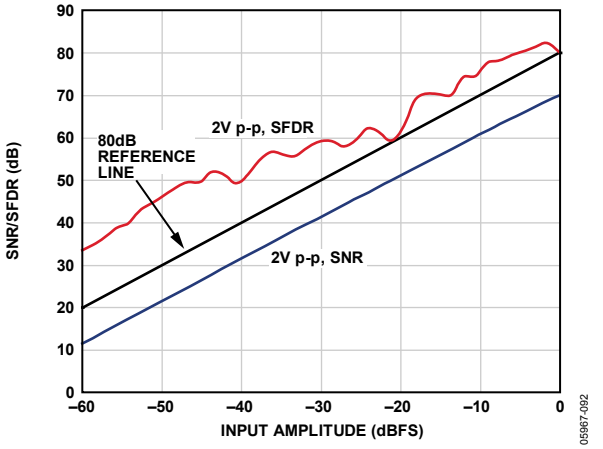

Figure 32. SNR/SFDR vs. Analog Input Level, f_{IN} = 35 MHz, AD9222-65