3 MSPS,10-/12-Bit ADCs in 8-Lead TSOT

AD7273/AD7274

FEATURES

Throughput rate: 3 MSPS
Specified for V_{DD} of 2.35 V to 3.6 V
Power consumption
11.4 mW at 3 MSPS with 3 V supplies
Wide input bandwidth
70 dB SNR at 1 MHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Temperature range: −40°C to +125°C
Power-down mode: 0.1 µA typ
8-lead TSOT package
8-lead MSOP package

FUNCTIONAL BLOCK DIAGRAM

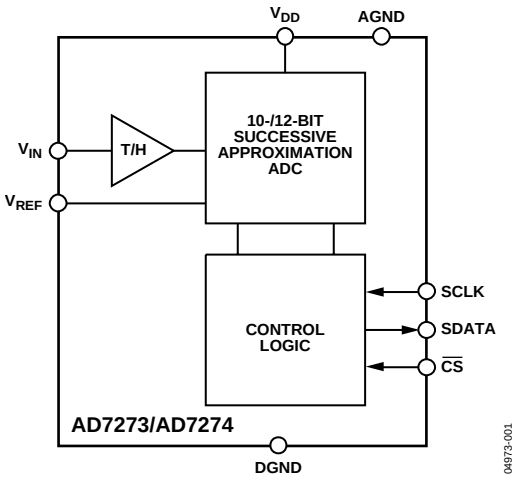

Figure 1.

GENERAL DESCRIPTION

The AD7273/AD7274 are 10-/12-bit, high speed, low power, successive approximation ADCs, respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates of up to 3 MSPS. Each part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 55 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. The conversion rate is determined by the SCLK. There are no pipeline delays associated with these parts.

The AD7273/AD7274 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the parts is applied externally and can be in the range of 1.4 V to V_{DD}. This allows the widest dynamic input range to the ADC.

Table 1.

Part Number	Resolution	Package	
AD7273[1]	10	8-lead MSOP	8-Lead TSOT
AD7274[1]	12	8-lead MSOP	8-Lead TSOT
AD7276	12	8-lead MSOP	6-Lead TSOT
AD7277	10	8-lead MSOP	6-Lead TSOT
AD7278	8	8-lead MSOP	6-Lead TSOT

[1] Parts contain external reference pin.

PRODUCT HIGHLIGHTS

1. 3 MSPS ADCs in an 8-lead TSOT package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management. Allows maximum power efficiency at low throughput rates.
4. Reference can be driven up to the power supply.
5. No pipeline delay.
6. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. 0

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REVISION HISTORY

9/05—Revision 0: Initial Version

SPECIFICATIONS

AD7274 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, V_{REF} = 2.35 V to V_{DD}, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	68	dB min	
Signal-to-Noise Ratio (SNR)	69.5	dB min	
Total Harmonic Distortion (THD)[3]	−73	dB max	
	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	ns typ	
Aperture Jitter	18	ps typ	
Full Power Bandwidth	55	MHz typ	@ 3 dB
	8	MHz typ	@ 0.1 dB
Power Supply Rejection Ratio (PSRR)	82	dB typ	
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[3]	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	Guaranteed no missed codes to 12 bits
Offset Error[3]	±3	LSB max	
Gain Error[3]	±3.5	LSB max	
Total Unadjusted Error (TUE)[3]	±3.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	V	
DC Leakage Current	±1	µA max	−40°C to +85°C
	±5.5	µA max	85°C to 125°C
Input Capacitance	42	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.4 to V_{DD}	V min/V max	
DC leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
Input Impedance	32	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	V max	2.35 V ≤ V_{DD} < 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	2	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	pF max	
Output Coding	Straight (natural) binary		

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	291	ns max	14 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	ns max	
Throughput Rate	3	MSPS max	See the Serial Interface section
POWER RQUIREMENTS			
V_{DD}	2.35/3.6	V min/V max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	1	mA typ	V_{DD} = 3 V, SCLK on or off
Normal Mode (Operational)	5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.8	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	µA typ	
Full Power-Down Mode (Static)	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	µA max	85°C to 125°C
Power Dissipation[5]			
Normal Mode (Operational)	18	mW max	V_{DD} = 3.6 V , f_{SAMPLE} = 3 MSPS
	11.4	mW typ	V_{DD} = 3 V
Partial Power-Down	102	µW max	V_{DD} = 3 V
Full Power-Down	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and V_{REF} = 3 V at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

AD7273 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, V_{REF} = 2.35 V to V_{DD}, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	61	dB min	
Total Harmonic Distortion (THD)[3]	−72	dB max	
	−77	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−81	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−81	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	ns typ	
Aperture Jitter	18	ps typ	
Full Power Bandwidth	74	MHz typ	@ 3 dB
	10	MHz typ	@ 0.1 dB
Power Supply Rejection Ratio (PSRR)	82	dB typ	
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[3]	±0.5	LSB max	
Differential Nonlinearity[3]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[3]	±1	LSB max	
Gain Error[3]	±1.5	LSB max	
Total Unadjusted Error (TUE)[3]	±2.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	V	
DC Leakage Current	±1	µA max	−40°C to +85°C
	±5.5	µA max	85°C to 125°C
Input Capacitance	42	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.4 to V_{DD}	V min/V max	
DC leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
Input Impedance	32	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{IN}	0.7	V max	2.35 V ≤ V_{DD}< 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	2	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	pF max	
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	250	ns max	12 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	ns max	
Throughput Rate	3.45	MSPS max	See the Serial Interface section

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
POWER RQUIREMENTS			
V_{DD}	2.35/3.6	V min/V max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	0.6	mA typ	V_{DD} = 3 V, SCLK on or off
Normal Mode (Operational)	5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.2	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	µA typ	
Full Power-Down Mode (Static)	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	µA max	85°C to 125°C
Power Dissipation[5]			
Normal Mode (Operational)	18	mW max	V_{DD} = 3.6 V , f_{SAMPLE} = 3 MSPS
	9.6	mW typ	V_{DD} = 3 V
Partial Power-Down	102	µW max	V_{DD} = 3 V
Full Power-Down	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and V_{REF} = 3 V at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V; V_{REF} = 2.35 to V_{DD}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1] Guaranteed by characterization. All input signals are specified with tr = tf = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX} AD7273/AD7274	Unit	Description
f_{SCLK}[2]	500	kHz min[3]	
	48	MHz max	
$t_{CONVERT}$	14 × t_{SCLK}		AD7274
	12 × t_{SCLK}		AD7273
t_{QUIET}	4	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	3	ns min	Minimum $\overline{CS}$ pulse width
t_2	6	ns min	$\overline{CS}$ to SCLK setup time
t_3[4]	4	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[4]	15	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7[4]	5	ns min	SCLK to data valid hold time
t_8	14	ns max	SCLK falling edge to SDATA three-state
	5	ns min	SCLK falling edge to SDATA three-state
t_9	4.2	ns max	$\overline{CS}$ rising edge to SDATA three-state
$t_{POWER-UP}$[5]	1	µs max	Power-up time from full power-down

[1] Sample tested during initial release to ensure compliance. All timing specifications given are with a 10 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Minimum f_{SCLK} at which specifications are guaranteed.
[4] The time required for the output to cross the V_{IH} or V_{IL} voltage.
[5] See the Power-Up Times section

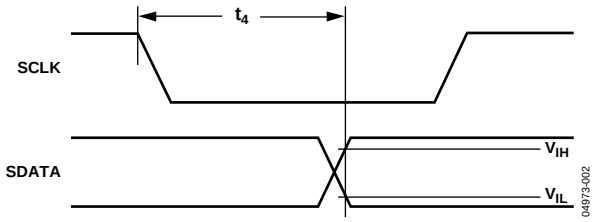

Figure 2. Access Time After SCLK Falling Edge

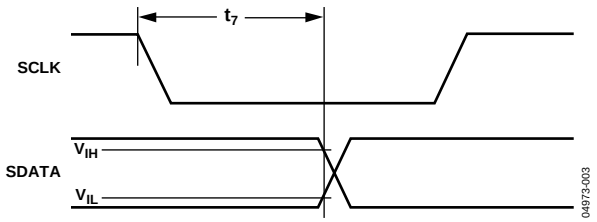

Figure 3. Hold Time After SCLK Falling Edge

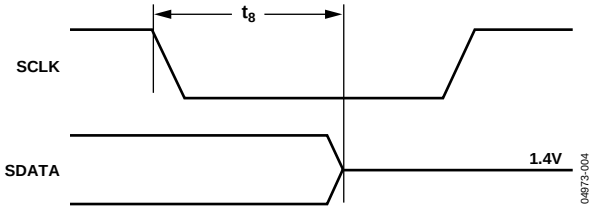

Figure 4. SCLK Falling Edge SDATA Three-State

TIMING EXAMPLES

For the AD7274, if $\overline{CS}$ is brought high during the 14th SCLK rising edge after the two leading zeros and 12 bits of the conversion are provided, the part can achieve the fastest throughput rate, 3 MSPS. If $\overline{CS}$ is brought high during the 16th SCLK rising edge after the two leading zeros, 12 bits of the conversion, and two trailing zeros are provided, a throughput rate of 2.97 MSPS is achievable. This is illustrated in the following two timing examples.

Timing Example 1

In Figure 6, using a 14 SCLK cycle, f_{SCLK} = 48 MHz, and the throughput is 3 MSPS. This produces a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 333 ns, where t_2 = 6 ns min and t_{ACQ} = 67 ns. This satisfies the requirement of 60 ns for t_{ACQ}. Figure 6 also shows that t_{ACQ} comprises $0.5(1/f_{SCLK}) + t_9 + t_{QUIET}$, where t_9 = 4.2 ns max. This allows a value of 52.8 ns for t_{QUIET}, satisfying the minimum requirement of 4 ns.

Timing Example 2

The example in Figure 7 uses a 16 SCLK cycle, f_{SCLK} = 48 MHz, and the throughput is 2.97 MSPS. This produces a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 336 ns, where t_2 = 6 ns min and t_{ACQ} = 70 ns. Figure 7 shows that t_{ACQ} comprises $2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where t_8 = 14 ns max. This satisfies the minimum requirement of 4 ns for t_{QUIET}.

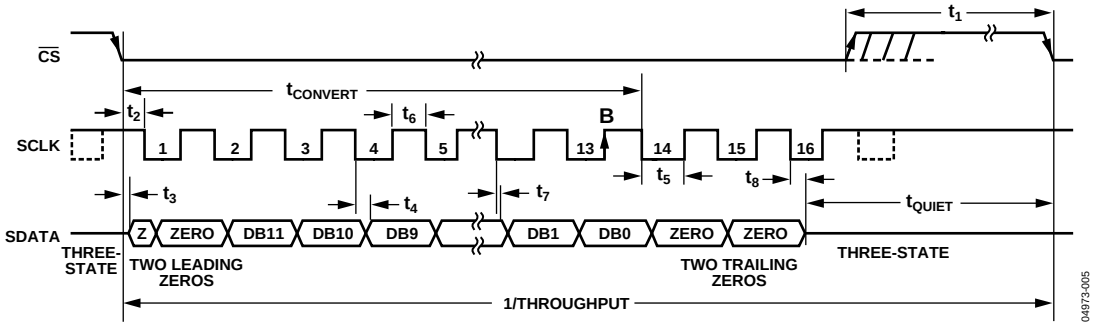

Figure 5. AD7274 Serial Interface Timing 16 SCLK Cycle

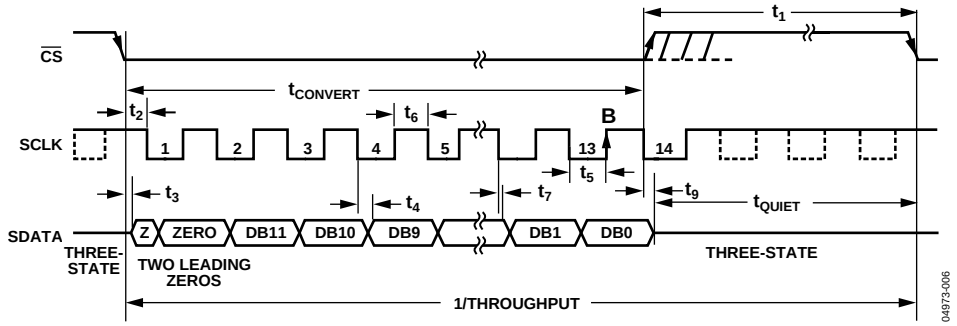

Figure 6.AD7274 Serial Interface Timing 14 SCLK Cycle

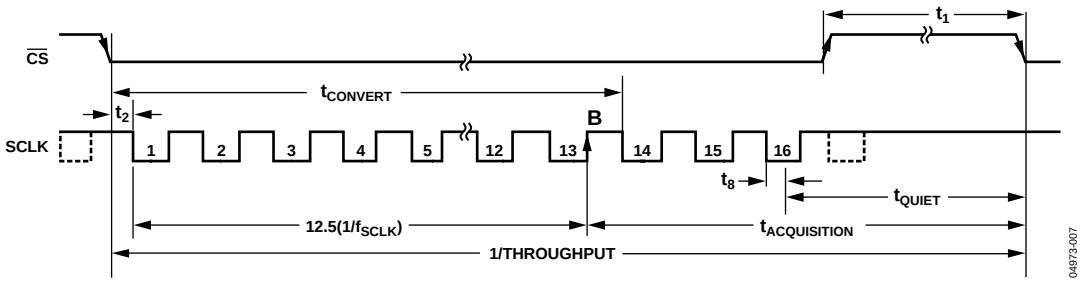

Figure 7. Serial Interface Timing 16 SCLK Cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameters	Ratings
V_{DD} to AGND/DGND	−0.3 V to +6 V
Analog Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +6 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
6-Lead TSOT Package	
θ_{JA} Thermal Impedance	230°C/W
θ_{JC} Thermal Impedance	92°C/W
8-Lead MSOP Package	
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature Soldering	
Reflow (10 to 30 sec)	255°C
Lead Temperature Soldering	
Reflow (10 to 30 sec)	260°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

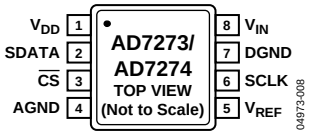

Figure 8. 8-Lead MSOP Pin Configuration

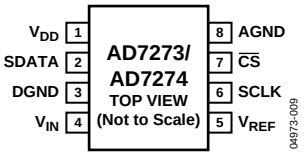

Figure 9. 8-Lead TSOT Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
MSOP	**TSOT**	**Mnemonic**	**Description**
1	1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7273/AD7274 is from 2.35 V to 3.6 V.
2	2	SDATA	Data Out. Logic output. The conversion result from the AD7273/AD7274 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7274 consists of two leading zeros followed by the 12 bits of conversion data and two trailing zeros, provided MSB first. The data stream from the AD7273 consists of two leading zeros followed by the 10 bits of conversion data and four trailing zeros, provided MSB first.
3	7	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversion on the AD7273/AD7274 and framing the serial data transfer.
4	8	AGND	Analog Ground. Ground reference point for all circuitry on the AD7273/AD7274. All analog signals and any external reference signal should be referred to this AGND voltage.
5	5	V_{REF}	Voltage Reference Input. This pin becomes the reference voltage input. An external reference should be applied at this pin. The external reference input range is 1.4 V to V_{DD}. A 10 µF capacitor should be tied between this pin and AGND.
6	6	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of AD7273/AD7274.
7	3	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7273/AD7274. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
8	4	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{REF}.