Freescale Semiconductor
Product Brief

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QorIQ™ P2020 Communications Processor Product Brief

This document provides an overview of features and functionality of the QorIQ™ P2020 communications processor. The P2020 combines dual Power Architecture™ e500v2 processor cores with system logic required for networking, wireless infrastructure, and telecommunications applications.

The P2020 offers an excellent combination of protocol and interface support including dual high-performance CPU cores, a DDR2/DDR3 memory controller, three enhanced three-speed Ethernet controllers with SGMII support, two Serial RapidIO® interfaces with a messaging unit, a secure digital interface, a USB 2.0 interface, and three PCI Express controllers. The device also supports IEEE Std 1588™ precision time protocol for network synchronization over Ethernet.

Contents

1 P2020 Overview

This section describes the features of the device.

1.1 Block Diagram

Figure 1 shows the major functional units within the P2020.

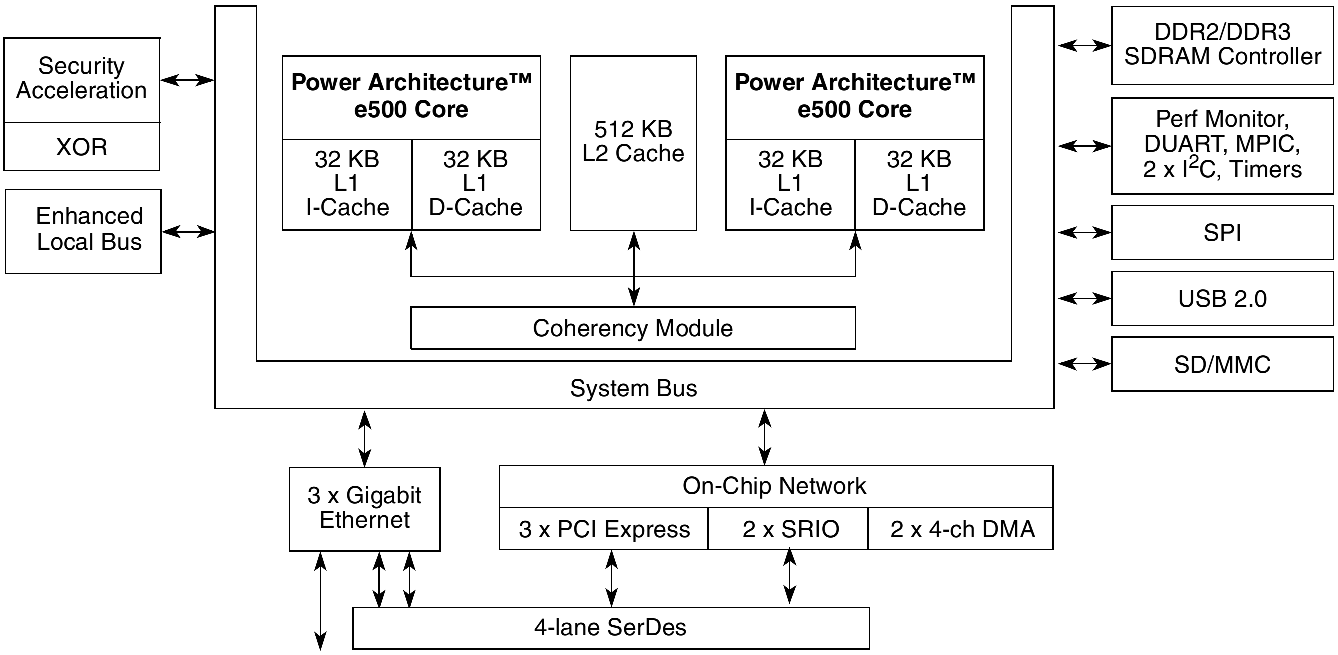

Figure 1. P2020 Block Diagram

1.2 Critical Performance Parameters

Critical performance parameters are as follows:

- e500v2 core frequency of up to 1.2 GHz
- 45-nm SOI process technology
- Supply voltages:
  - Core: 1.05 V
  - PCI Express, Serial RapidIO: 1.05 V
  - Ethernet: 3.3 or 2.5 V (subject to protocol)
  - Local bus: 3.3, 2.5, or 1.8 V
  - DDR: 1.8 V for DDR2, 1.5 V for DDR3 (conforms to JEDEC standard)
  - SGMII: 1.05 V
  - SPI, eSDHC, USB: 3.3, 2.5, or 1.8 V
- Operating junction temperature (T_j) range: 0–125° C and –40–125° C (industrial specification)
- Package: 31 × 31 mm 689-pin TEPBGA (thermally-enhanced plastic BGA)

1.3 Chip-Level Features

Key features of the P2020 include the following:

- Dual high-performance Power Architecture e500v2 cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache for each core
- 512-Kbyte L2 cache with ECC
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
- High-speed interfaces:
  - Two x1 or one x4 Serial RapidIO interfaces with message unit
  - Three PCI Express interfaces:
    - Two x1, one x2
    - Two x2
    - One x4
  - Two SGMII interfaces
- High-speed USB interface (USB 2.0)
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface

- Integrated security engine (optional)
  - XOR acceleration
  - Protocol support includes SNOW, ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS, Kasumi
- DDR2/DDR3 SDRAM memory controller with ECC support
- Power management controller
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Two four-channel DMA controllers
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals

These features are described in greater detail in subsequent sections.

NOTE

The P2020 is also available without a security engine. All specifications other than those relating to security apply to the non-security version exactly as described in this document.

2 P2020 Application Examples

The following section provides block diagrams of different applications. The P2020 is a very flexible device and can be configured to meet many system application needs.Target applications include the following:

- Networking (switches and routers)—Line card controller, mid-range line card control plane, low-end line card combined control and data plane, shelf controller, business gateway, multiservice router, wireless access points
- Telecommunications—AMC card, controller on ATCA carrier card, channel and control card for NodeB/BTS/WCDMA/4G LTE/WiMax, general-purpose compute blade
- Industrial—Robotics, multifunction printer, single board computers, industrial applications, test and measurement for networking/telecommunications

Both cores can operate in a symmetric multiprocessing mode to achieve higher performance, or they can perform separate tasks, optionally running independent operating systems. This flexibility enables application developers to assign distinct processing resources to distinct tasks that need guaranteed performance. For example, one core can manage a data plane and the other a control plane.

The LTE and WiMax baseband and line card control plane applications are described in the following sections.

2.1 LTE and WiMax Baseband Application

As an integrated dual-core device, the P2020 is well-suited for Long Term Evolution (LTE) and WiMax channel card applications. The P2020 offers dual-core performance without breaking out of a single core power budget. Additionally, in order to maximize subscriber bandwidth, the P2020 also offers support for the increased performance needed in Layer 2 baseband processing and implementing network interfaces.

Figure 2 shows an example of a channel card application using the P2020. The advanced Quality of Service (QoS) features of the eTSEC ports assist in resource scheduling and Medium Access Control (MAC), implemented by Layer 2 baseband processing. For network interfacing, the P2020 supports dual Gigabit Ethernet on SGMII and dual Serial RapidIO (for redundancy). The Serial RapidIO interface also allows direct connection to the digital signal processors (DSPs), such as Freescale's MSC8156, that implement the Layer 1 processing. The security block handles the secure network termination requirement

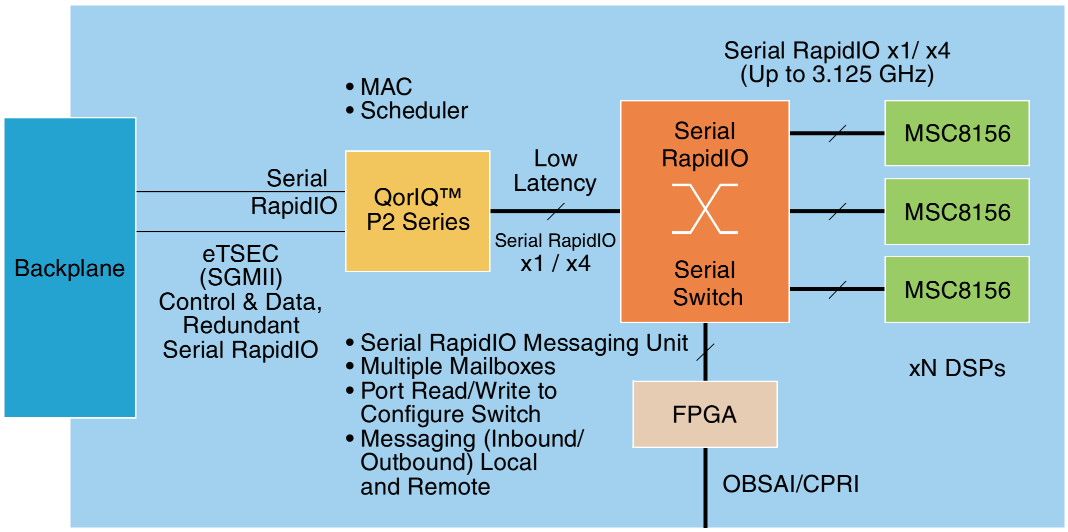

Figure 2. Channel Card Application

2.2 Line Card Control Plane Application

One of the primary applications for the P2020 is as a line card control plane processor, as shown in Figure 3. Typically the P2020 sits to the side of the main datapath, which has I/O processors on the front panel connected to a backplane interface device. The P2020 communicates with these components using standard interfaces, such as PCI Express or the local bus. The P2020 often has front panel interfaces as well. One eTSEC may be used for high-performance debug; the DUART can be used for a low-level command line interface; and the USB port may be used for front-panel code uploads when connecting directly to a PC for maintenance. Redundant Gigabit Ethernet ports to the backplane are used as a management interface, which can be used to communicate with a centralized resource for receiving table updates, for instance. The SD/MMC interface enables modularity by supporting booting from flash cards.

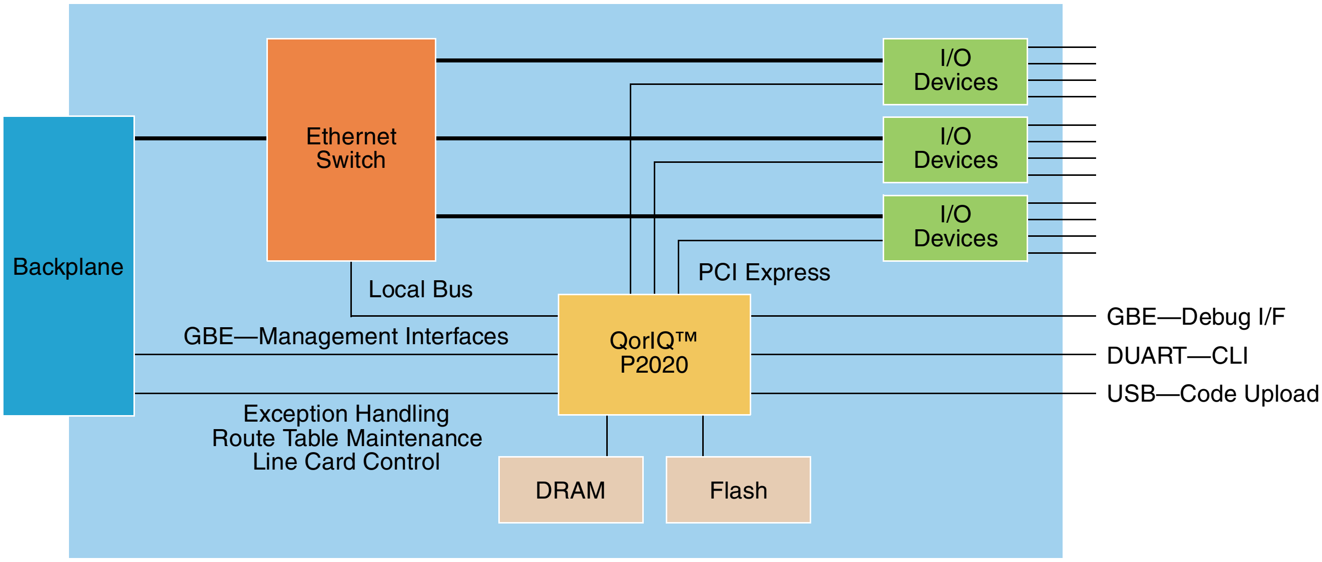

Figure 3. Line Card Control Plane Application

3 P2020 Architecture Overview

This section contains a high-level view of the device architecture.

3.1 e500v2 Cores and Memory Unit

The P2020 contains two high-performance 32-bit e500v2 cores that implement the Power Architecture. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- SPE double-precision floating-point instruction set using 64-bit operands
- SPE embedded vector and scalar single-precision floating-point instruction set using 32- or 64-bit operands
- 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection

The device also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - — I/O devices access SRAM regions by marking transactions as snoopable (global).
  - — Regions can reside at any aligned location in the memory map.
  - — Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

3.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500v2 cores and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The P2020 supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by ten local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The P2020 can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the P2020 to be part of larger address maps such as those of PCI Express or RapidIO.

3.3 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.11i™, IEEE 802.16 (WiMAX), IEEE 802.1AE (MACSec), 3GPP, A5/3 for GSM and EDGE, and GEA3 for GPRS. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the P2020 is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

SEC features include the following:

- Compatible with code written for the Freescale MPC8548E, MPC8555E, and MPC8541E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  - PKEU—public key execution unit
  - DEU—Data Encryption Standard execution unit
  - AESU—Advanced Encryption Standard unit
  - AFEU—ARC four execution unit
  - MDEU—message digest execution unit
  - KEU—Kasumi execution unit
  - CRCU—cyclical redundancy check unit
  - RNG—random number generator
  - STHA—SNOW 3.0 hardware accelerator

3.4 Enhanced Three-Speed Ethernet Controllers

The P2020 has three on-chip enhanced three-speed Ethernet controllers (eTSECs), as used in the 90 nm PowerQUICC III family. The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with SGMII, GMII, RGMII, MII, RMII, TBI, and RTBI physical interfaces, as well as 8- or 16-bit FIFO interfaces that bypass the Ethernet MAC. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

Each eTSEC provides a full-duplex packet FIFO interface port, multiplexed on the PHY interface pins, that bypasses the Ethernet MAC. As a result, the FIFO interface does not impose the overhead of Ethernet framing.

The P2020 eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with IEEE Std. 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab.

Some of the key features of these controllers include: the following

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 1. eTSEC Configuration Options[1]

eTSEC1	eTSEC2	eTSEC3
Standard interface[2] -or- none	Standard interface -or- none	SGMII -or- none
Reduced interface[3] -or- none	Reduced interface -or- SGMII -or- none	SGMII -or- none
16-bit FIFO	SGMII -or- none	SGMII -or- none
RGMII -or- RTBI -or- RMII -or- none	RGMII -or- RTBI -or- RMII -or- SGMII -or- none	RGMII -or- RTBI -or- RMII -or- SGMII -or- none

Notes:

[1] The parallel interfaces must use the same voltage.

[2] Standard interfaces are GMII, TBI, MII.

[3] Reduced interfaces are RGMII, RTBI, RMII.

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

3.5 Universal Serial Bus (USB) 2.0

The P2020 USB 2.0 controller provides point-to-point connectivity complying with the USB specification, Rev. 2.0. The USB controller can be configured to operate as a stand-alone host or stand-alone device. The host and device functions are both configured to support the following types of USB transfers:

- Bulk
- Control
- Interrupt
- Isochronous

Other controller features are as follows:

The USB dual-role controller does the following:

- Supports USB dual-role operation and can be configured as host or device
- Complies with USB specification, Rev. 2.0
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports six programmable USB endpoints
- Supports operation as a stand-alone USB host controller

  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Supports external PHY with UTMI+ low-pin interface (ULPI)

3.6 Enhanced Secure Digital Host Controller

The enhanced secure digital host controller (eSDHC) provides an interface between the host system and SD/MMC cards. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards. It handles SD/MMC protocols at the transmission level. For the P2020, booting from on-chip ROM is supported through the eSDHC.

The secure digital (SD) card is an evolution of old MultiMediaCard (MMC) technology. The MMC is a universal low-cost data storage and communication media designed to cover a wide area of applications including mobile video and gaming, which are available from either pre-loaded MMC cards or downloadable from cellular phones, WLAN, or other wireless networks. Old MMC cards are based on a 7-pin serial bus with a single data pin, while the new high-speed MMC communication is based on an advanced 11-pin serial bus designed to operate in a low voltage range.

The SD card is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. The physical form factor, pin assignments, and data transfer protocol are forward compatible with the old MMC.

3.7 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other communication processors, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit. The P2020 also has the ability to boot from an SPI serial flash device.

The SPI receiver and transmitter each have a FIFO of 32 bytes to support more efficient transfers to and from SPI devices. The SPI interface supports RapidS for Atmel devices as well as Winbond devices dual read commands; in this mode the SPI uses two bits in parallel for reads.

3.8 DDR SDRAM Controller

The P2020 supports DDR2 and DDR3 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 32 Gbytes of main memory.

The device supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities from 64 Mbits to 8 Gbits. Four chip select signals support up to four banks of memory. The device supports bank sizes from 64 Mbytes to 8 Gbytes. Nine column address strobes ($\overline{\text{MDM}}$[0:8]) are used to provide byte selection for memory bank writes.

The P2020 can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 32 simultaneously open pages can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the device detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The device can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The P2020 offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature which system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

3.9 High Speed I/O Interfaces

The P2020 supports the SGMII, Serial RapidIO, and PCI Express high-speed I/O interface standards.

3.9.1 PCI Express Interfaces

The P2020 supports three PCI Express interfaces that are compliant with the *PCI Express Base Specification Revision 1.0a*. They are configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

Other features of the PCI Express interface include the following:

- x4, x2, and x1 link widths supported
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

3.9.2 Serial RapidIO Interfaces

The two Serial RapidIO interfaces are based on the *RapidIO Interconnect Specification, Revision 1.2*. RapidIO is a high-performance, point-to-point, low-pin-count, packet-switched system-level interconnect that can be used in a variety of applications as an open standard. The RapidIO architecture has a rich variety of features including high data bandwidth, low-latency capability, and support for high-performance I/O devices, as well as support for message-passing and software-managed programming models. Key features of the Serial RapidIO interface unit include:

- Support for *RapidIO Interconnect Specification, Revision 1.2* (all transaction flows and priorities)
- Both 1x and 4x LP-serial link interfaces, with transmission rates of 1.25, 2.5, or 3.125 Gbaud (data rates of 1.0, 2.0, or 2.5 Gbps) per lane

- Auto detection of 1x or 4x mode operation during port initialization
- 34-bit addressing and up to 256-byte data payload
- Receiver-controlled flow control
- Support for RapidIO error injection
- Internal LP-serial and application interface-level loopback modes

The RapidIO messaging unit supports two inbox/outbox mailboxes (queues) for data and one doorbell message structure. Both chaining and direct modes are provided for the outbox, and messages can hold up to 16 packets of 256 bytes, or a total of 4 Kbytes.

3.9.3 SGMII

The serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signaling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse; no clock signals are required.

3.9.4 High-Speed Interface Multiplexing

Table 2 shows the supported high-speed interface configurations. The desired configuration must be selected at power-on reset.

Table 2. Supported High-Speed Interface Combinations

<table>
<tr><th colspan="4">Lanes</th><th colspan="2">Gbaud</th></tr>
<tr><th>A</th><th>B</th><th>E</th><th>F</th><th>A&B</th><th>E&F</th></tr>
<tr><td>PEX1: x1</td><td>off</td><td>off</td><td>off</td><td>2.5</td><td>—</td></tr>
<tr><td>off</td><td>off</td><td>off</td><td>off</td><td>—</td><td>—</td></tr>
<tr><td>PEX1: x1</td><td>PEX2: x1</td><td colspan="2">PEX3: x2</td><td>2.5</td><td>2.5</td></tr>
<tr><td colspan="4">Reserved</td><td>—</td><td>—</td></tr>
<tr><td colspan="2">PEX1: x2</td><td colspan="2">PEX3: x2</td><td>2.5</td><td>2.5</td></tr>
<tr><td colspan="4">Reserved</td><td colspan="2">—</td></tr>
<tr><td colspan="4">PEX1: x4</td><td colspan="2">2.5</td></tr>
<tr><td>SRIO2: 1x</td><td>SRIO1: 1x</td><td>off</td><td>off</td><td>3.125</td><td>—</td></tr>
<tr><td colspan="4">SRIO2: 4x</td><td colspan="2">1.25</td></tr>
<tr><td colspan="4">SRIO2: 4x</td><td colspan="2">2.5</td></tr>
<tr><td colspan="4">SRIO2: 4x</td><td colspan="2">3.125</td></tr>
<tr><td>SRIO2: 1x</td><td>SRIO1: 1x</td><td>SGMII2</td><td>SGMII3</td><td>1.25</td><td>1.25</td></tr>
<tr><td>SRIO2: 1x</td><td>SRIO1: 1x</td><td>SGMII2</td><td>SGMII3</td><td>2.5</td><td>1.25</td></tr>
<tr><td>PEX1: x1</td><td>SRIO1: 1x</td><td>SGMII2</td><td>SGMII3</td><td>2.5</td><td>1.25</td></tr>
<tr><td>PEX1: x1</td><td>PEX2: x1</td><td>SGMII2</td><td>SGMII3</td><td>2.5</td><td>1.25</td></tr>
<tr><td colspan="2">PEX1: x2</td><td>SGMII2</td><td>SGMII3</td><td>2.5</td><td>1.25</td></tr>
</table>

3.10 Programmable Interrupt Controller (PIC)

The P2020 PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported. The PIC can be bypassed to allow use of an external interrupt controller.

3.11 DMA, I^2C, DUART, and Enhanced Local Bus Controller

The P2020 provides two integrated four-channel DMA controllers, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controllers can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.
- To handle misaligned transfers as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The enhanced local bus controller (eLBC) port allows connection with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The NAND flash control machine (FCM) further extends interface options. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or FCM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 16-bit address and data bus operating at up to 150 MHz
- 32-bit address support
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8 or 16 bits)
- Supports zero-bus-turnaround (ZBT) RAM
- FCM supports NAND flash, GPCM supports NOR flash

3.12 Device Boot Locations

The P2020 may be configured to boot using one of the following interfaces:

- DDR2/DDR3 memory controller
- Any PCI Express interface
- Any Serial RapidIO interface
- Enhanced local bus interface (using the GPCM or FCM)
- SPI flash
- SD/MMC flash

3.12.1 Boot Sequencer

The P2020 provides a boot sequencer that uses the I^2C1 interface to access an external serial ROM and loads the data into the device's configuration registers. The boot sequencer is enabled by a configuration pin sampled at the negation of the devices's hardware reset signal. If enabled, the boot sequencer holds the processor cores in reset until the boot sequence is complete. If the boot sequencer is not enabled, the processor cores exit reset and fetch boot code in default configurations.

3.13 Power Management

The P2020E has features to minimize power consumption at several levels. Dynamic power management locally minimizes power consumption when a block is idle. Software can also shut down clocks to individual blocks when they are not needed. Additionally, software running on the e500 cores can access the cores's SPRs to put the device into doze or nap power-down state. Overall, four power consumption modes are supported: full on, doze, nap, and sleep.

3.14 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

4 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and the Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

5 Document Revision History

Table 3 provides a revision history for this product brief.

Table 3. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	01/2009	Initial release.

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