Complete, Quad, 12-/14-/16-Bit, Serial Input, Unipolar/Bipolar Voltage Output DACs

AD5724R/AD5734R/AD5754R

FEATURES

Complete, quad, 12-/14-/16-bit DACs
Operates from single/dual supplies
Software programmable output range
+5 V, +10 V, +10.8 V, ±5 V, ±10 V, ±10.8 V
INL error: ±16 LSB maximum, DNL error: ±1 LSB maximum
Total unadjusted error (TUE): 0.1% FSR maximum
Settling time: 10 µs typical
Integrated reference: ±5 ppm/°C maximum
Integrated reference buffers
Output control during power-up/brownout
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous $\overline{\text{CLR}}$ to zero scale/midscale
DSP/microcontroller-compatible serial interface
24-lead TSSOP
Operating temperature range: −40°C to +85°C
***i*CMOS process technology[1]**

APPLICATIONS

Industrial automation
Closed-loop servo control, process control
Automotive test and measurement
Programmable logic controllers

GENERAL DESCRIPTION

The AD5724R/AD5734R/AD5754R are quad, 12-/14-/16-bit serial input, voltage output, digital-to-analog converters (DACs). They operate from single supply voltages of +4.5 V up to +16.5 V or dual supply voltages from ±4.5 V up to ±16.5 V. Nominal full-scale output range is software selectable from +5 V, +10 V, +10.8 V, ±5 V, ±10 V, or ±10.8 V. Integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry are also provided.

The parts offer guaranteed monotonicity, integral nonlinearity (INL) of ±16 LSB maximum, low noise, 10 µs typical settling time, and an on-chip +2.5 V reference.

The AD5724R/AD5734R/AD5754R use a serial interface that operates at clock rates up to 30 MHz and are compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is user-selectable twos complement or offset binary for a bipolar output (depending on the state of Pin BIN/$\overline{\text{2sCOMP}}$) and straight binary for a unipolar output. The asynchronous clear function clears all DAC registers to a user-selectable zero-scale or mid-scale output. The parts are available in a 24-lead TSSOP and offer guaranteed specifications over the −40°C to +85°C industrial temperature range.

Table 1. Pin Compatible Devices

Part Number	Description
AD5724/AD5734/AD5754	AD5724R/AD5734R/AD5754R without internal reference.
AD5722/AD5732/AD5752	Complete, dual, 12-/14-/16-bit, serial input, unipolar/bipolar, voltage output DACs.
AD5722R/AD5732R/AD5752R	AD5722/AD5732/AD5752 with internal reference.

[1] *i*CMOS®, Reg. U.S. Patent and Trademark Office.

Rev. A

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1/09—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

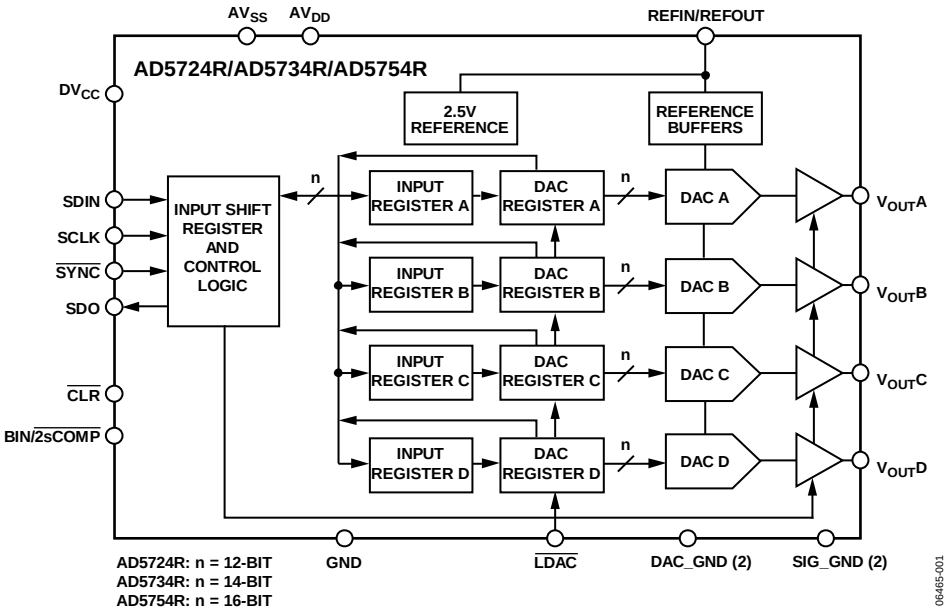

Figure 1.

SPECIFICATIONS

AV_{DD} = 4.5 V[1] to 16.5 V, AV_{SS} = −4.5 V[1] to −16.5 V or AV_{SS} = 0 V, GND = 0 V, REFIN= +2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Outputs unloaded
Resolution					
AD5754R	16			Bits	
AD5734R	14			Bits	
AD5724R	12			Bits	
Total Unadjusted Error (TUE)	−0.1		+0.1	% FSR	
Integral Nonlinearity (INL)[2]					
AD5754R	−16		+16	LSB	
AD5734R	−4		+4	LSB	
AD5724R	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	All models, guaranteed monotonic
Bipolar Zero Error	−6		+6	mV	T_A = 25°C, error at other temperatures obtained using bipolar zero TC
Bipolar Zero TC[3]		±4		ppm FSR/°C	
Zero-Scale Error	−6		+6	mV	T_A = 25°C, error at other temperatures obtained using zero-scale TC
Zero-Scale TC[3]		±4		ppm FSR/°C	
Offset Error	−6		+6	mV	T_A = 25°C, error at other temperatures obtained using offset error TC
Offset Error TC[3]		±4		ppm FSR/°C	
Gain Error	−0.025		+0.025	% FSR	±10 V range, T_A = 25°C, error at other temperatures obtained using gain TC
Gain Error[3]	−0.065		0		+10 V and +5 V ranges, T_A = 25°C, error at other temperatures obtained using gain TC
Gain Error[3]	0		+0.08		±5 V range, T_A = 25°C, error at other temperatures obtained using gain TC
Gain TC[3]		±4		ppm FSR/°C	
DC Crosstalk[3]			120	µV	
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage		2.5		V	±1% for specified performance
DC Input Impedance	1	5		MΩ	
Input Current	−2	±0.5	+2	µA	
Reference Range	2		3	V	
Reference Output					
Output Voltage	2.497		2.501	V	T_A = 25°C
Reference TC[3, 4]		1.8	5	ppm/°C	T_A = 0°C to 85°C
		2.2	10	ppm/°C	T_A = −40°C to +85°C
Output Noise (0.1 Hz to 10 Hz)[3]		5		µV p-p	
Noise Spectral Density[3]		75		nV/√Hz	@ 10 kHz
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	−10.8		+10.8	V	AV_{DD}/AV_{SS} = ±11.7 V min, REFIN = +2.5 V
	−12		+12	V	AV_{DD}/AV_{SS} = ±12.9 V min, REFIN = +3 V
Headroom		0.5	0.9	V	
Output Voltage TC		±4		ppm FSR/°C	
Output Voltage Drift vs. Time		±12		ppm FSR/500 hr	
		±15		ppm FSR/1000 hr	
Short-Circuit Current		20		mA	
Load	2			kΩ	For specified performance
Capacitive Load Stability			4000	pF	
DC Output Impedance		0.5		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS[3]					DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current			±1	µA	Per pin
Pin Capacitance		5		pF	Per pin
DIGITAL OUTPUTS (SDO)[3]					
Output Low Voltage, V_{OL}			0.4	V	DV_{CC} = 5 V ± 10%, sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} − 1			V	DV_{CC} = 5 V ± 10%, sourcing 200 µA
Output Low Voltage, V_{OL}			0.4	V	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} − 0.5			V	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current			±1	µA	
High Impedance Output Capacitance		5		pF	
POWER REQUIREMENTS					
AV_{DD}	4.5		16.5	V	
AV_{SS}	−4.5		−16.5	V	
DV_{CC}	2.7		5.5	V	
Power Supply Sensitivity[3]					
$\Delta V_{OUT}/\Delta AV_{DD}$		−65		dB	200 mV sine wave superimposed on AV_{SS}/AV_{DD} @ 50 Hz/60 Hz
AI_{DD}			2.5	mA/channel	Outputs unloaded
			1.75	mA/channel	AV_{SS} = 0 V, outputs unloaded
AI_{SS}			2.2	mA/channel	Outputs unloaded
DI_{CC}		0.5	3	µA	$V_{IH} = DV_{CC}$, V_{IL} = GND, 0.5 µA typical
Power Dissipation			310	mW	±16.5 V operation, outputs unloaded
			115	mW	+16.5 V operation, outputs unloaded
Power-Down Currents					All DAC channels and internal reference powered-down
AI_{DD}		40		µA	
AI_{SS}		40		µA	
DI_{CC}		300		nA	

[1] For specified performance, headroom requirement is 0.9 V.
[2] INL is the relative accuracy. It is measured from Code 512, Code 128, Code 32 for the AD5754R, AD5734R, AD5724R respectively.
[3] Guaranteed by characterization; not production tested.
[4] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +85°C.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 4.5 V[1] to 16.5 V, AV_{SS} = −4.5 V[1] to −16.5 V or 0 V, GND = 0 V, REFIN= 2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time		10	12	µs	20 V step to ±0.03 % FSR
		7.5	8.5	µs	10 V step to ±0.03 % FSR
			5	µs	512 LSB step settling (16-bit resolution)
Slew Rate		3.5		V/µs	
Digital-to-Analog Glitch Energy		13		nV-sec	
Glitch Impulse Peak Amplitude		35		mV	
Digital Crosstalk		10		nV-sec	
DAC-to-DAC Crosstalk		10		nV-sec	
Digital Feedthrough		0.6		nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth		15		µV p-p	0x8000 DAC code
100 kHz Bandwidth		80		µV rms	
Output Noise Spectral Density		320		nV/√Hz	Measured at 10 kHz, 0x8000 DAC code

[1] For specified performance, headroom requirement is 0.9 V.
[2] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 4.5 V to 16.5 V, AV_{SS} = −4.5 V to −16.5 V or 0 V, GND = 0 V, REFIN = 2.5 V external, DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 200 pF, all specifications are T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1[4]	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	100	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	0	ns min	Data hold time
t_9	20	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{10}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	10	µs typ	DAC output settling time
t_{13}	20	ns min	$\overline{CLR}$ pulse width low
t_{14}	2.5	µs max	$\overline{CLR}$ pulse activation time
t_{15}[5]	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{16}[5]	40	ns max	SCLK rising edge to SDO valid ($C_{L\,SDO}$[6] = 15 pF)
t_{17}	200	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)

[1] Guaranteed by characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] To accommodate t_{16} , in readback and daisy-chain modes the SCLK cycle time must be increased to 90 ns.
[5] Daisy-chain and readback mode.
[6] $C_{L\,SDO}$ = capacitive load on SDO output.

TIMING DIAGRAMS

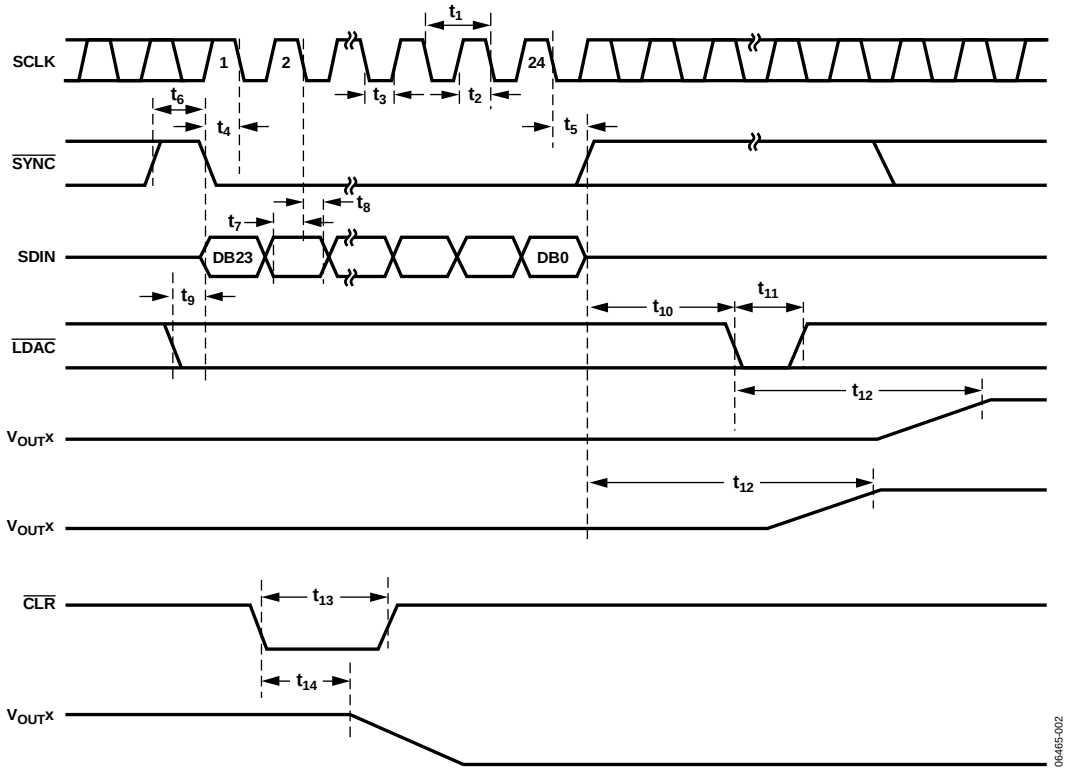

Figure 2. Serial Interface Timing Diagram

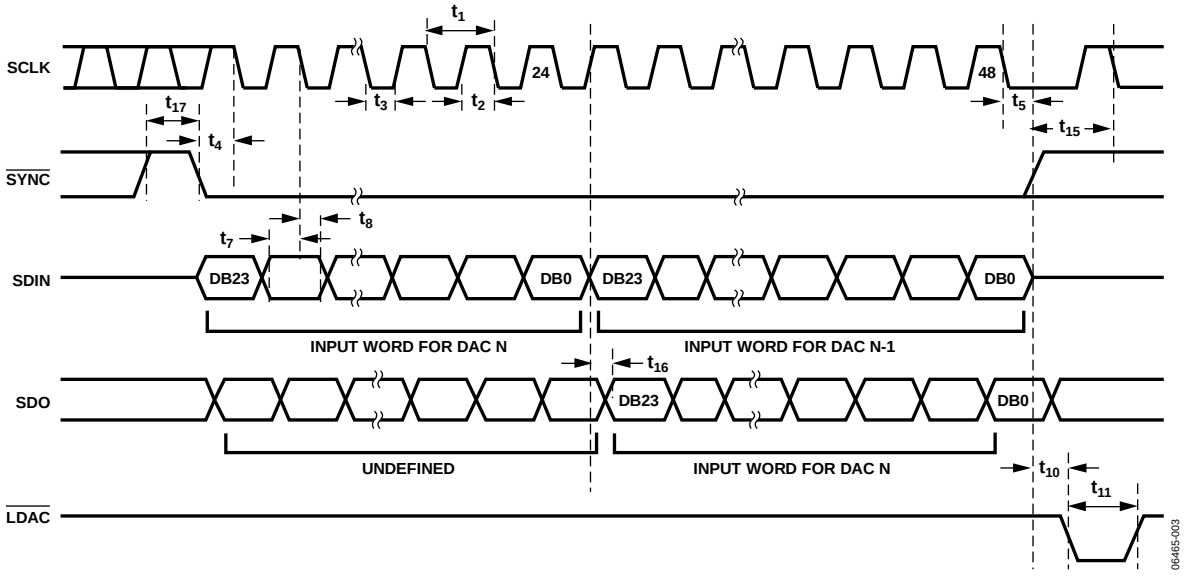

Figure 3. Daisy-Chain Timing Diagram

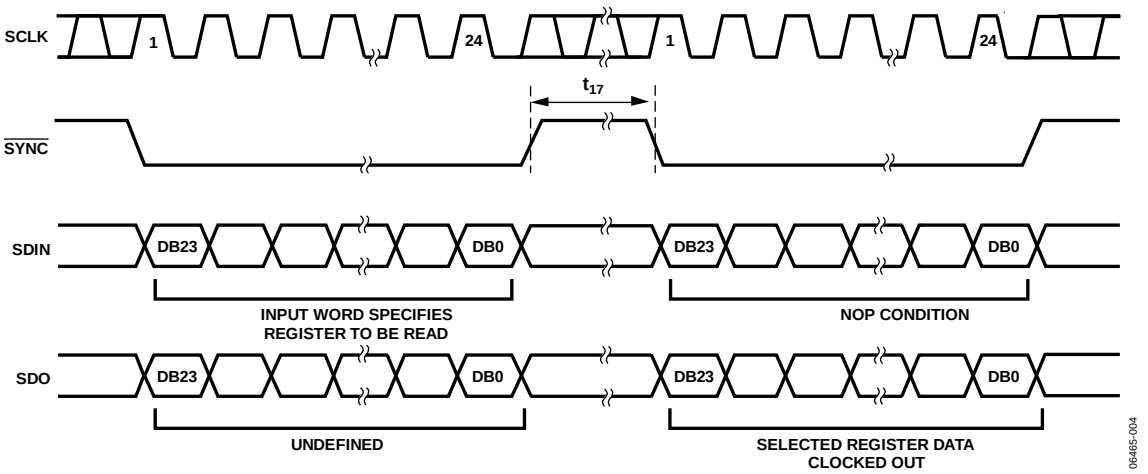

Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +17 V
AV_{SS} to GND	+0.3 V to −17 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +5 V
V_{OUT}x to GND	AV_{SS} to AV_{DD}
DAC_GND to GND	−0.3 V to +0.3 V
SIG_GND to GND	−0.3 V to +0.3 V
Operating Temperature Range, T_A	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, T_J max	105°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	42°C/W
θ_{JC} Thermal Impedance	9°C/W
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

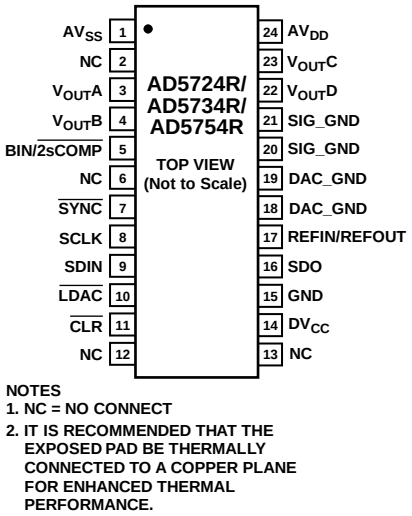

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AV_{SS}	Negative Analog Supply Pin. Voltage range is from –4.5 V to –16.5 V. This pin can be connected to 0 V if output ranges are unipolar.
2, 6, 12, 13	NC	No Connect. Do not connect to these pins.
3	$V_{OUT}A$	Analog Output Voltage of DAC A. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
4	$V_{OUT}B$	Analog Output Voltage of DAC B. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
5	BIN/$\overline{2sCOMP}$	This pin determines the DAC coding for a bipolar output range. This pin should be hardwired to either DV_{CC} or GND. When hardwired to DV_{CC}, input coding is offset binary. When hardwired to GND, input coding is twos complement. (For unipolar output ranges, coding is always straight binary.)
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK. Data is latched on the rising edge of $\overline{SYNC}$.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	$\overline{LDAC}$	Load DAC, Logic Input. This is used to update the DAC registers and, consequently, the analog output. When tied permanently low, the addressed DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the output update is held off until the falling edge of $\overline{LDAC}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
11	$\overline{CLR}$	Active Low Input. Asserting this pin sets the DAC registers to zero-scale code or midscale code (user selectable).
14	DV_{CC}	Digital Supply Pin. Voltage range is from 2.7 V to 5.5 V.
15	GND	Ground Reference Pin.
16	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
17	REFIN/REFOUT	External Reference Voltage Input and Internal Reference Voltage Output. Reference input range is 2 V to 3 V. REFIN = 2.5 V for specified performance. REFOUT = 2.5 V ± 2 mV @ 25°C.
18, 19	DAC_GND	Ground reference pins for the four digital-to-analog converters.
20, 21	SIG_GND	Ground reference pins for the four output amplifiers.
22	$V_{OUT}D$	Analog Output Voltage of DAC D. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
23	$V_{OUT}C$	Analog Output Voltage of DAC C. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
24	AV_{DD}	Positive Analog Supply Pin. Voltage range is from 4.5 V to 16.5 V.
25 (EPAD)	Exposed Paddle (EPAD)	Negative Analog Supply Connection. Voltage range is from –4.5 V to –16.5 V. This paddle can be connected to 0 V if output ranges are unipolar. The paddle can be left electrically unconnected provided that a supply connection is made at the AV_{SS} pin. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

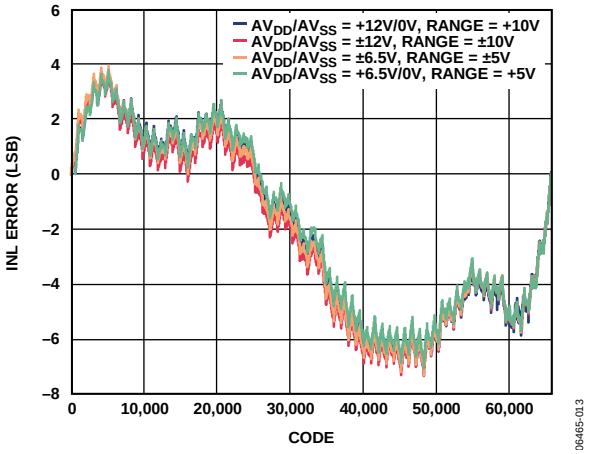

Figure 6. AD5754R Integral Nonlinearity Error vs. Code

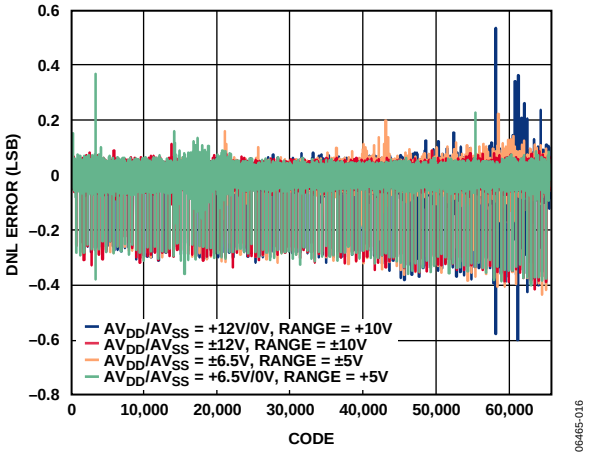

Figure 9. AD5754R Differential Nonlinearity Error vs. Code

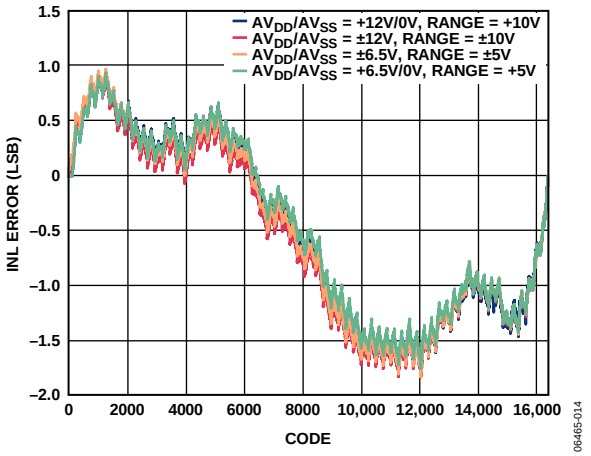

Figure 7. AD5734R Integral Nonlinearity Error vs. Code

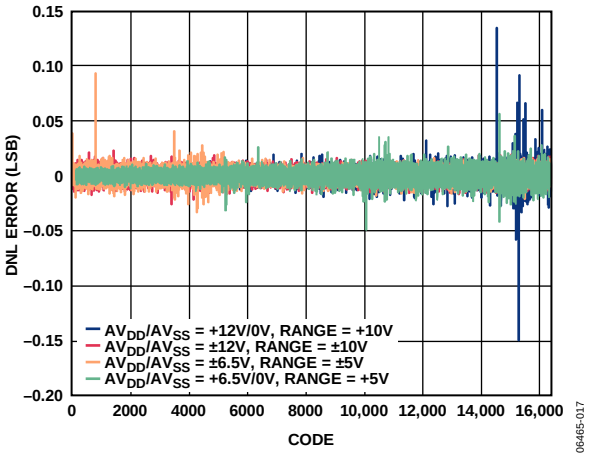

Figure 10. AD5734R Differential Nonlinearity Error vs. Code

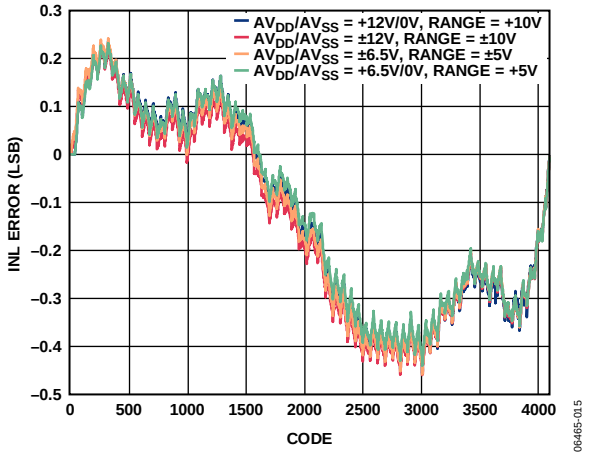

Figure 8. AD5724R Integral Nonlinearity Error vs. Code

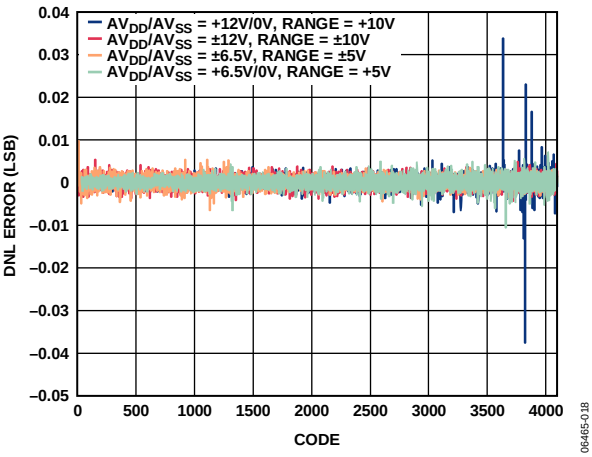

Figure 11. AD5724R Differential Nonlinearity Error vs. Code

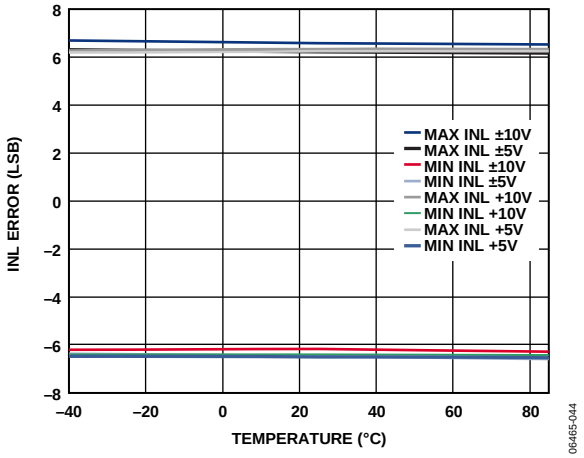

Figure 12. AD5754R Integral Nonlinearity Error vs. Temperature

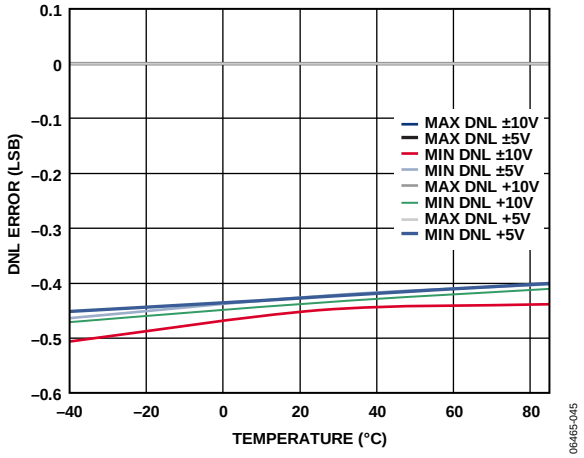

Figure 13. AD5754R Differential Nonlinearity Error vs. Temperature

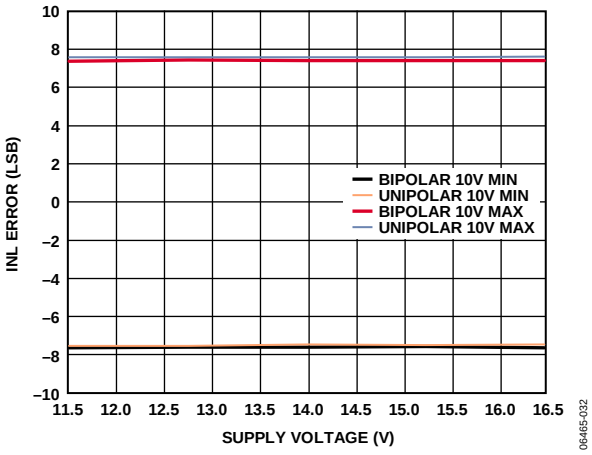

Figure 14. AD5754R Integral Nonlinearity Error vs. Supply Voltage

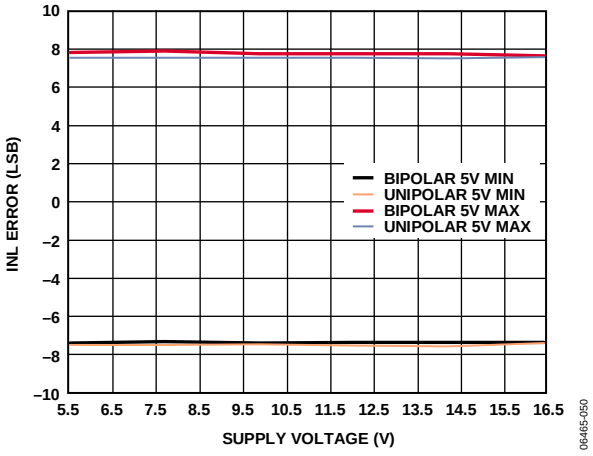

Figure 15. AD5754R Integral Nonlinearity Error vs. Supply Voltage

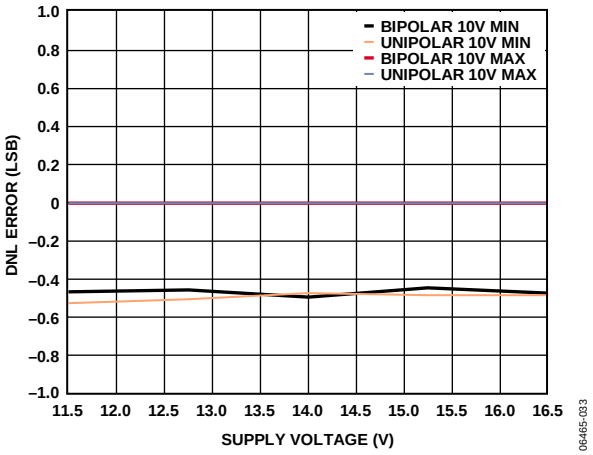

Figure 16. AD5754R Differential Nonlinearity Error vs. Supply Voltage

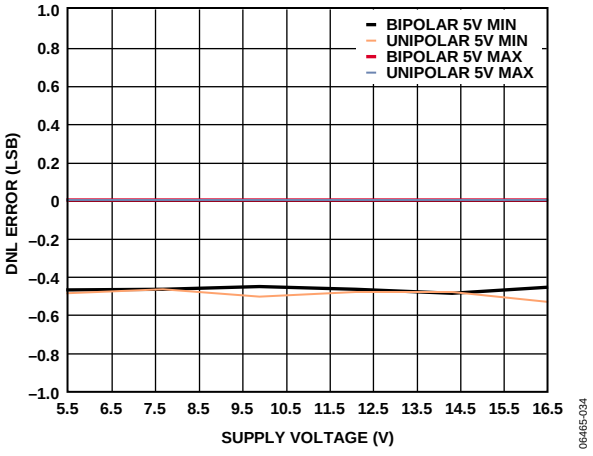

Figure 17. AD5754R Differential Nonlinearity Error vs. Supply Voltage

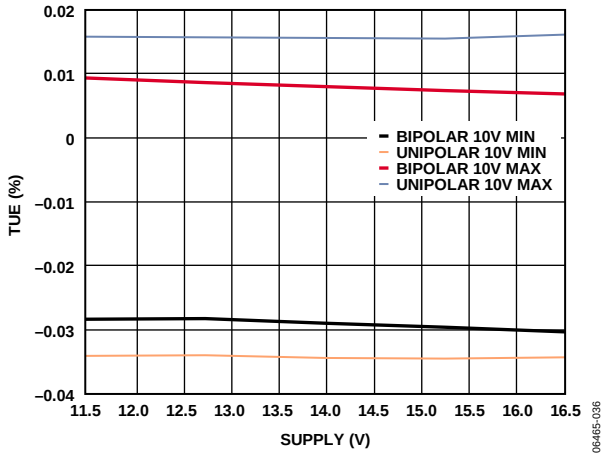

Figure 18. AD5754R Total Unadjusted Error vs. Supply Voltage

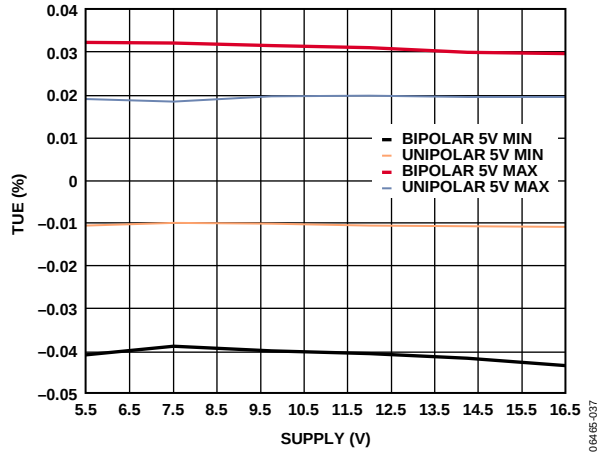

Figure 19. AD5754R Total Unadjusted Error vs. Supply Voltage

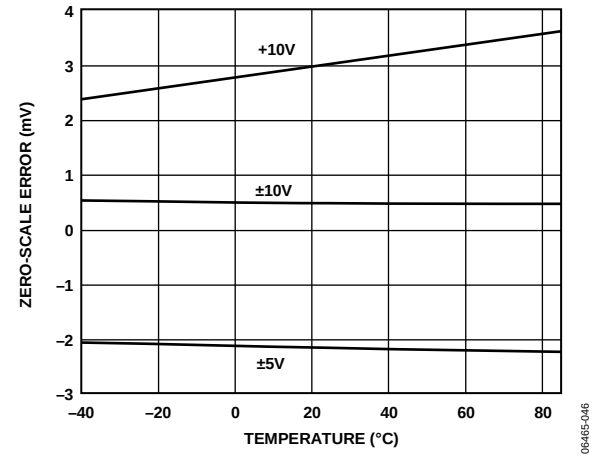

Figure 20. Zero-Scale Error vs. Temperature

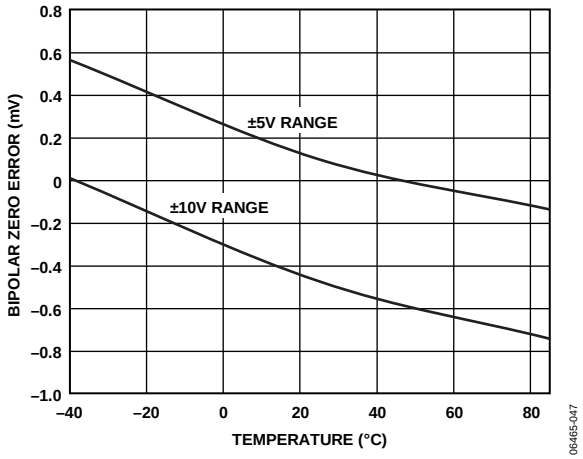

Figure 21. Bipolar Zero Error vs. Temperature

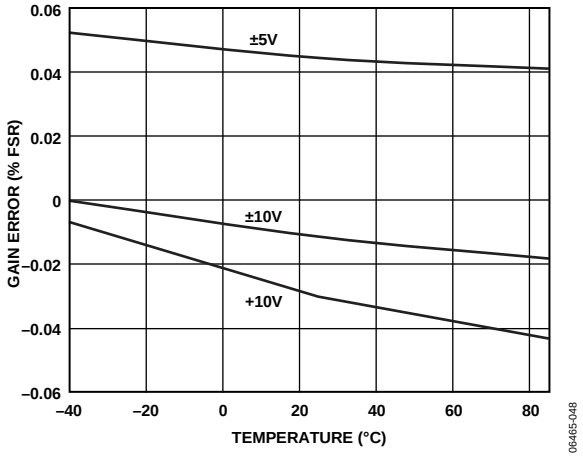

Figure 22. Gain Error vs. Temperature

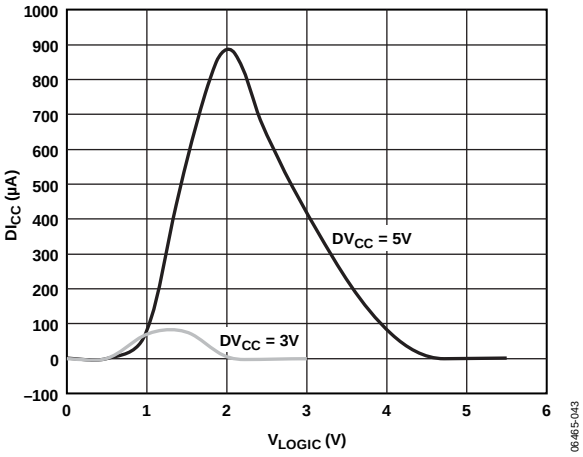

Figure 23. Digital Current vs. Logic Input Voltage

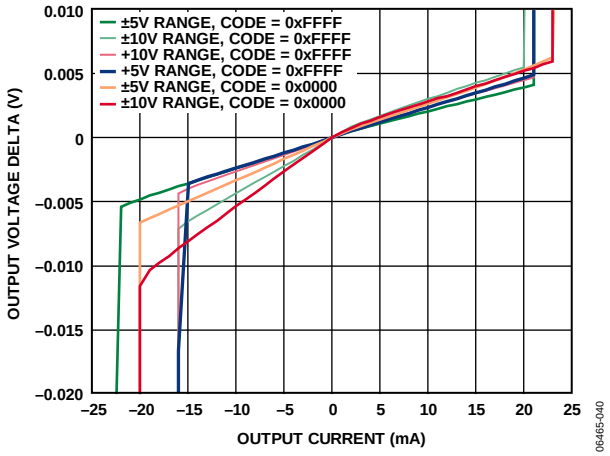

Figure 24. Output Source and Sink Capability

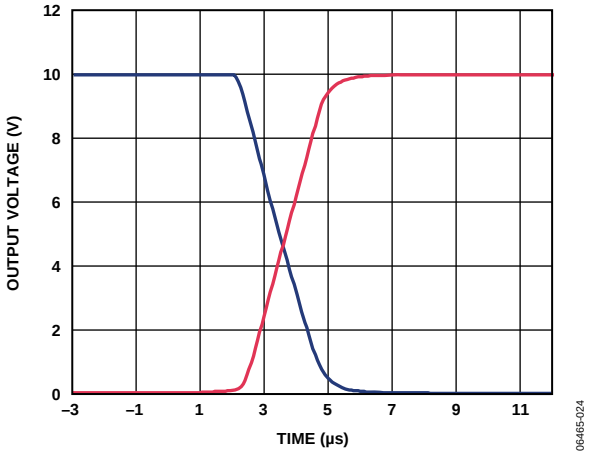

Figure 27. Full-Scale Settling, +10 V Range

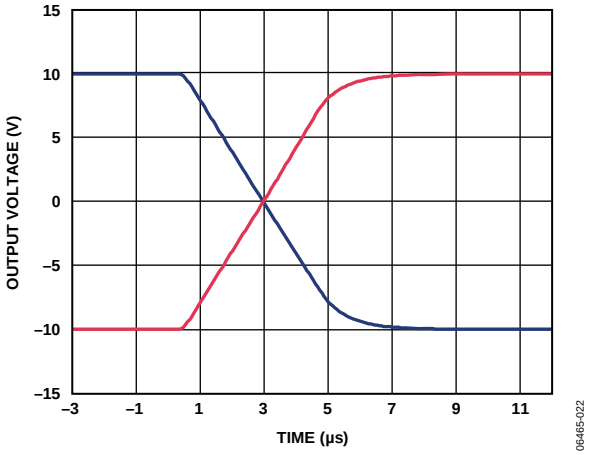

Figure 25. Full-Scale Settling Time, ±10 V Range

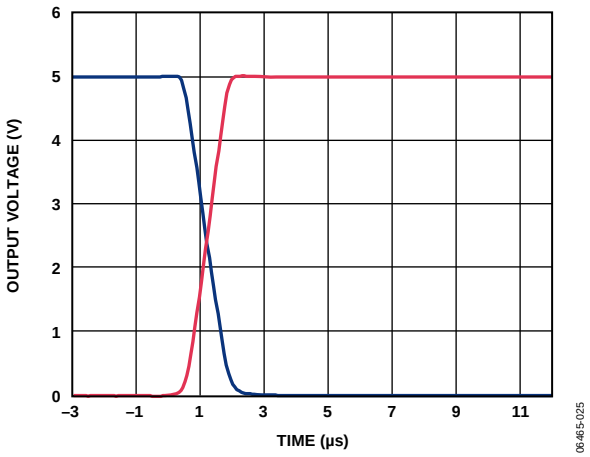

Figure 28. Full-Scale Settling, +5 V Range

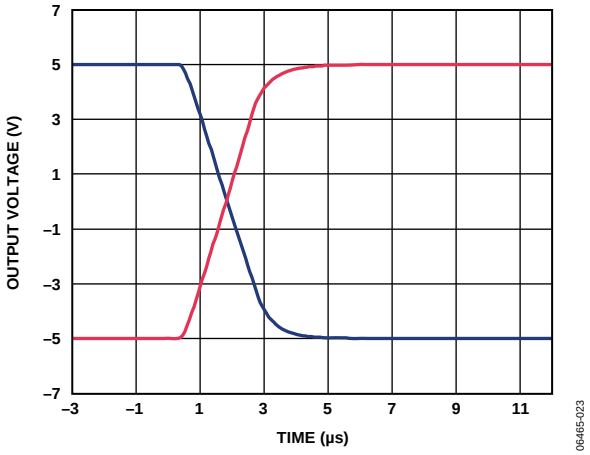

Figure 26. Full-Scale Settling, ±5 V Range

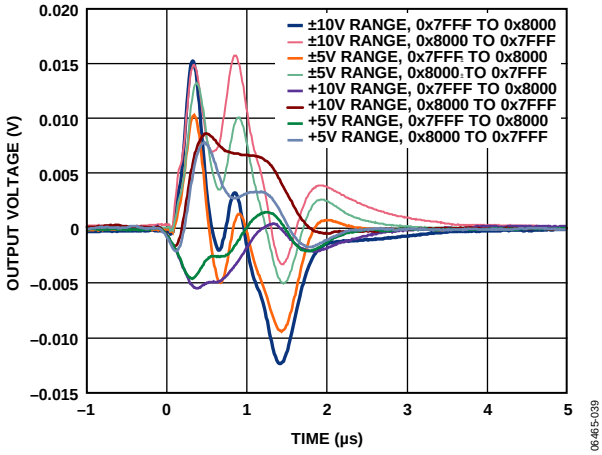

Figure 29. Digital-to-Analog Glitch Energy