Quad, 12-/14-/16-Bit *nano*DACs with 5 ppm/°C On-Chip Reference, I²C Interface

AD5625R/AD5645R/AD5665R, AD5625/AD5665

FEATURES

- Low power, smallest pin-compatible, quad *nano*DACs
- AD5625R/AD5645R/AD5665R
  - 12-/14-/16-bit *nano*DACs
  - On-chip 2.5 V, 5 ppm/°C reference in TSSOP
  - On-chip 1.25 V, 10 ppm/°C reference in LFCSP
- AD5625/AD5665
  - 12-/16-bit *nano*DACs
  - External reference only
- 3 mm × 3 mm 10-lead LFCSP and 14-lead TSSOP
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-on reset to zero scale/midscale
- Per channel power-down
- Hardware $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ functions
- I²C-compatible serial interface supports standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

GENERAL DESCRIPTION

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 members of the *nano*DAC® family are low power, quad, 12-/14-/16-bit, buffered voltage-out DACs with/without an on-chip reference. All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and have an I²C®-compatible serial interface.

The AD5625R/AD5645R/AD5665R have an on-chip reference. The LFCSP versions of the AD56x5R have a 1.25 V, 10 ppm/°C reference, giving a full-scale output range of 2.5 V; the TSSOP versions of the AD56x5R have a 2.5 V, 5 ppm/°C reference giving a full-scale output range of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. The AD5625/AD5665 require an external reference voltage to set the output range of the DAC.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V (POR = GND) or midscale (POR = V_{DD}) and remains there until a valid write occurs. The on-chip precision output amplifier enables rail-to-rail output swing.

FUNCTIONAL BLOCK DIAGRAMS

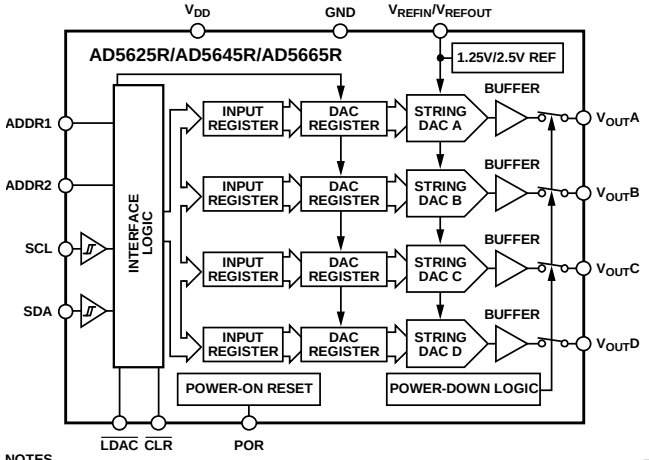

Figure 1. AD5625R/AD5645R/AD5665R

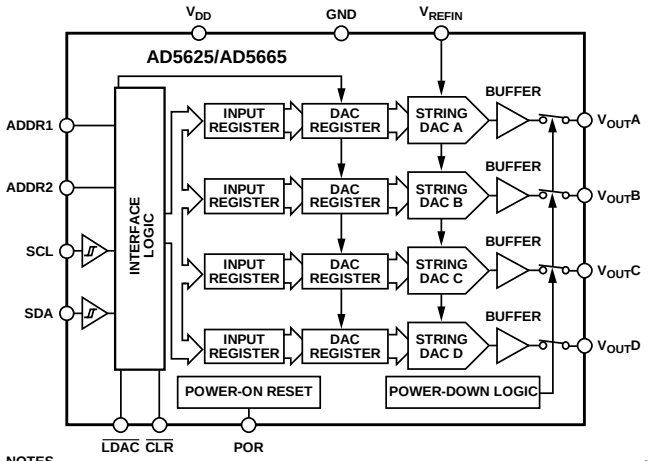

Figure 2. AD5625/AD5665

The AD56x5R/AD56x5 use a 2-wire I²C-compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

Table 1. Related Devices

Part No.	Description
AD5624R/AD5644R/AD5664R, AD5624/AD5664	Quad SPI 12-/14-/16-bit DACs, with/without internal reference.
AD5627R/AD5647R/AD5667R, AD5627/AD5667	Dual I²C 12-/14-/16-bit DACs, with/without internal reference.
AD5666	Quad SPI 16-bit DAC with internal reference.

Rev. A

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3/07—Revision 0: Initial Version

SPECIFICATIONS—AD5665R/AD5645R/AD5625R

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A Grade[1]			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Max**	**Max**	**Unit**	**Conditions/Comments[2]**
STATIC PERFORMANCE[3]								
AD5665R								
Resolution				16			Bits	
Relative Accuracy					±8	±16	LSB	
Differential Nonlinearity						±1	LSB	Guaranteed monotonic by design
AD5645R								
Resolution				14			Bits	
Relative Accuracy					±2	±4	LSB	
Differential Nonlinearity						±0.5	LSB	Guaranteed monotonic by design
AD5625R								
Resolution	12			12			Bits	
Relative Accuracy		±1	±4		±0.5	±1	LSB	
Differential Nonlinearity			±1			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10		±1	±10	mV	
Full-Scale Error		−0.1	±0.5		−0.1	±0.5	% FSR	All 1s loaded to DAC register
Gain Error		±0.1	±1.25		±0.1	±1	% FSR	
Zero-Code Error Drift		±2			±2		µV/°C	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100			−100		dB	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		15			15		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
		8			8		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20			20		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[4]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	Internal reference disabled
	0		2 × V_{REF}			2 × V_{REF}		Internal reference enabled
Capacitive Load Stability		2			2		nF	$R_L = \infty$
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 5 V
Power-Up Time		4			4		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS								
Reference Current		210	260		210	260	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0.75		V_{DD}	0.75		V_{DD}	V	
Reference Input Impedance		26			26		kΩ	
REFERENCE OUTPUT (LFCSP)								
Output Voltage	1.247		1.253	1.247		1.253	V	At ambient
Reference TC[4]		±10			±10		ppm/°C	
Output Impedance		7.5			7.5		kΩ	

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade Min	B Grade Max	B Grade Max	Unit	Conditions/Comments[2]
REFERENCE OUTPUT (TSSOP)								V_{DD} = 4.5 V to 5.5 V
Output Voltage				2.495		2.505	V	At ambient
Reference TC[4]					±5	±10	ppm/°C	
Output Impedance					7.5		kΩ	
LOGIC INPUTS (ADDRx, $\overline{CLR}$, $\overline{LDAC}$, POR)[4]								
I_{IN}, Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.15 × V_{DD}			0.15 × V_{DD}	V	
V_{INH}, Input High Voltage	0.85 × V_{DD}			0.85 × V_{DD}			V	
C_{IN}, Pin Capacitance		2			2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			0.1 × V_{DD}			V	
LOGIC INPUTS (SDA, SCL)[4]								
I_{IN}, Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2			2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			0.1 × V_{DD}			V	High speed mode
	0.05 × V_{DD}			0.05 × V_{DD}			V	Fast mode
LOGIC OUTPUTS (SDA)[4]								
V_{OL}, Output Low Voltage			0.4			0.4	V	I_{SINK} = 3 mA
			0.6			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1			±1	µA	
Floating-State Output Capacitance		2			2		pF	
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	
I_{DD} (Normal Mode)[5]								V_{IH} = V_{DD}, V_{IL} = GND, full-scale loaded
V_{DD} = 4.5 V to 5.5 V		1.0	1.16		1.0	1.16	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		0.9	1.05		0.9	1.05	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		1.9	2.14		1.9	2.14	mA	Internal reference on
V_{DD} = 2.7 V to 3.6 V		1.4	1.59		1.4	1.59	mA	Internal reference on
I_{DD} (All Power-Down Modes)[6]								
V_{DD} = 2.7 V to 5.5 V		0.48	1		0.48	1	µA	V_{IH} = V_{DD}, V_{IL} = GND (LFCSP)
V_{DD} = 3.6 V to 5.5 V		0.48	1		0.48	1	µA	V_{IH} = V_{DD}, V_{IL} = GND (TSSOP)

[1] A grade is offered in AD5625R LFCSP only.
[2] Temperature range of A and B grades is −40°C to +105°C.
[3] Linearity calculated using a reduced code range: AD5665R (Code 512 to Code 65,024), AD5645R (Code 128 to Code 16,256), AD5625R (Code 32 to Code 4064). Output unloaded.
[4] Guaranteed by design and characterization; not production tested.
[5] Interface inactive. All DACs active. DAC outputs unloaded.
[6] All DACs powered down. Power-down function is not available on 14-lead TSSOP parts when the part is powered with V_{DD} < 3.6 V.

SPECIFICATIONS—AD5665/AD5625

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

	B Grade				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments[1]**
STATIC PERFORMANCE[2]					
AD5665					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5625					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±0.5	% FSR	All ones loaded to DAC register
Gain Error		±0.1	±1	% FSR	
Zero-Code Error Drift		±2		µV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		15		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		µV/mA	Due to load current change
		8		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20		µV/mA	Due to load current change
		10		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS					
Reference Current		210	260	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		26		kΩ	
LOGIC INPUTS (ADDRx, $\overline{CLR}$, $\overline{LDAC}$, POR)[4]					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.15 × V_{DD}	V	
V_{INH}, Input High Voltage	0.85 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	
LOGIC INPUTS (SDA, SCL)[4]					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	High speed mode
	0.05 × V_{DD}			V	Fast mode

	B Grade				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments[1]**
LOGIC OUTPUTS (SDA)[4]					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)[4]					$V_{IH} = V_{DD}$, V_{IL} = GND, full-scale loaded
V_{DD} = 4.5 V to 5.5 V		1.0	1.16	mA	
V_{DD} = 2.7 V to 3.6 V		0.9	1.05	mA	
I_{DD} (All Power-Down Modes)[5]					
V_{DD} = 2.7 V to 5.5 V		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (LFCSP)
V_{DD} = 3.6 V to 5.5 V		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (TSSOP)

[1] Temperature range of B grade is −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5665 (Code 512 to Code 65,024), AD5625 (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down. Power-down function is not available on 14-lead TSSOP parts when the part is powered with V_{DD} < 3.6 V.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1,2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time					
AD5625R/AD5625		3	4.5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5645R		3.5	5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5665R/AD5665		4	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/µs	
Digital-to-Analog Glitch Impulse					1 LSB change around major carry
		15		nV-s	LFCSP
		5		nV-s	TSSOP
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-s	
Analog Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
DAC-to-DAC Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical @ 25°C.

I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted.[1]

Table 5.

Parameter	Conditions[2]	Min	Max	Unit	Description
f_{SCL}[3]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode, C_B = 100 pF		3.4	MHz	
	High speed mode, C_B = 400 pF		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode, C_B = 100 pF	60		ns	
	High speed mode, C_B = 400 pF	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode, C_B = 100 pF	160		ns	
	High speed mode, C_B = 400 pF	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode, C_B = 100 pF	0	70	ns	
	High speed mode, C_B = 400 pF	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	

Parameter	Conditions[2]	Min	Max	Unit	Description
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{13}	Standard mode	10		ns	$\overline{\text{LDAC}}$ pulse width low
	Fast mode	10		ns	
	High speed mode	10		ns	
t_{14}	Standard mode	300		ns	Falling edge of ninth SCL clock pulse of last byte of a valid write to $\overline{\text{LDAC}}$ falling edge
	Fast mode	300		ns	
	High speed mode	30		ns	
t_{15}	Standard mode	20		ns	$\overline{\text{CLR}}$ pulse width low
	Fast mode	20		ns	
	High speed mode	20		ns	
t_{SP}[4]	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

[1] See Figure 3. High speed mode timing specification applies only to the AD5625RBRUZ-2/AD5625RBRUZ-2REEL7 and AD5665RBRUZ-2/AD5665RBRUZ-2REEL7.
[2] C_B refers to the capacitance on the bus line.
[3] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[4] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode or less than 10 ns for high speed mode.

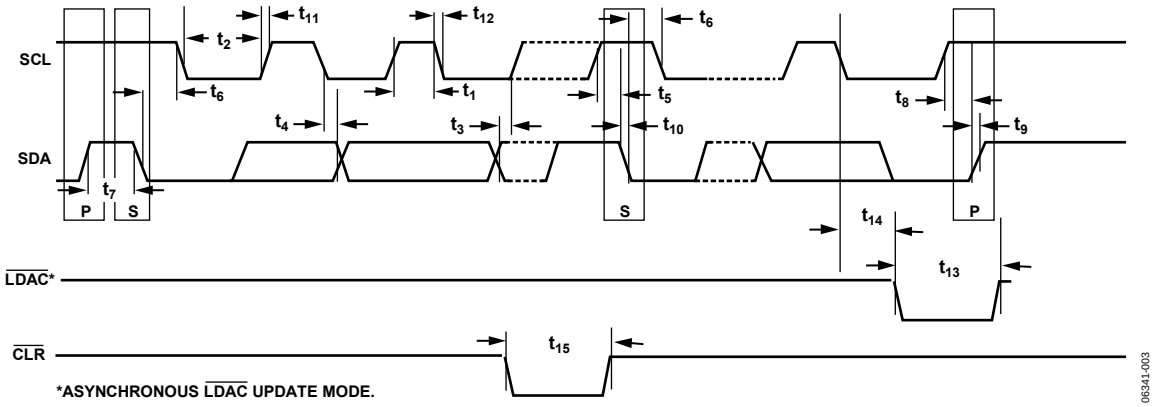

Figure 3. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J maximum)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	
LFCSP_WD (4-Layer Board)	61°C/W
TSSOP	150.4°C/W
Reflow Soldering Peak Temperature, RoHS Compliant	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

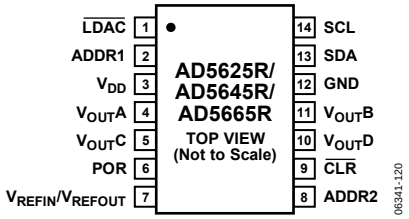

Figure 4. Pin Configuration (14-Lead TSSOP), R Suffix Version

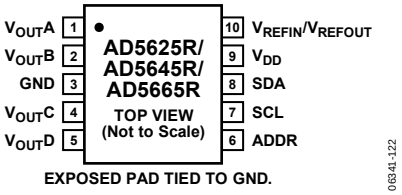

Figure 6. Pin Configuration (10-Lead LFCSP), R Suffix Version

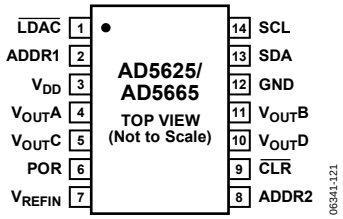

Figure 5. Pin Configuration (14-Lead TSSOP)

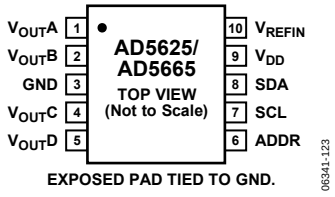

Figure 7. Pin Configuration (10-Lead LFCSP)

Table 7. Pin Function Descriptions

Pin Number			
14-Lead	**10-Lead**	**Mnemonic**	**Description**
1	N/A	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	N/A	ADDR1	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 8).
3	9	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	4	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	N/A	POR	Power-On Reset Pin. Tying the POR pin to GND powers up the part to 0 V. Tying the POR pin to V_{DD} powers up the part to midscale.
7	10	V_{REFIN}/V_{REFOUT}	The AD56x5R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. (The internal reference and reference output are only available on R suffix versions.) The AD56x5 has a reference input pin only.
8	N/A	ADDR2	Three-State Address Input. Sets Bit A3 and Bit A2 of the 7-bit slave address (see Table 9).
9	N/A	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling-edge sensitive. While $\overline{\text{CLR}}$ is low, all LDAC pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the falling edge of the ninth clock pulse of the last byte of the valid write. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted. If $\overline{\text{CLR}}$ is activated during high speed mode, the part exits high speed mode.
10	5	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	3	GND	Ground reference point for all circuitry on the part.
13	8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
14	7	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
N/A	6	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 8).
	EPAD		For the 10-lead version, the exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

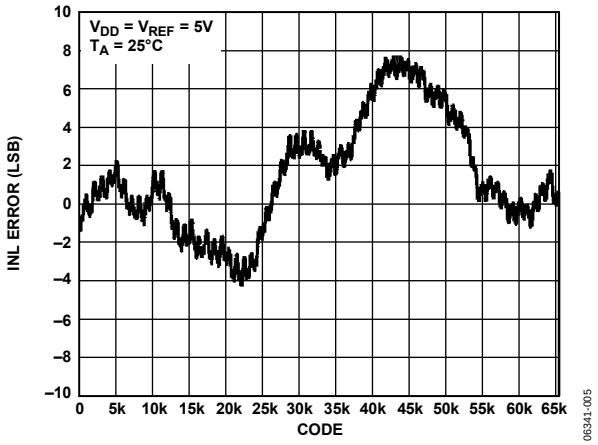

Figure 8. INL AD5665, External Reference

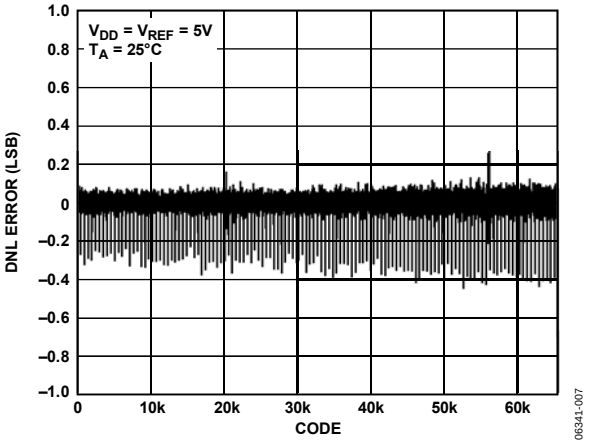

Figure 11. DNL AD5665, External Reference

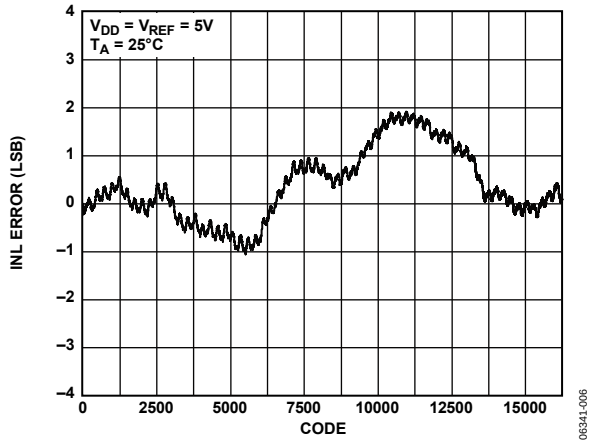

Figure 9. INL AD5645R, External Reference

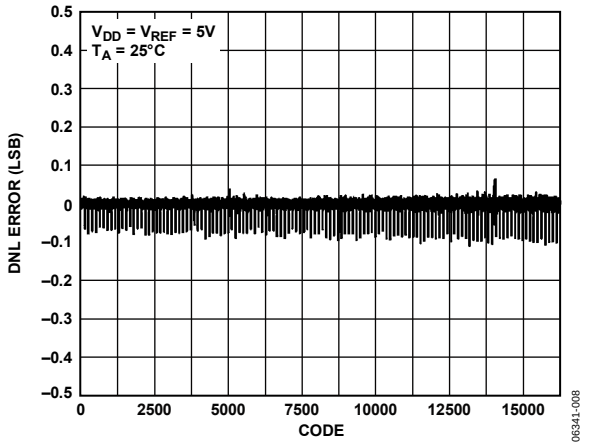

Figure 12. DNL AD5645R, External Reference

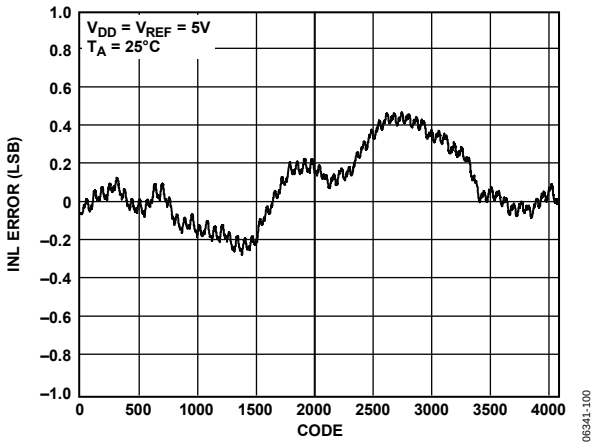

Figure 10. INL AD5625, External Reference

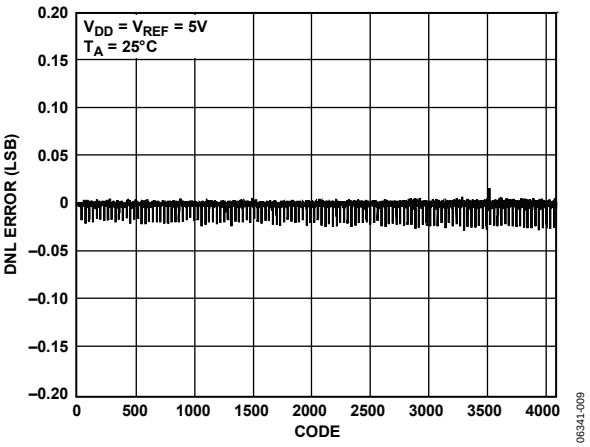

Figure 13. DNL AD5625, External Reference

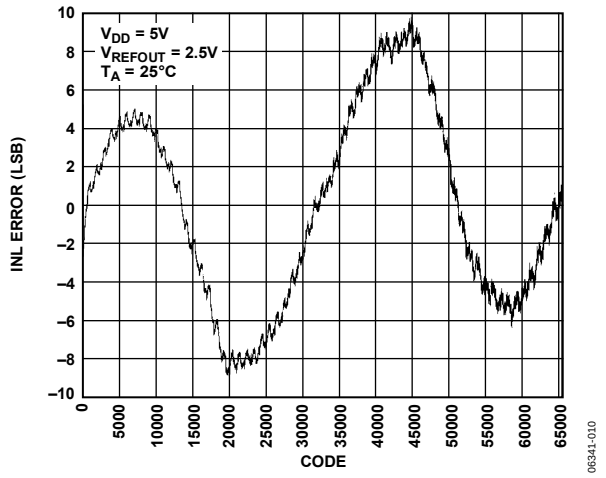

Figure 14. INL AD5665R, 2.5 V Internal Reference

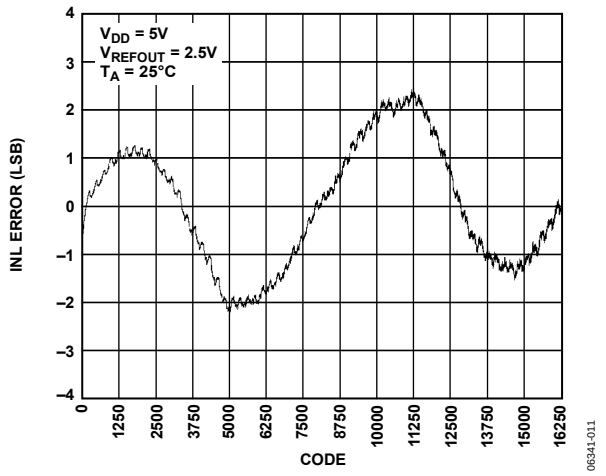

Figure 15. INL AD5645R, 2.5 V Internal Reference

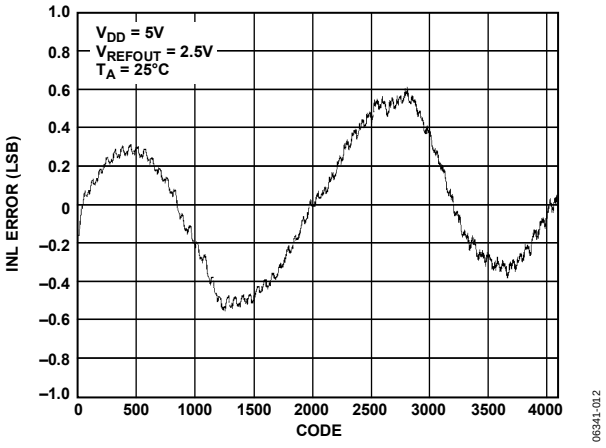

Figure 16. INL AD5625R, 2.5 V Internal Reference

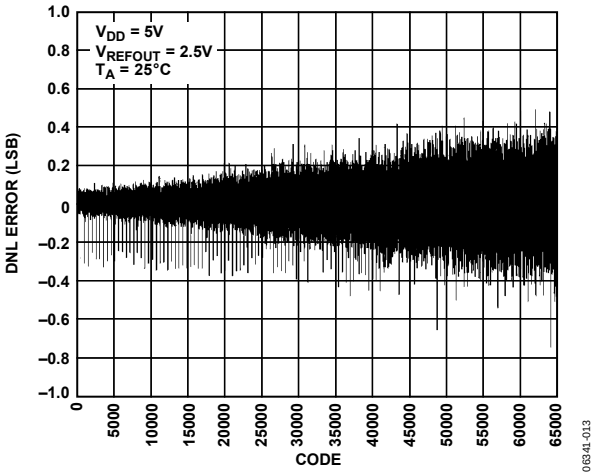

Figure 17. DNL AD5665R, 2.5 V Internal Reference

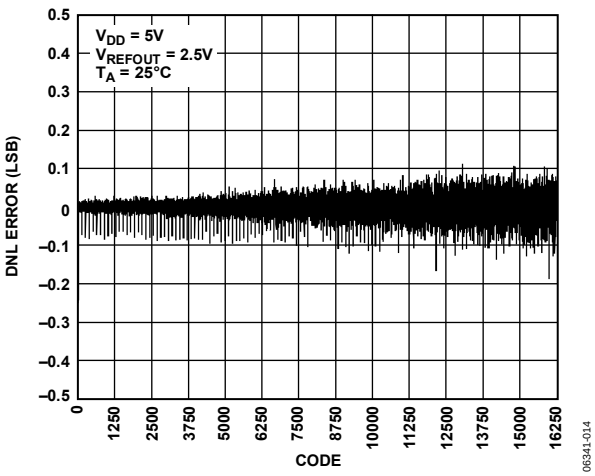

Figure 18. DNL AD5645R, 2.5 V Internal Reference

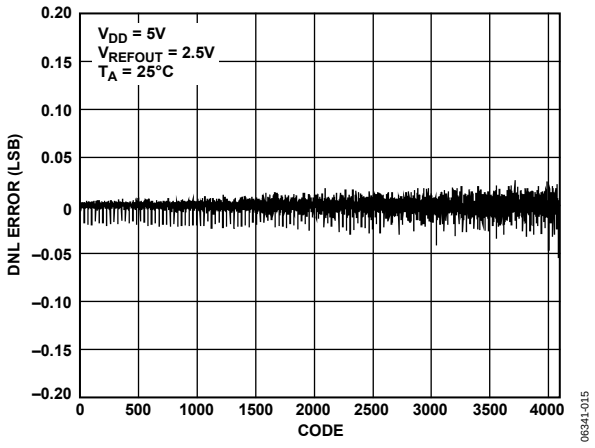

Figure 19. DNL AD5625R, 2.5 V Internal Reference