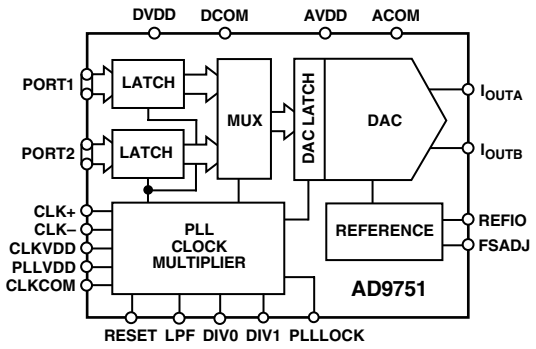
10-Bit, 300 MSPS High Speed TxDAC+® D/A Converter

AD9751*

FEATURES
10-Bit Dual Muxed Port DAC
300 MSPS Output Update Rate
Excellent SFDR and IMD Performance
SFDR to Nyquist @ 25 MHz Output: 64 dB
Internal Clock Doubling PLL
Differential or Single-Ended Clock Input
On-Chip 1.2 V Reference
Single 3.3 V Supply Operation
Power Dissipation: 155 mW @ 3.3 V
48-Lead LQFP

APPLICATIONS
Communications: LMDS, LMCS, MMDS
Base Stations
Digital Synthesis
QAM and OFDM

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9751 is a dual muxed port, ultrahigh speed, single-channel, 10-bit CMOS DAC. It integrates a high quality 10-bit TxDAC+ core, a voltage reference, and digital interface circuitry into a small 48-lead LQFP package. The AD9751 offers exceptional ac and dc performance while supporting update rates up to 300 MSPS.

The AD9751 has been optimized for ultrahigh speed applications up to 300 MSPS where data rates exceed those possible on a single data interface port DAC. The digital interface consists of two buffered latches as well as control logic. These latches can be time multiplexed to the high speed DAC in several ways. This PLL drives the DAC latch at twice the speed of the externally applied clock and is able to interleave the data from the two input channels. The resulting output data rate is twice that of the two input channels. With the PLL disabled, an external 2× clock may be supplied and divided by two internally.

The CLK inputs (CLK+/CLK–) can be driven either differentially or single-ended, with a signal swing as low as 1 V p-p.

The DAC utilizes a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and maximize dynamic accuracy. Differential current outputs support single-ended or differential applications. The differential outputs each provide a nominal full-scale current from 2 mA to 20 mA.

The AD9751 is manufactured on an advanced low cost 0.35 µm CMOS process. It operates from a single supply of 3.0 V to 3.6 V and consumes 155 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9751 is a member of a pin compatible family of high speed TxDAC+s, providing 10-, 12-, and 14-bit resolution.
2. Ultrahigh Speed 300 MSPS Conversion Rate.
3. Dual 10-Bit Latched, Multiplexed Input Ports. The AD9751 features a flexible digital interface allowing high speed data conversion through either a single or dual port input.
4. Low Power. Complete CMOS DAC function operates on 155 mW from a 3.0 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation.
5. On-Chip Voltage Reference. The AD9751 includes a 1.20 V temperature compensated band gap voltage reference.

*Protected by U.S. Patent numbers 5450084, 5568145, 5689257, and 5703519. Other patents pending.

REV. C

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AD9751–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = PLLVDD = CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	10			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	–1	±0.3	+1	LSB
Differential Nonlinearity (DNL)	–0.5	±0.2	+0.5	LSB
ANALOG OUTPUT				
Offset Error	–0.025	±0.01	+0.025	% of FSR
Gain Error (Without Internal Reference)	–5	±0.5	+2	% of FSR
Gain Error (With Internal Reference)	–7	±0.25	+2	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
PLLVDD	3.0	3.3	3.6	V
CLKVDD	3.0	3.3	3.6	V
Analog Supply Current (I_{AVDD})[4]		33	36	mA
Digital Supply Current (I_{DVDD})[4]		3.5	4.5	mA
PLL Supply Current (I_{PLLVDD})[4]		4.5	5.1	mA
Clock Supply Current (I_{CLKVDD})[4]		10.0	11.5	mA
Power Dissipation[4] (3 V, I_{OUTFS} = 20 mA)		155	165	mW
Power Dissipation[5] (3 V, I_{OUTFS} = 20 mA)		216		mW
Power Supply Rejection Ratio[6]—AVDD	–0.1		+0.1	% of FSR/V
Power Supply Rejection Ratio[6]—DVDD	–0.04		+0.04	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at I_{OUTA}, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3]An external buffer amplifier is recommended to drive any external load.
[4]100 MSPS f_{DAC} with PLL on, f_{OUT} = 1 MHz, all supplies = 3.0 V.
[5]300 MSPS f_{DAC}.
[6]±5% power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = CLKVDD = 3.3 V, PLLVDD = 0 V, I_{OUTFS} = 20 mA, Differential Transformer-Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{DAC})	300			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})[1]		1		ns
Glitch Impulse[1]		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (90% to 10%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/$\sqrt{Hz}$
Output Noise (I_{OUTFS} = 2 mA)		30		pA/$\sqrt{Hz}$
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{DAC} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	70	80		dBc
–6 dBFS Output		72		dBc
–12 dBFS Output		72		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 1.1 MHz[2]		73		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 5.1 MHz[2]		73		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 10.1 MHz[2]		72		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 20.1 MHz[2]		68		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 30.1 MHz[2]		64		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 1.1 MHz		74		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 11.1 MHz		71		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 31.1 MHz		66		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 51.1 MHz		66		dBc
f_{DAC} = 200 MSPS; f_{OUT} = 71.1 MHz		63		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 1.1 MHz		74		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 26.1 MHz		71		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 51.1 MHz		66		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 101.1 MHz		66		dBc
f_{DAC} = 300 MSPS; f_{OUT} = 141.1 MHz		63		dBc
Spurious-Free Dynamic Range within a Window				
f_{DAC} = 100 MSPS; f_{OUT} = 1 MHz; 2 MHz Span				
0 dBFS	81	91		dBc
f_{DAC} = 65 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		81		dBc
f_{DAC} = 150 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		81		dBc
Total Harmonic Distortion				
f_{DAC} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS		–80	–69	dBc
f_{DAC} = 65 MHz; f_{OUT} = 2.00 MHz		–72		dBc
f_{DAC} = 150 MHz; f_{OUT} = 2.00 MHz		–72		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)				
f_{DAC} = 65 MSPS; f_{OUT} = 2.00 MHz to 2.77 MHz				
0 dBFS Output		69		dBc
–6 dBFS Output		67		dBc
–12 dBFS Output		65		dBc

NOTES
[1]Measured single-ended into 50 Ω load.
[2]Single-Port Mode (PLL disabled, DIV0 = 1, DIV1 = 0, data on Port 1).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = PLLVDD = CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1	2.1	3		V
Logic 0		0	0.9	V
Logic 1 Current	–10		+10	μA
Logic 0 Current	–10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S), T_A = 25°C	1.0	0.5		ns
Input Hold Time (t_H), T_A = 25°C	1.0	0.5		ns
Latch Pulsewidth (t_{LPW}), T_A = 25°C	1.5			ns
Input Setup Time (t_S, PLLVDD = 0 V), T_A = 25°C	–1.0	–1.5		ns
Input Hold Time (t_H, PLLVDD = 0 V), T_A = 25°C	2.5	1.7		ns
CLK to PLLLOCK Delay (t_D, PLLVDD = 0 V), T_A = 25°C	3.5		4.0	ns
Latch Pulsewidth (t_{LPW} PLLVDD = 0 V), T_A = 25°C	1.5			ns
PLLOCK (V_{OH})	3.0			V
PLLOCK (V_{OL})			0.3	V
CLK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
Min CLK Frequency*		6.25		MHz

*Min CLK Frequency applies only when using internal PLL. When PLL is disabled, there is no minimum CLK frequency.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD, DVDD, CLKVDD, PLLVDD	ACOM, DCOM, CLKCOM, PLLCOM	–0.3	+3.9	V
AVDD, DVDD, CLKVDD, PLLVDD	AVDD, DVDD, CLKVDD, PLLVDD	–3.9	+3.9	V
ACOM, DCOM, CLKCOM, PLLCOM	ACOM, DCOM, CLKCOM, PLLCOM	–0.3	+0.3	V
REFIO, REFLO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–1.0	AVDD + 0.3	V
Digital Data Inputs (DB9 to DB0)	DCOM	–0.3	DVDD + 0.3	V
CLK+/CLK–, PLLLOCK	CLKCOM	–0.3	CLKVDD + 0.3	V
DIV0, DIV1, RESET	CLKCOM	–0.3	CLKVDD + 0.3	V
LPF	PLLCOM	–0.3	PLLVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

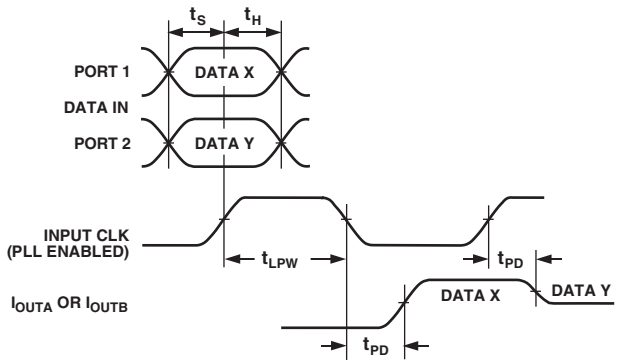


Figure 1. I/O Timing

ORDERING GUIDE

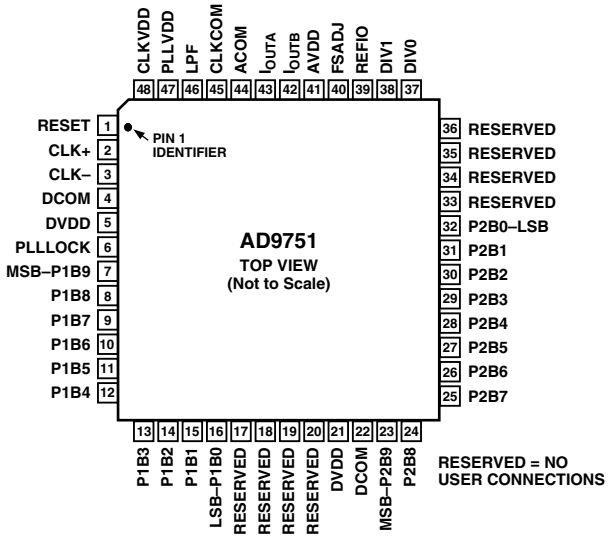
Model	Temperature Range	Package Description	Package Option
AD9751AST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9751ASTRL	–40°C to +85°C	48-Lead LQFP	ST-48
AD9751-EB			Evaluation Board

THERMAL CHARACTERISTIC
Thermal Resistance
θ_{JA} = 91°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9751 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	RESET	Internal Clock Divider Reset
2	CLK+	Differential Clock Input
3	CLK–	Differential Clock Input
4, 22	DCOM	Digital Common
5, 21	DVDD	Digital Supply Voltage
6	PLLLOCK	Phase-Locked Loop Lock Indicator Output
7–16	P1B9–P1B0	Data Bits P1B9 to P1B0, Port 1
17–20, 33–36	RESERVED	
23–32	P2B9–P2B0	Data Bits P2B9 to P2B0, Port 2
37, 38	DIV0, DIV1	Control Inputs for PLL and Input Port Selector Mode; see Tables I and II for details.
39	REFIO	Reference Input/Output
40	FSADJ	Full-Scale Current Output Adjust
41	AVDD	Analog Supply Voltage
42	I_{OUTB}	Differential DAC Current Output
43	I_{OUTA}	Differential DAC Current Output
44	ACOM	Analog Common
45	CLKCOM	Clock and Phase-Locked Loop Common
46	LPF	Phase-Locked Loop Filter
47	PLLVDD	Phase-Locked Loop Supply Voltage
48	CLKVDD	Clock Supply Voltage

TERMINOLOGY

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when the inputs are all 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC cause undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Adjacent Channel Power Ratio (ACPR)
A ratio in dBc between the measured power within a channel relative to its adjacent channel.

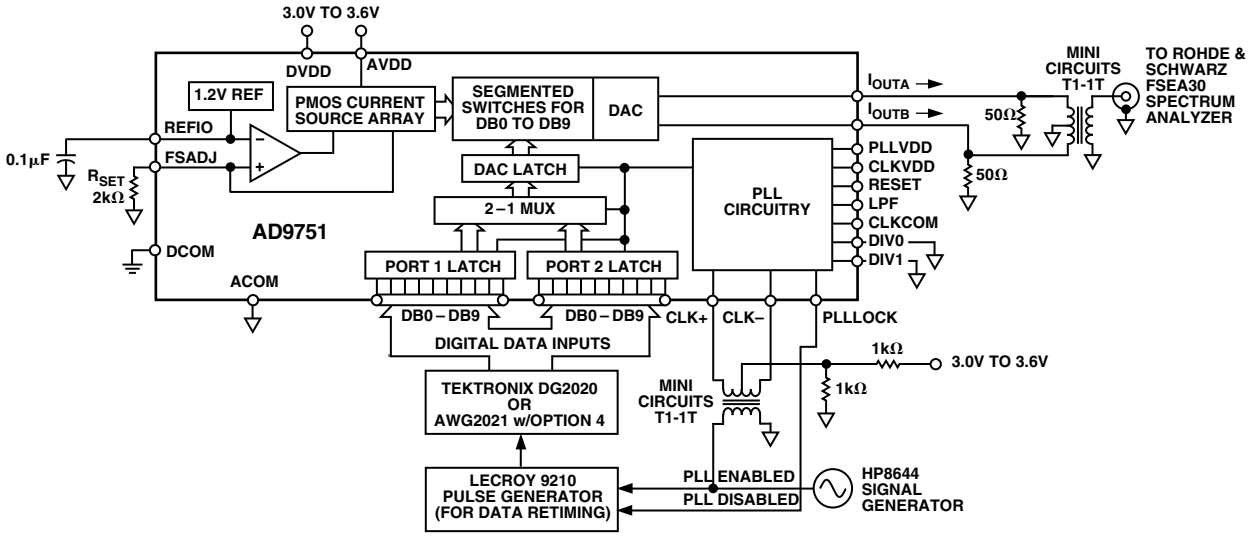
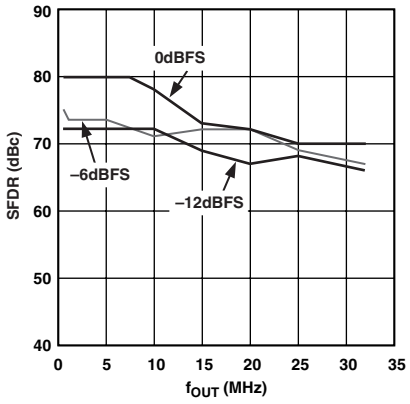
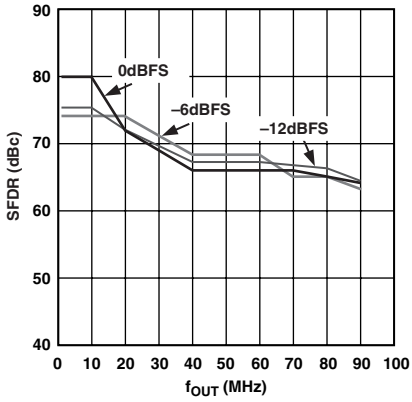


Figure 2. Basic AC Characterization Test Setup

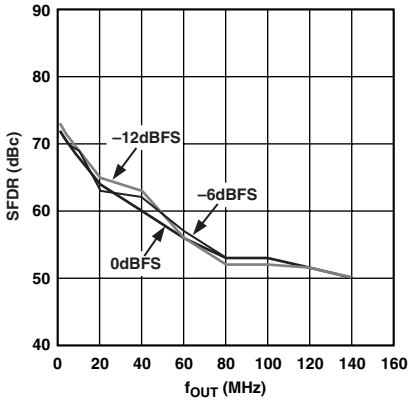
AD9751–Typical Performance Characteristics



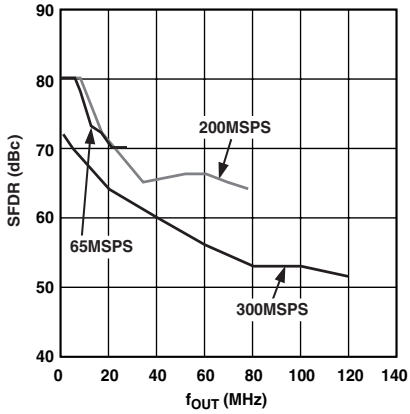
TPC 1. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 65 MSPS; Single Port Mode



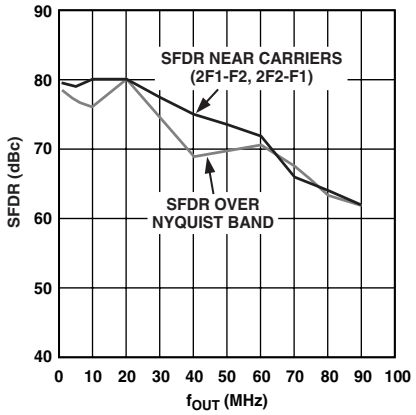
TPC 2. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 200 MSPS



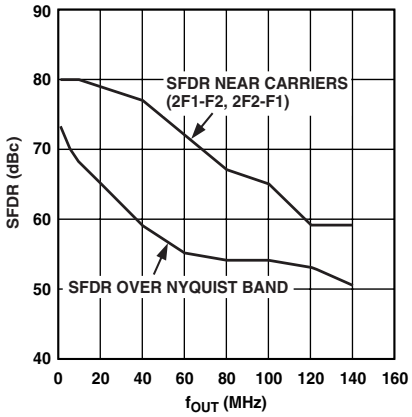
TPC 3. Single-Tone SFDR vs. f_{OUT} @ f_{DAC} = 300 MSPS



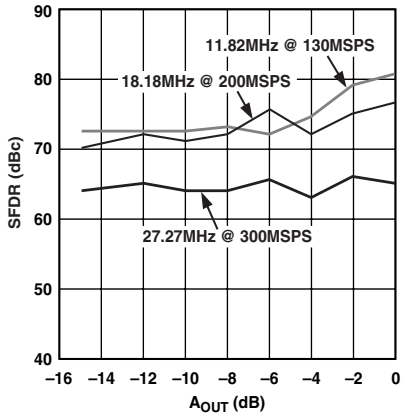
TPC 4. SFDR vs. f_{OUT} @ 0 dBFS



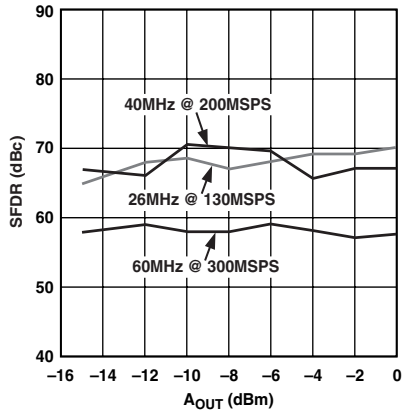
TPC 5. Two-Tone IMD vs. f_{OUT} @ f_{DAC} = 200 MSPS, 1 MHz Spacing between Tones, 0 dBFS



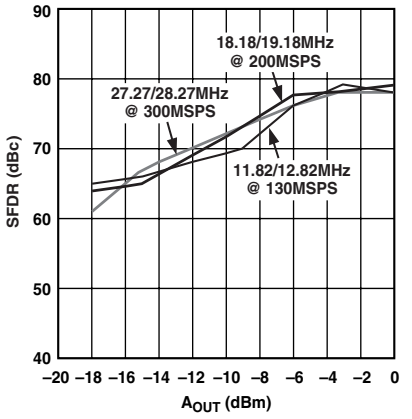
TPC 6. Two-Tone IMD vs. f_{OUT} @ f_{DAC} = 300 MSPS, 1 MHz Spacing between Tones, 0 dBFS



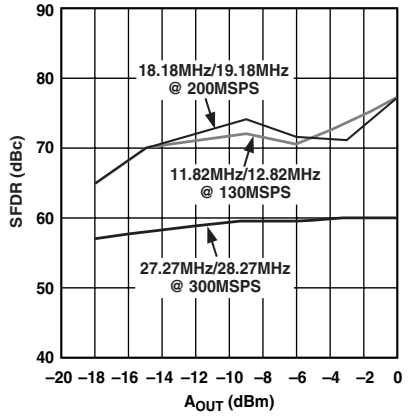
TPC 7. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



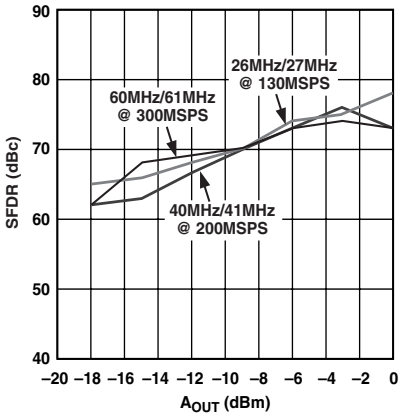
TPC 8. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



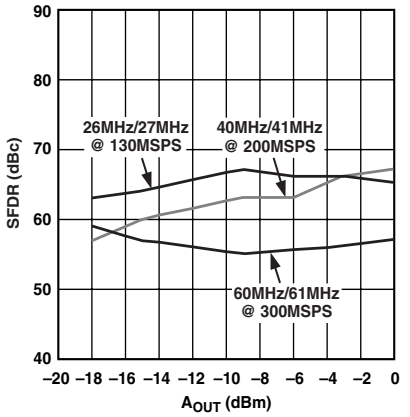
TPC 9. Two-Tone IMD (Third Order Products) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



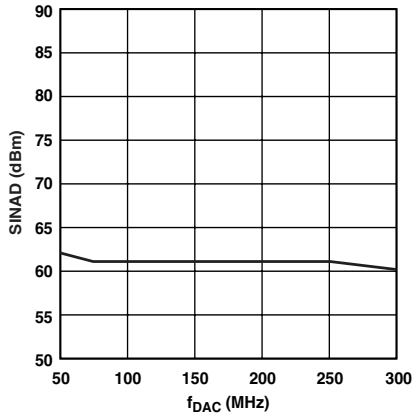
TPC 10. Two-Tone IMD (to Nyquist) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/11$



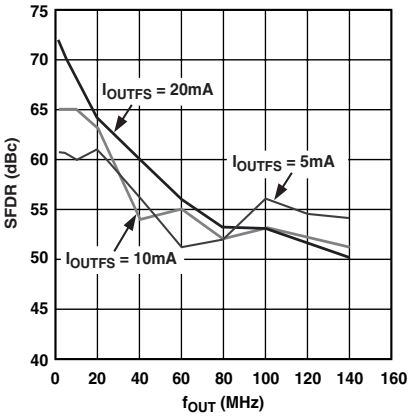
TPC 11. Two-Tone IMD (Third Order Products) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



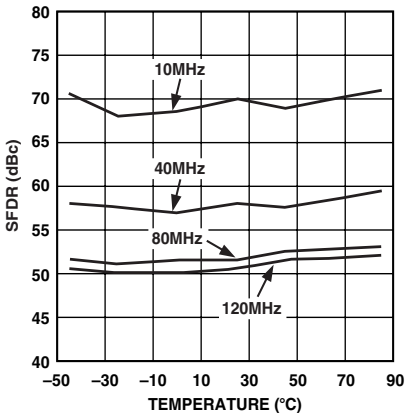
TPC 12. Two-Tone IMD (to Nyquist) vs. A_{OUT} @ $f_{OUT} = f_{DAC}/5$



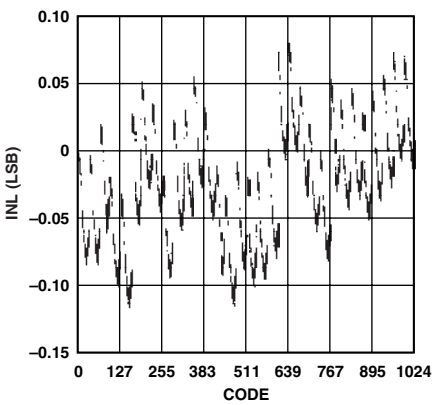
TPC 13. SINAD vs. f_{DAC} @ f_{OUT} = 10 MHz, 0 dBFS



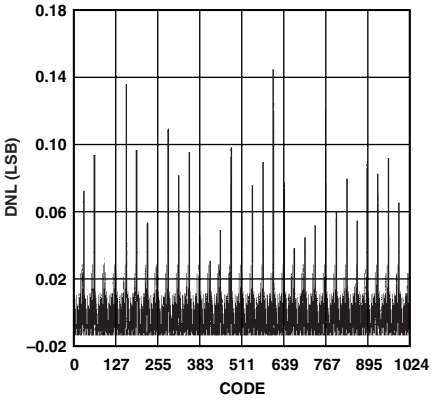
TPC 14. SFDR vs. I_{OUTFS}, f_{DAC} = 300 MSPS @ 0 dBFS



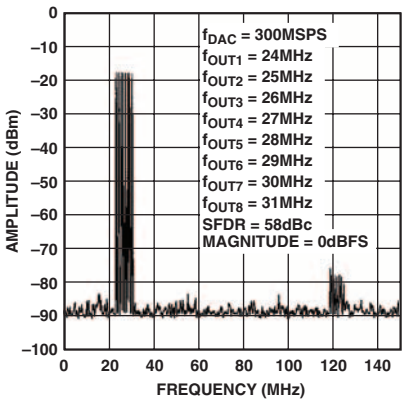
TPC 15. SFDR vs. Temperature, f_{DAC} = 300 MSPS @ 0 dBFS



TPC 16. Typical INL



TPC 17. Typical DNL



TPC 18. Eight-Tone SFDR @ $f_{OUT} \approx f_{DAC}/11$, f_{DAC} = 300 MSPS

FUNCTIONAL DESCRIPTION

Figure 3 shows a simplified block diagram of the AD9751. The AD9751 consists of a PMOS current source array capable of providing up to 20 mA of full-scale current, I_{OUTFS}. The array is divided into 31 equal sources that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSB is a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of the current sources are switched to one or the other of the two outputs (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that significantly improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9751 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 3.0 V to 3.6 V range. The digital section, which is capable of operating at a 300 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V band gap voltage reference, and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times the value of I_{REF}.

REFERENCE OPERATION

The AD9751 contains an internal 1.20 V band gap reference. This can easily be overdriven by an external reference with no effect on performance. REFIO serves as either an *input* or *output*, depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 μF capacitor. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used elsewhere in the circuit, an external buffer amplifier with an input bias current less than 100 nA should be used. An example of the use of the internal reference is shown in Figure 4.

A low impedance external reference can be applied to REFIO, as shown in Figure 5. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 μF compensation capacitor is not required since the internal reference is overdriven, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

REFERENCE CONTROL AMPLIFIER

The AD9751 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a voltage-to-current converter as shown in Figure 4, so that its current output, I_{REF}, is determined by the ratio of V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is applied to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 μA and 625 μA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9751, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low frequency, small signal multiplying applications.

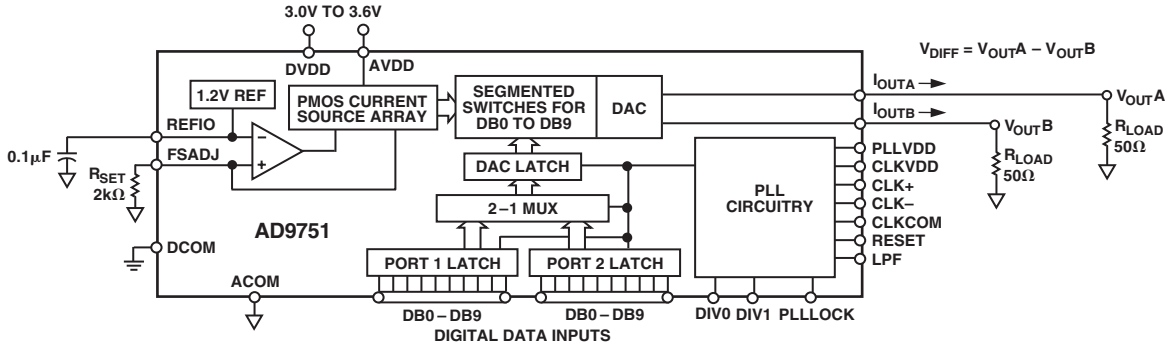


Figure 3. Simplified Block Diagram

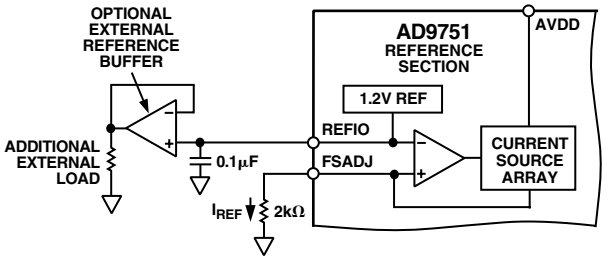


Figure 4. Internal Reference Configuration

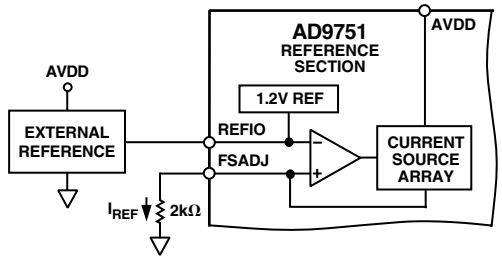


Figure 5. External Reference Configuration

PLL CLOCK MULTIPLIER OPERATION

The Phase-Locked Loop (PLL) is intrinsic to the operation of the AD9751 in that it produces the necessary internally synchronized 2× clock for the edge-triggered latches, multiplexer, and DAC.

With PLLVDD connected to its supply voltage, the AD9751 is in PLL active mode. Figure 6 shows a functional block diagram of the AD9751 clock control circuitry with PLL active. The circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO), input data rate range control, clock logic circuitry, and control input/outputs. The ÷2 logic in the feedback loop allows the PLL to generate the 2× clock needed for the DAC output latch.

Figure 7 defines the input and output timing for the AD9751 with the PLL active. CLK in Figure 7 represents the clock that is generated external to the AD9751. The input data at both Ports 1 and 2 is latched on the same CLK rising edge. CLK may be applied as a single-ended signal by tying CLK– to midsupply and applying CLK to CLK+, or as a differential signal applied to CLK+ and CLK–.

RESET has no purpose when using the internal PLL and should be grounded. When the AD9751 is in PLL active mode, PLLLOCK is the output of the internal phase detector. When locked, the lock output in this mode is Logic 1.

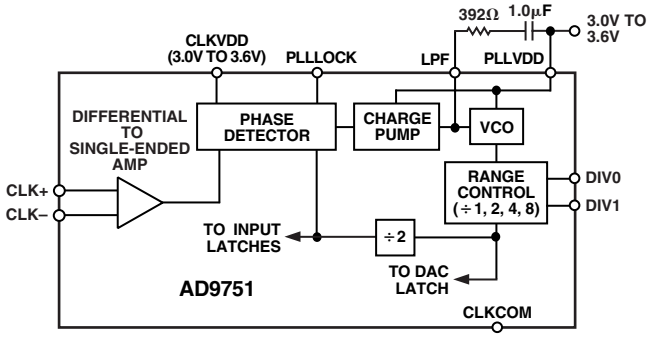
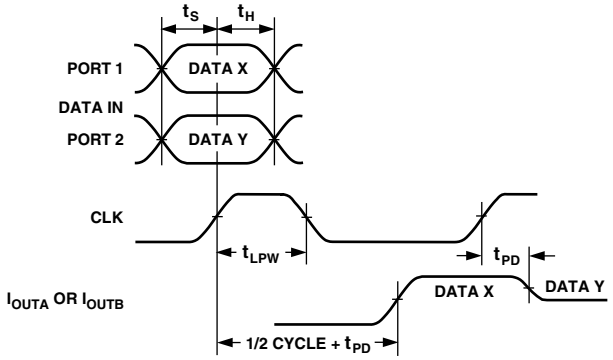


Figure 6. Clock Circuitry with PLL Active



7a. DAC Input Timing Requirements with PLL Active, Single Clock Cycle

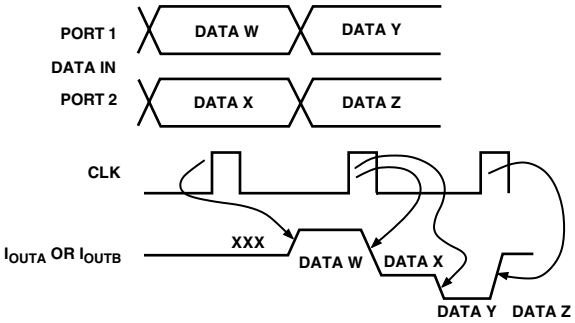


Figure 7b. DAC Input Timing Requirements with PLL Active, Multiple Clock Cycles

Typically, the VCO can generate outputs of 100 MHz to 400 MHz. The range control is used to keep the VCO operating within its designed range while allowing input clocks as low as 6.25 MHz. With the PLL active, logic levels at DIV0 and DIV1 determine the divide (prescaler) ratio of the range controller. Table I gives the frequency range of the input clock for the different states of DIV0 and DIV1.

Table I. CLK Rates for DIV0, DIV1 Levels with PLL Active

CLK Frequency	DIV1	DIV0	Range Controller
50 MHz–150 MHz	0	0	÷1
25 MHz–100 MHz	0	1	÷2
12.5 MHz–50 MHz	1	0	÷4
6.25 MHz–25 MHz	1	1	÷8

A 392 Ω resistor and 1.0 µF capacitor connected in series from LPF to PLLVDD are required to optimize the phase noise versus settling/acquisition time characteristics of the PLL. To obtain optimum noise and distortion performance, PLLVDD should be set to a voltage level similar to DVDD and CLKVDD.

In general, the best phase noise performance for any PLL range control setting is achieved with the VCO operating near its maximum output frequency of 400 MHz.

As stated earlier, applications requiring input data rates below 6.25 MSPS must disable the PLL clock multiplier and provide an external 2× reference clock. At higher data rates however, applications already containing a low phase noise (i.e., jitter) reference clock that is twice the input data rate should consider disabling the PLL clock multiplier to achieve the best SNR performance from the AD9751. Note that the SFDR performance of the AD9751 remains unaffected with or without the PLL clock multiplier enabled.

The effects of phase noise on the AD9751's SNR performance become more noticeable at higher reconstructed output frequencies and signal levels. Figure 8 compares the phase noise of a full-scale sine wave at exactly $f_{DATA}/4$ at different data rates (thus carrier frequency) with the optimum DIV1, DIV0 setting.

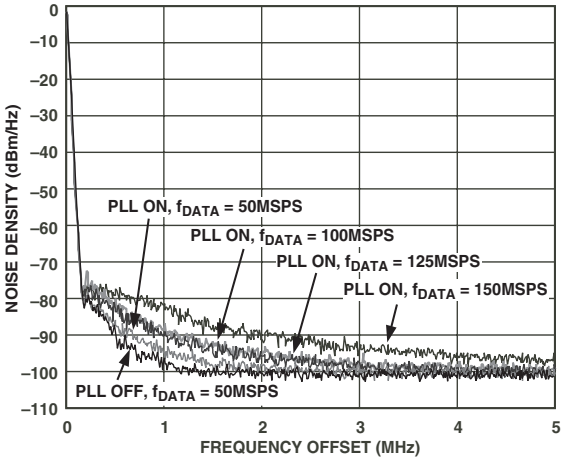


Figure 8. Phase Noise of PLL Clock Multiplier at $f_{OUT} = f_{DATA}/4$ at Different f_{DATA} Settings with DIV0/DIV1 Optimized, Using R&S FSEA30 Spectrum Analyzer, RBW = 30 kHz

SNR is partly a function of the jitter generated by the clock circuitry. As a result, any noise on PLLVDD or CLKVDD may degrade the SNR at the output of the DAC. To minimize this potential problem, PLLVDD and CLKVDD can be connected to DVDD using an LC filter network similar to the one shown in Figure 9.

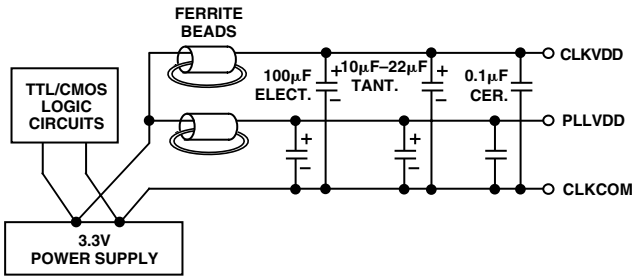


Figure 9. LC Network for Power Filtering

DAC TIMING WITH PLL ACTIVE

As described in Figure 7, in PLL ACTIVE mode, Port 1 and Port 2 input latches are updated on the rising edge of CLK. On the same rising edge, data previously present in the input Port 2 latch is written to the DAC output latch. The DAC output will update after a short propagation delay (t_{PD}).

Following the rising edge of CLK, at a time equal to half of its period, the data in the Port 1 latch will be written to the DAC output latch, again with a corresponding change in the DAC output. Due to the internal PLL, the time at which the data in the Port 1 and Port 2 input latches is written to the DAC latch is independent of the duty cycle of CLK. When using the PLL, the external clock can be operated at any duty cycle that meets the specified input pulsewidth.

On the next rising edge of CLK, the cycle begins again with the two input port latches being updated and the DAC output latch being updated with the current data in the Port 2 input latch.

PLL DISABLED MODE

When PLLVDD is grounded, the PLL is disabled. An external clock must now drive the CLK inputs at the desired DAC output update rate. The speed and timing of the data present at input Ports 1 and 2 is now dependent on whether or not the AD9751 is interleaving the digital input data or only responding to data on a single port. Figure 10 is a functional block diagram of the AD9751 clock control circuitry with the PLL disabled.

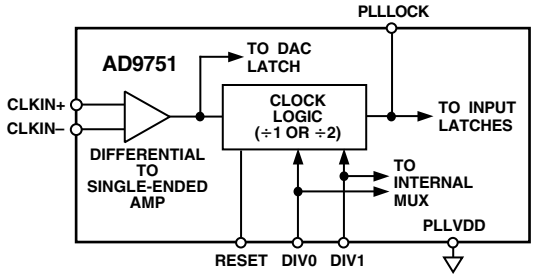


Figure 10. Clock Circuitry with PLL Disabled

DIV0 and DIV1 no longer control the PLL, but are used to set the control on the input mux for either interleaving or not interleaving the input data. The different modes for states of DIV0 and DIV1 are given in Table II.

Table II. Input Mode for DIV0, DIV1 Levels with PLL Disabled

Input Mode	DIV1	DIV0
Interleaved (2×)	0	0
Noninterleaved		
Port 1 Selected	0	1
Port 2 Selected	1	0
Invalid	1	1