# Stellaris® LM3S9B92 RevB1 Errata

This document contains known errata at the time of publication for the Stellaris® LM3S9B92 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

| Erratum Number | Erratum Title | Revision(s) Affected |
|---|---|---|
| 1.1 | JTAG INTEST instruction does not work | B1 |
| 1.2 | The Recover Locked Device sequence does not work | B1 |
| 2.1 | Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled | B1 |
| 2.2 | Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory | B1 |
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| 10.1 | Ethernet receive packet corruption may occur when using optional auto-clock gating | B1 |
| 10.2 | Ethernet packet count decremented before the FCS is read | B1 |
| 10.3 | Ethernet packet loss with cables longer than 50 meters | B1 |
| 10.4 | Ethernet PHY interrupts do not function correctly | B1 |
| 11.1 | USB0ID and USB0VBUS signals are required to be connected regardless of mode | B1 |

| Erratum Number | Erratum Title | Revision(s) Affected |
|---|---|---|
| 11.2 | Latch up may occur if power is applied to the VBUS pin but not to VDD | B1 |
| 12.1 | PWM generation is incorrect with extreme duty cycles | B1 |
| 12.2 | Sync of PWM does not trigger "zero" action | B1 |
| 12.3 | PWM "zero" action occurs when the PWM module is disabled | B1 |
| 12.4 | PWM Enable Update register bits do not function | B1 |
| 13.1 | Power-on event may disrupt operation | B1 |
| 13.2 | Momentarily exceeding $V_{IN}$ ratings on any pin can cause latch-up | B1 |

# 1 JTAG

## 1.1 JTAG INTEST instruction does not work

**Description:**

The JTAG INTEST (Boundary Scan) instruction does not properly capture data.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 1.2 The Recover Locked Device sequence does not work

**Description:**

If software configures any of the JTAG/SWD pins as GPIO or loses the ability to communicate with the debugger, there is a debug sequence that can be used to recover the microcontroller, called the Recover Locked Device sequence. After reconfiguring the JTAG/SWD pins, using the Recover Locked Device sequence does not recover the device.

**Workaround:**

To get the device unlocked, follow these steps:

1. Power cycle the board and run the debug port unlock procedure in LM Flash Programmer. DO NOT power cycle when LM Flash Programmer tells you to.
2. Go to the Flash Utilities tab in LM Flash Programmer and do a mass erase operation (check "Entire Flash" and then click the Erase button). This erase appears to have failed, but that is ok.
3. Power cycle the board.

4. Go to the Flash Utilities tab in LM Flash Programmer and do another mass erase operation (check "Entire Flash" and then click the Erase button).

**Silicon Revision Affected:**

B1

**Fixed:**

Not fixed in Rev C.

# 2 System Control

## 2.1 Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled

**Description:**

If the Cortex-M3 Debug Access Port (DAP) has been enabled, and the device wakes from a low power sleep or deep-sleep mode, the core may start executing code before all clocks to peripherals have been restored to their run mode configuration. The DAP is usually enabled by software tools accessing the JTAG or SWD interface when debugging or flash programming. If this condition occurs, a Hard Fault is triggered when software accesses a peripheral with an invalid clock.

**Workaround:**

A software delay loop can be used at the beginning of the interrupt routine that is used to wake up a system from a WFI (Wait For Interrupt) instruction. This stalls the execution of any code that accesses a peripheral register that might cause a fault. This loop can be removed for production software since the DAP is most likely not enabled during normal execution.

Since the DAP is disabled by default (power on reset), the user can also power cycle the device. The DAP will not be enabled unless it is enabled through the JTAG or SWD interface.

**Silicon Revision Affected:**

B1

**Fixed:**

Will not be fixed.

## 2.2 Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory

**Description:**

Sleep and Deep-Sleep modes cannot be used when running the processor at 66 or 80 MHz when the ISRs and vector table reside in Flash memory. If Sleep or Deep-Sleep mode is used at those speeds, an invalid PC is sometimes returned for the interrupt vector address when exiting sleep mode.

**Workaround:**

There are two possible workarounds for this issue:

1. Store the ISRs and vector table in the on-chip SRAM when running the processor at 66 or 80 MHz.

2. Run the processor at 50 MHz.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 2.3 Device Capabilities registers may not accurately reflect available signals

**Description:**

Some of the Device Capabilities register bits reflect the presence of specific pins on the microcontroller. These bits do not always properly reflect the available signals. Bits affected include **DC3** [31:0], **DC4** [15:14], **DC5** [27:24] and [7:0], and **DC8** [31:0]. Do not rely on the value of these bits in system design.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 3 Internal Memory

## 3.1 Cumulative page erases may introduce bit errors in Flash memory

**Description:**

Cumulative page erases anywhere in the Flash memory array may introduce bit errors. The bit error is not confined to the page being erased or the 4-KB block but could be in any page in the Flash memory. A page erase is used to erase a 1-KB page so it can be rewritten. A mass erase erases the entire Flash memory array (all pages). A bit error means that a bit may change from 0 to 1 or 1 to 0.

**Workaround:**

There are two possible workarounds for this issue:

1. Minimize total page erases to less than 3000 between mass erases for the lifetime of the product. After each mass erase, an additional 3000 page erase operations are allowed before bit errors may be introduced. At the rate of one page erase per week, this issue would not be seen over at least 17 years.

2. Perform CRC checks on all Flash memory after page erases to increase the chances of detecting the issue. The two CRC functions built into ROM can assist in this.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 3.2 Flash Write Buffer does not function above 50 MHz

**Description:**

The Flash Write Buffer does not successfully program the Flash memory at speeds above 50 MHz.

**Workaround:**

Lower the speed of the system clock to 50 MHz or less while programming the Flash memory.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 4 ROM

## 4.1 Ethernet fails to connect when using the Boot loader software in ROM

**Description:**

The Ethernet controller takes longer to connect than the Boot loader software in ROM allows.

**Workaround:**

Download the Boot loader software in the on-chip Flash memory and ensure that the Ethernet connection uses MDI mode only.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 4.2 Some ROM functions are unsupported

**Description:**

The following functions are unsupported in ROM:

- CANBitRateSet
- GPIOPinConfigure
- GPIOPinTypeI2S
- I2CSlaveIntClearEx
- I2CSlaveIntDisableEx
- I2CSlaveIntEnableEx
- I2CSlaveIntStatusEx
- I2SIntClear
- I2SIntDisable

- I2SIntEnable
- I2SIntStatus
- I2SMasterClockSelect
- I2SRxConfigSet
- I2SRxDataGet
- I2SRxDataGetNonBlocking
- I2SRxDisable
- I2SRxEnable
- I2SRxFIFOLevelGet
- I2SRxFIFOLimitGet
- I2SRxFIFOLimitSet
- I2STxConfigSet
- I2STxDataPut
- I2STxDataPutNonBlocking
- I2STxDisable
- I2STxEnable
- I2STxFIFOLevelGet
- I2STxFIFOLimitGet
- I2STxFIFOLimitSet
- I2STxRxConfigSet
- I2STxRxDisable
- I2SRxDataGet
- I2STxRxEnable
- SysCtlDelay
- SysCtlI2SMClkSet
- UARTBusy
- UARTFIFODisable
- UARTFIFOEnable
- UARTRxErrorClear
- UARTRxErrorGet
- UARTTxIntModeGet
- UARTTxIntModeSet
- uDMAChannelSelectDefault
- uDMAChannelSelectSecondary
- uDMAIntClear
- uDMAIntStatus
- USBDevEndpointConfigGet
- USBEndpointDataAvail
- USBEndpointDMAChannel
- USBEndpointDMADisable
- USBEndpointDMAEnable
- USBModeGet
- USBOTGHostRequest

**Workaround:**

Code for these functions is included in the current version of StellarisWare, which can be downloaded from the website at http://www.luminarymicro.com/products/software_updates.html.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 4.3 ROM mapping check for the Boot loader does not function properly

**Description:**

Before the processor is released from the reset state, the System Control module is supposed to check address 0x0000.0004 of Flash memory looking for a reset vector that is not 0xFFFF.FFFF. If an initialized reset vector is found, Flash memory is mapped to address 0x0000.0000, otherwise ROM is mapped to address 0x0000.0000. Currently, the System Control module errantly checks address 0x0000.0008, which is the NMI vector. So, in situations where a valid reset vector (address 0x0000.0004) has been programmed, but the NMI vector has not been programmed, the ROM is errantly mapped to zero preventing the application that is stored in Flash memory from being executed out of reset.

**Workaround:**

Ensure that the NMI vector is always programmed.

**Silicon Revision Affected:**

B1

**Fixed:**

Not fixed in Rev C.

# 5 GPIO

## 5.1 Port B [1:0] pins require external pull-up resistors

**Description:**

The internal pull-up resistors are not effective for the Port B0 and B1 pins.

**Workaround:**

External pull-up resistors must be used on these two pins.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 6 EPI

## 6.1 EPI dual-chip select function does not work

**Description:**

The Dual CSn Configuration mode (CSCFG=0x2) and the ALE with Dual CSn Configuration mode (CSCFG=-x3) controlled by the **EPI Host-Bus 8 Configuration 2 (EPIHB8CFG2)** register do not function. System designs should use ALE Configuration mode (CSCFG=0x0) or CSn Configuration mode (CSCFG=0x1).

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 6.2 EPI Host-Bus 16 mode does not work

**Description:**

The Host-Bus 16 mode (MODE=0x3) controlled by the **EPI Configuration (EPICFG)** register do not function.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 6.3 Clock signal in EPI General-Purpose mode is inverted

**Description:**

The clock signal that is output on the EPI0S31 signal in General-Purpose mode is inverted.

**Workaround:**

Use the opposite edge for timing when designing with this interface.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 7 UART

## 7.1 UART Smart Card (ISO 7816) mode does not function

**Description:**

The UnTX signal does not function correctly as the bit clock in Smart Card mode.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 7.2 When in IrDA mode, the UnRx signal requires configuration even if not used

**Description:**

When in IrDA mode, the transmitter may not function correctly if the UnRx signal is not used.

**Workaround:**

When in IrDA mode, if the application does not require the use of the UnRx signal, the GPIO pin that has the UnRx signal as an alternate function must be configured as the UnRx signal and pulled High.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 8 SSI

## 8.1 An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set

**Description:**

When using the primary µDMA channels with the SSI module, an interrupt is not generated on transmit µDMA completion if the E0T bit (bit 4 of the **SSICR1** register) is enabled.

**Workaround:**

Use the alternate µDMA channels for the SSI module.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 9 I2S

## 9.1 Some bits in the I2SMCLKCFG register do not function

**Description:**

The top 2 bits of the RXI and TXI bit fields in the **I2SMCLKCFG** register do not function (bits [29:28] of RXI and bits [13:12] of TXI). The RXI and TXI fields contain the 10-bit integer input for the receive and transmit clock generator, respectively. The remaining 8 bits in each field function correctly, so most of the possible integer input choices can be used in system design.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 9.2 I²S SCLK signal is inverted in certain modes

**Description:**

When the I²S controller is operating as a receiver in SCLK Master mode, the WS signal is latched on the rising edge of SCLK, not the falling edge. In addition, when the controller is operating as a transmitter in SCLK Slave mode, the data is launched on the rising edge of SCLK, not the falling edge.

**Workaround:**

For the transmitter, there are two possible workarounds for this issue:

1. Ensure that the I2S0TXSCK signal leads the I2S0TXWS signal by at least 4 ns.
2. Configure as I²S mode with DAC in Left-Justified audio format.

For the receiver, ensure that the CODEC is configured as the SCLK master, and the I²S receive module is configured as the SCLK slave.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 10 Ethernet Controller

## 10.1 Ethernet receive packet corruption may occur when using optional auto-clock gating

**Description:**

Ethernet receive packets may be corrupted if the ACG bit in the **Run-Mode Clock Configuration (RCC)** register is set.

**Workaround:**

Do not set the ACG bit in the **RCC** register.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 10.2 Ethernet packet count decremented before the FCS is read

**Description:**

The Number of Packets Register (NPR) decrements in the cycle before the Frame Check Sequence (FCS) is read from the Receive FIFO. As a result, software may incorrectly believe the entire packet has been received when it has not.

**Workaround:**

Use either the DriverLib routine or compare the number of bytes received to the Length field from the Frame to determine when the FIFO is empty.

**Silicon Revision Affected:**

B1

**Fixed:**

Will not be fixed.

## 10.3 Ethernet packet loss with cables longer than 50 meters

**Description:**

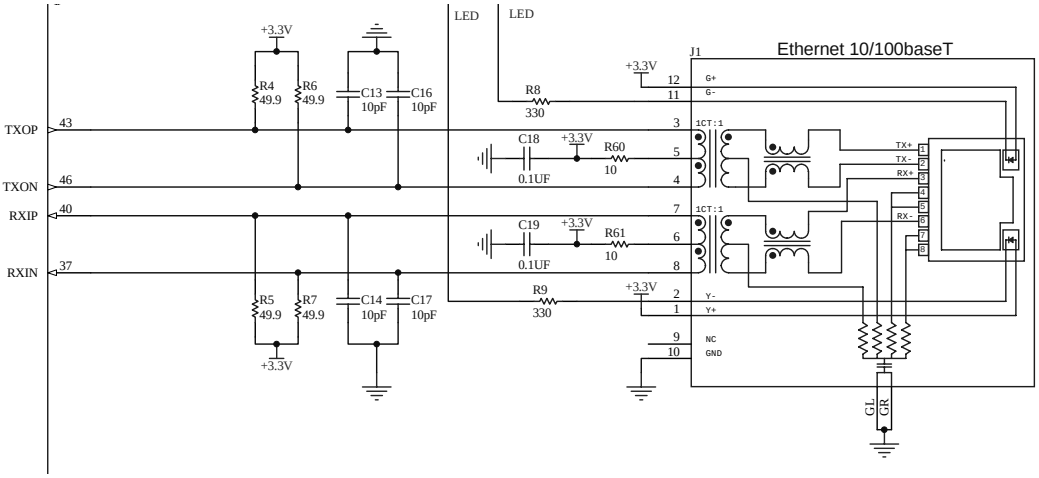
The microcontroller experiences some packet loss with Ethernet cables longer than 50 meters in normal operating conditions.

**Workaround:**

There are two possible workarounds for this issue:

1. Add 10 Ω resistor to the center-tap of the transformer as shown in the figure. These resistors should be replaced by a direct connection for silicon that has this item fixed.
2. Continue using the recommended circuit, but limit cable lengths to 50 meters.

**Figure 1. Recommended Center-Tap Connections**




**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 10.4 Ethernet PHY interrupts do not function correctly

**Description:**

The Ethernet PHY interrupts are not functional. Ethernet PHY interrupts are not necessary for normal Ethernet operation. MAC interrupts are all functional and provide necessary operation.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 11 USB

## 11.1 USB0ID and USB0VBUS signals are required to be connected regardless of mode

**Description:**

The DEVMODOTG bit in the **USB General-Purpose Control and Status (USBGPCS)** register does not function correctly.

**Workaround:**

Connect the USB0VBUS input to VBUS in all modes. In addition, connect the USB0ID pin to ground for Host mode operation and to VDD for Device mode operation using the DEVMOD bit in the **USB General-Purpose Control and Status (USBGPCS)** register.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 11.2 Latch up may occur if power is applied to the VBUS pin but not to VDD

**Description:**

If power is applied to the VBUS pin but not to VDD, the microcontroller may latch up and or draw excessive current. This condition can occur if the microcontroller is unpowered and is connected as a USB device or OTG B.

**Workaround:**

Power up the microcontroller before attaching the USB cable. Also, the USB cable must be detached before powering down the microcontroller.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 12 PWM

## 12.1 PWM generation is incorrect with extreme duty cycles

**Description:**

If a PWM generator is configured for Count-Up/Down mode, and the **PWM Load (PWMnLOAD)** register is set to a value N, setting the compare to a value of 1 or N-1 results in steady state signals instead of a PWM signal. For example, if the user configures PWM0 as follows:

- PWMENABLE = 0x00000001
  - PWM0 Enabled
- PWM0CTL = 0x00000007
  - Debug mode enabled
  - Count-Up/Down mode
  - Generator enabled
- PWM0LOAD = 0x00000063

  - Load is 99 (decimal), so in Count-Up/Down mode the counter counts from zero to 99 and back down to zero (200 clocks per period)

- PWM0GENA = 0x000000b0
  - Output High when the counter matches comparator A while counting up
  - Output Low when the counter matches comparator A while counting down
- PWM0DBCTL = 0x00000000
  - Dead-band generator is disabled

If the **PWM0 Compare A (PWM0CMPA)** value is set to 0x00000062 (N-1), PWM0 should output a 2-clock-cycle long High pulse. Instead, the PWM0 output is a constant High value.

If the **PWM0CMPA** value is set to 0x00000001, PWM0 should output a 2-clock-cycle long negative (Low) pulse. Instead, the PWM0 output is a constant Low value.

**Workaround:**

User software must ensure that when using the PWM Count-Up/Down mode, the compare values must never be 1 or the **PWMnLOAD** value minus one (N-1).

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 12.2 Sync of PWM does not trigger "zero" action

**Description:**

If the **PWM Generator Control (PWM0GENA)** register has the `ActZero` field set to 0x2, then the output is set to 0 when the counter reaches 0, as expected. However, if the counter is cleared by setting the appropriate bit in the **PWM Time Base Sync (PWMSYNC)** register, then the "zero" action is not triggered, and the output is not set to 0.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 12.3 PWM "zero" action occurs when the PWM module is disabled

**Description:**

The zero pulse may be asserted when the PWM module is disabled.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 12.4 PWM Enable Update register bits do not function

**Description:**

The ENUPDn bits in the **PWM Enable Update (PWMENUPD)** register do not function. As a result, enabling the PWM modules can't be synchronized.

**Workaround:**

None.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

# 13 Electrical Characteristics

## 13.1 Power-on event may disrupt operation

**Description:**

Incorrect power sequencing during power up can disrupt operation and potentially cause device failure.

**Workaround:**

$V_{DDC}$ must be applied approximately 50 µs before $V_{DD}$. Normally $V_{DDC}$ is controlled by the part's internal LDO voltage regulator. The workaround requires the addition of an external regulator (see Figure 2) to ensure that $V_{DDC}$ sequencing requirements are met (see Figure 3). Recommended regulators include FAN1112SX (SOT223) and FAN2558S12X (SOT23-5).

This fix mitigates the on-chip power issue, but does not solve it completely. During development, the Flash memory should also be reprogrammed (using LMflash or another programming tool) at least once a week.

**Figure 2. Configuration of External Regulator**

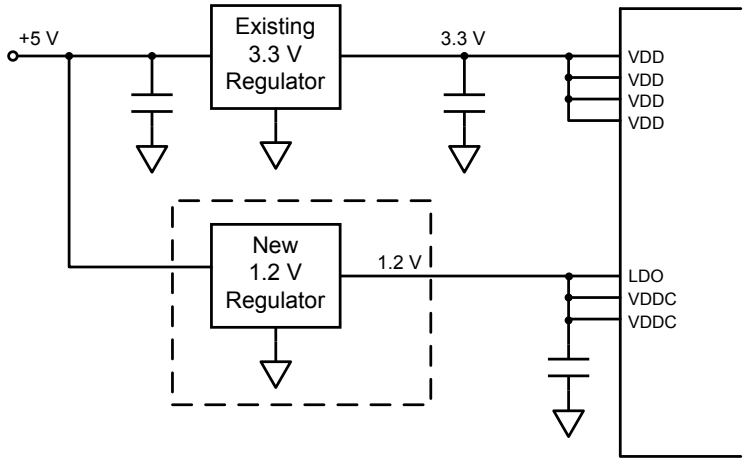
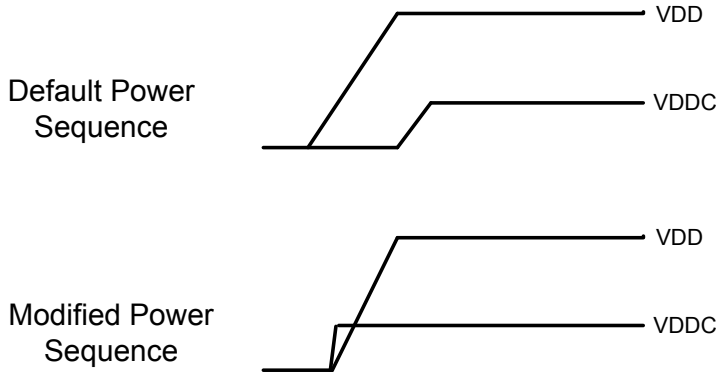



**Figure 3. VDDC Sequencing Requirements**




Detailed characterization is ongoing. Contact the Applications Support Team for the latest information.

**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.

## 13.2 Momentarily exceeding $V_{IN}$ ratings on any pin can cause latch-up

**Description:**

To avoid latch-up, the maximum DC ratings of the part must be strictly enforced. The most common violation of the $V_{IN}$ electrical specification can occur when a mechanical switch or contact is connected directly to a GPIO or special function ($\overline{RST}$, $\overline{WAKE}$, ...) pin. The circuit shown in Figure 4 on page 17 typically has stray inductance and capacitance that can cause a voltage glitch when the switch transitions, as shown in Figure 5 on page 17. The magnitude of the glich may exceed the $V_{IN}$ in the maximum DC ratings table in the Electrical Characteristics chapter. Figure 6 on page 17 shows an improved circuit that eliminates the glitch.

**Figure 4. Incorrect Reset Circuitry**

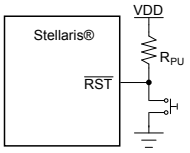
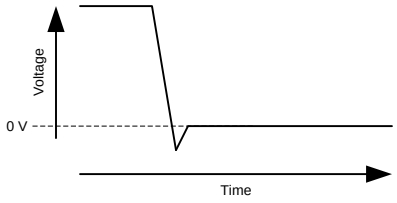



**Figure 5. Excessive Undershoot Voltage on Reset**

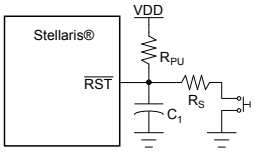



**Workaround:**

Use a circuit as shown in Figure 6 on page 17. In this circuit, $R_S$ should be less than or equal to $R_{PU}/10$. $C_1$ should be matched to $R_{PU}$ to achieve a suitable $t_{RC}$ for the application. Typical values are:

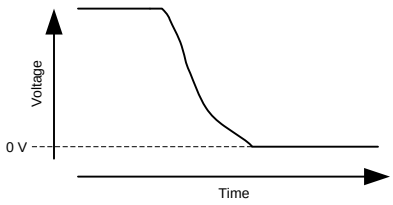
- $R_{PU}$ = 10 kΩ
- $R_S$ = 470 Ω
- $C_1$ = 0.01 µF

**Figure 6. Recommended Reset Circuitry**




After implementing the circuit shown in Figure 6 on page 17, confirm that the voltage on the $\overline{RST}$ input has a curve similar to the one in Figure 7 on page 18, and that the $V_{IN}$ specification is not exceeded.

**Figure 7. Recommended Voltage on Reset**




**Silicon Revision Affected:**

B1

**Fixed:**

Fixed in Rev C.



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