

### FEATURES

- 128 positions
- End-to-end resistance: 5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$
- Ultracompact, SC70-6 (2 mm  $\times$  2.1 mm) package
- I<sup>2</sup>C-compatible interface
- Full read/write of wiper register
- Power-on preset to midscale
- Single-supply 2.7 V to 5.5 V
- Low temperature coefficient: 45 ppm/ $^{\circ}$ C
- Low power, I<sub>DD</sub> = 3  $\mu$ A typical
- Wide operating temperature range: -40 $^{\circ}$ C to +125 $^{\circ}$ C
- Available in Pb-free package
- Evaluation board available

### APPLICATIONS

- Mechanical potentiometer replacement in new designs
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier-biasing
- LCD brightness and contrast adjustment
- Automotive electronics adjustment
- Gain control and offset adjustment

### GENERAL DESCRIPTION

The AD5247 provides a compact, 2 mm  $\times$  2.1 mm, packaged solution for 128-position adjustment applications. This device performs the same electronic adjustment function as a mechanical potentiometer or a variable resistor. Available in four different end-to-end resistance values (5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ ), these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

The wiper settings are controllable through the I<sup>2</sup>C-compatible digital interface, which can also be used to read back the present wiper register control word. The 10 k $\Omega$  and 100 k $\Omega$  options each

### FUNCTIONAL BLOCK DIAGRAM

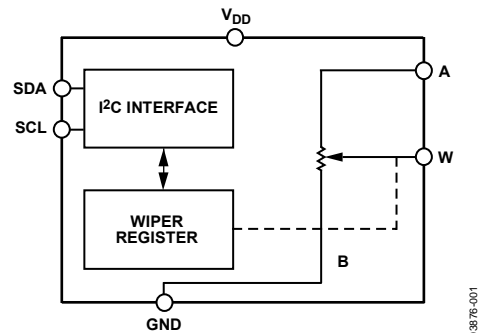


Figure 1.

have three hard-coded slave address options available to allow users access to three of these devices on one I<sup>2</sup>C bus (see Table 8 for a full list of slave address locations).

The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch. Note the terms digital potentiometer, VR (variable resistor), and RDAC are used interchangeably in this document.

Operating from a 2.7 V to 5.5 V power supply and consuming 3  $\mu$ A allows the AD5247 to be used in portable battery-operated applications.

#### Rev. B

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## REVISION HISTORY

### 3/07—Rev. A to Rev. B

Changes to General Description Section .....	1
Added Table 8.....	13
Changes to I <sup>2</sup> C-Compatible 2-Wire Serial Bus Section.....	15
Changes to Ordering Guide .....	18

### 7/06—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Absolute Maximum Ratings section .....	6
Changes to Ordering Guide .....	18

### 9/03—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-4	±0.75	+4	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$		-30		+30	%
Resistance Temperature Coefficient <sup>3</sup>	$\Delta R_{AB}/\Delta T$			45		ppm/°C
Output Resistance	$R_{WB}$	Code = 0x00		75	300	Ω
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE</b>						
Differential Nonlinearity <sup>4</sup>	DNL		-1	±0.1	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error	$V_{WFSE}$	Code = 0x7F	-3	-2	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	1	2	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_A, V_W$		GND		$V_{DD}$	V
Capacitance A <sup>6</sup>	$C_A$	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance W <sup>6</sup>	$C_W$	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	$I_{CM}$	$V_A = V_{DD}/2$		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High	$V_{IH}$	$V_{DD} = 5\text{ V}$	2.4			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5\text{ V}$			0.8	V
Input Logic High	$V_{IH}$	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$			±1	μA
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD\text{ RANGE}}$		2.7		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3	8	μA
Power Dissipation <sup>7</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$			40	μW
Power Supply Sensitivity	PSSR	$V_{DD} = 5\text{ V} \pm 10\%$ , code = midscale		±0.003	±0.05	%/%
<b>DYNAMIC CHARACTERISTICS<sup>5, 8</sup></b>						
Bandwidth -3 dB	BW_5 K	$R_{AB} = 5\text{ k}\Omega$ , code = 0x40		1.2		MHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1\text{ V rms}$ , $V_B = 0\text{ V}$ , $f = 1\text{ kHz}$		0.05		%
$V_W$ Settling Time	$t_s$	$V_A = 5\text{ V}$ , ±1 LSB error band		1		μs
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 2.5\text{ k}\Omega$ , $R_S = 0\ \Omega$		6		nV/√Hz

<sup>1</sup> Typical specifications represent average readings at 25°C and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_A = V_{DD}$ , wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ .

DNL specification limits of ±1 LSB maximum are guaranteed monotonic under operating conditions.

<sup>5</sup> Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design and not subject to production test.

<sup>7</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ . CMOS logic level inputs result in minimum power dissipation.

<sup>8</sup> All dynamic characteristics use  $V_{DD} = 5\text{ V}$ .

ELECTRICAL CHARACTERISTICS—10 k $\Omega$ , 50 k $\Omega$ , AND 100 k $\Omega$  VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1	$\pm 0.1$	+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-2	$\pm 0.25$	+2	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$		-20		+20	%
Resistance Temperature Coefficient <sup>3</sup>	$\Delta R_{AB}/\Delta T$			45		ppm/ $^\circ\text{C}$
Output Resistance	$R_{WB}$	Code = 0x00		75	300	$\Omega$
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity <sup>4</sup>	DNL		-1	$\pm 0.1$	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	$\pm 0.2$	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/ $^\circ\text{C}$
Full-Scale Error (50 k $\Omega$ , 100 k $\Omega$ )	$V_{WFSE}$	Code = 0x7F	-1	-1	0	LSB
Zero-Scale Error (50 k $\Omega$ , 100 k $\Omega$ )	$V_{WZSE}$	Code = 0x00	0	0.4	1	LSB
Full-Scale Error (10 k $\Omega$ )	$V_{WFSE}$	Code = 0x7F	-2	-0.5	0	LSB
Zero-Scale Error (10 k $\Omega$ )	$V_{WZSE}$	Code = 0x00	0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range <sup>5</sup>	$V_A, V_W$		GND		$V_{DD}$	V
Capacitance A <sup>6</sup>	$C_A$	$f = 1\text{ MHz}$ , measured to GND, code = 0x40		45		pF
Capacitance W <sup>6</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = 0x40		60		pF
Common-Mode Leakage	$I_{CM}$	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	$V_{IH}$	$V_{DD} = 5\text{ V}$	2.4			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5\text{ V}$			0.8	V
Input Logic High	$V_{IH}$	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\text{ RANGE}}$		2.7		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3	8	$\mu\text{A}$
Power Dissipation <sup>7</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$			40	$\mu\text{W}$
Power Supply Sensitivity	PSSR	$V_{DD} = 5\text{ V} \pm 10\%$ , code = midscale		$\pm 0.01$	$\pm 0.02$	%/%
DYNAMIC CHARACTERISTICS <sup>6, 8</sup>						
Bandwidth -3 dB	BW	$R_{AB} = 10\text{ k}\Omega/50\text{ k}\Omega/100\text{ k}\Omega$ , code = 0x40		600/100/40		kHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1\text{ V rms}$ , $f = 1\text{ kHz}$ , $R_{AB} = 10\text{ k}\Omega$		0.05		%
$V_W$ Settling Time (10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$ )	$t_s$	$V_A = 5\text{ V} \pm 1\text{ LSB error band}$		2		$\mu\text{s}$
Resistor Noise Voltage Density	$e_{N, WB}$	$R_{WB} = 5\text{ k}\Omega$ , $R_S = 0$		9		nV/ $\sqrt{\text{Hz}}$

<sup>1</sup> Typical specifications represent average readings at  $25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_A = V_{DD}$ , wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of  $\pm 1\text{ LSB}$  maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design, not subject to production test.

<sup>7</sup>  $P_{DISS}$  is calculated from ( $I_{DD} \times V_{DD}$ ). CMOS logic level inputs result in minimum power dissipation.

<sup>8</sup> All dynamic characteristics use  $V_{DD} = 5\text{ V}$ .

**TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS**

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter <sup>1, 2, 3</sup>	Symbol	Min	Typ <sup>4</sup>	Max	Unit
SCL Clock Frequency	$f_{SCL}$			400	kHz
Bus Free Time Between Stop and Start, $t_{BUF}$	$t_1$	1.3			$\mu\text{s}$
Hold Time (Repeated Start), $t_{HD,STA}$ <sup>5</sup>	$t_2$	0.6			$\mu\text{s}$
Low Period of SCL Clock, $t_{LOW}$	$t_3$	1.3			$\mu\text{s}$
High Period of SCL Clock, $t_{HIGH}$	$t_4$	0.6		50	$\mu\text{s}$
Setup Time for Repeated Start Condition, $t_{SU,STA}$	$t_5$	0.6			$\mu\text{s}$
Data Hold Time, $t_{HD,DAT}$	$t_6$			0.9	$\mu\text{s}$
Data Setup Time, $t_{SU,DAT}$	$t_7$	100			ns
Fall Time of Both SDA and SCL Signals, $t_f$	$t_8$			300	ns
Rise Time of Both SDA and SCL Signals, $t_r$	$t_9$			300	ns
Setup Time for Stop Condition, $t_{SU,STO}$	$t_{10}$	0.6			$\mu\text{s}$

<sup>1</sup> Specifications apply to all parts.

<sup>2</sup> Guaranteed by design, not subject to production test.

<sup>3</sup> See timing diagrams (Figure 2, Figure 33, and Figure 34) for locations of measured values.

<sup>4</sup> Typical specifications represent average readings at 25°C and  $V_{DD} = 5\text{ V}$ .

<sup>5</sup> After this period, the first clock pulse is generated.

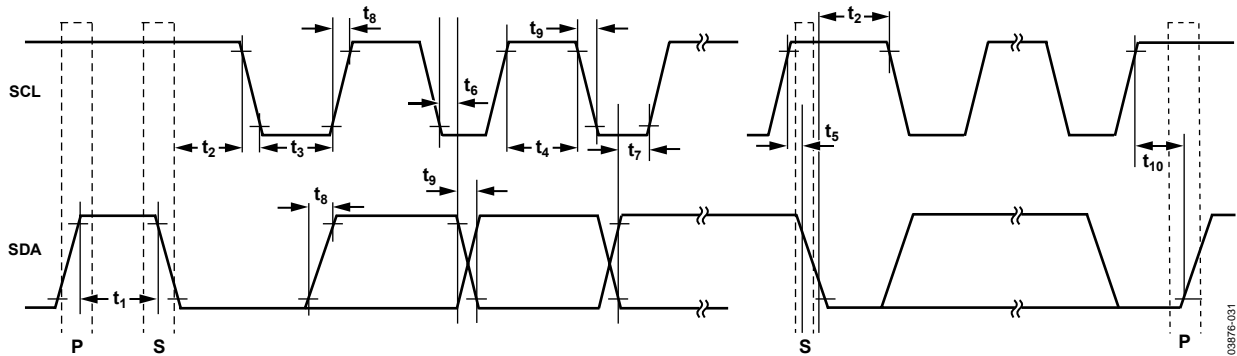


Figure 2. I<sup>2</sup>C Interface, Detailed Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_A$ , $V_W$ to GND	$V_{DD}$
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx	
Pulsed <sup>1</sup>	$\pm 20$ mA
Continuous	$\pm 5$ mA
Digital Inputs and Output Voltage to GND	0 V to $V_{DD} + 0.3$ V
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Maximum Junction Temperature ( $T_{JMAX}$ )	$150^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Thermal Resistance $\theta_{JA}$ <sup>2</sup> : (SC70-6)	$340^\circ\text{C/W}$
Reflow Soldering Peak Temperature	
SnPb	$240^\circ\text{C}$
Pb-Free	$260^\circ\text{C}$

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation =  $(T_{JMAX} - T_A)/\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

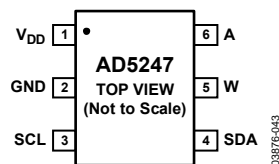


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Positive Power Supply.
2	GND	Digital Ground and B Termination Voltage.
3	SCL	Serial Clock Input; Positive Edge Triggered.
4	SDA	Serial Data Input/Output.
5	W	Terminal W.
6	A	Terminal A.

TYPICAL PERFORMANCE CHARACTERISTICS

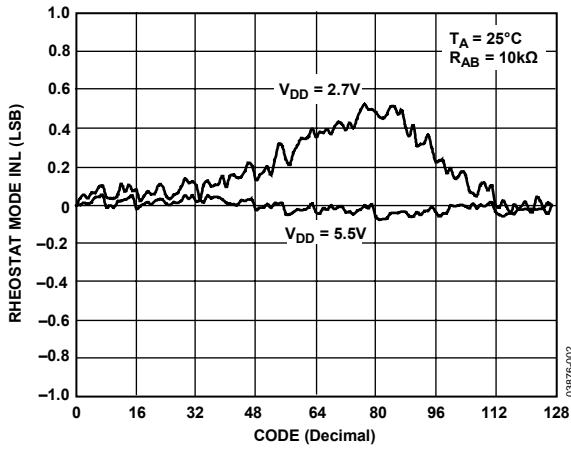


Figure 4. R-INL vs. Code vs. Supply Voltages

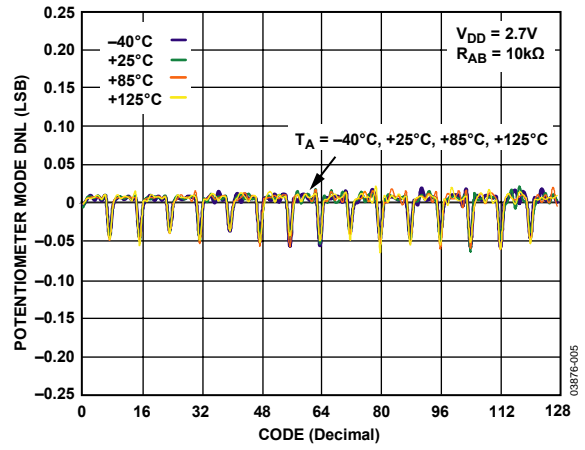


Figure 7. DNL vs. Code vs. Temperature

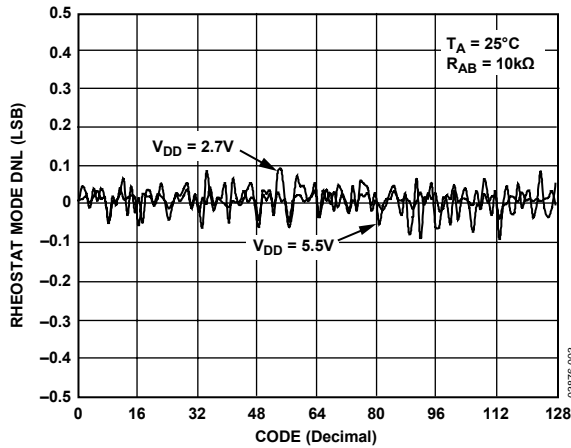


Figure 5. R-DNL vs. Code vs. Supply Voltages

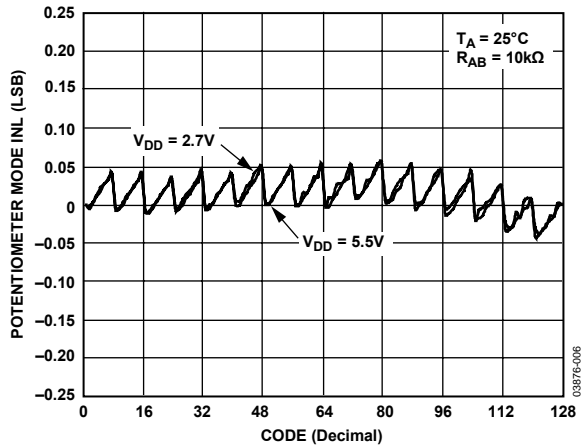


Figure 8. INL vs. Code vs. Supply Voltages

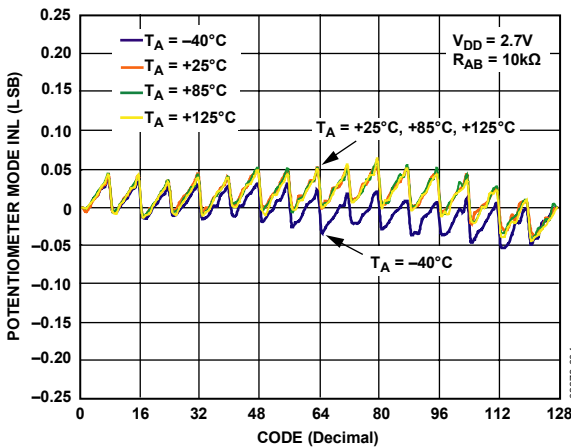


Figure 6. INL vs. Code vs. Temperature

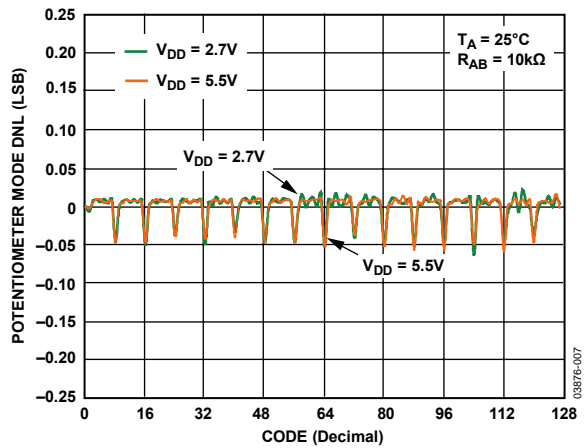


Figure 9. DNL vs. Code vs. Supply Voltages



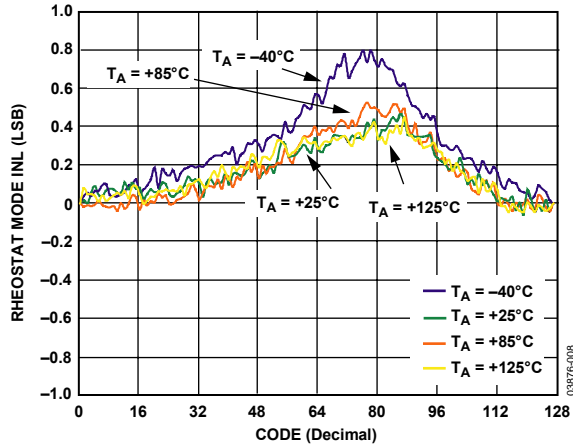


Figure 10. R-INL vs. Code vs. Temperature

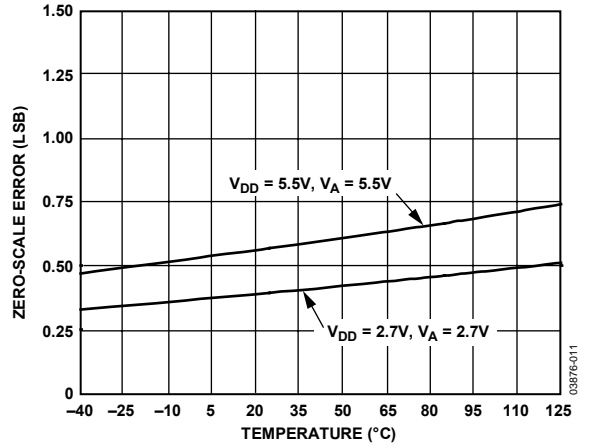


Figure 13. Zero-Scale Error vs. Temperature

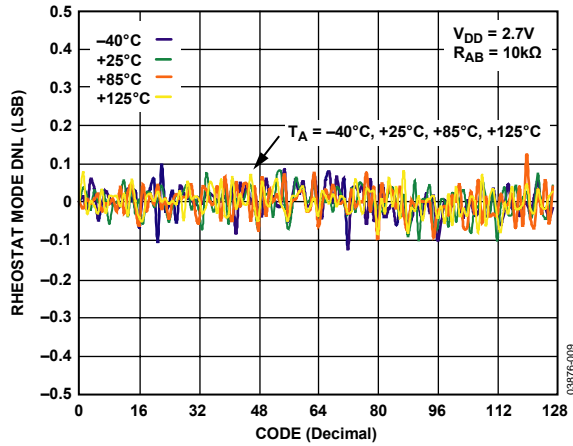


Figure 11. R-DNL vs. Code vs. Temperature

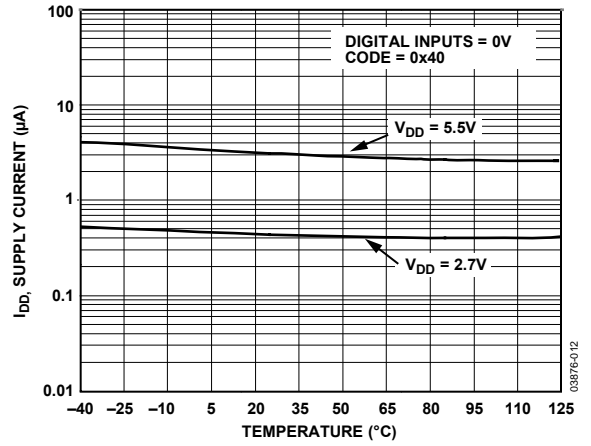


Figure 14. Supply Current vs. Temperature

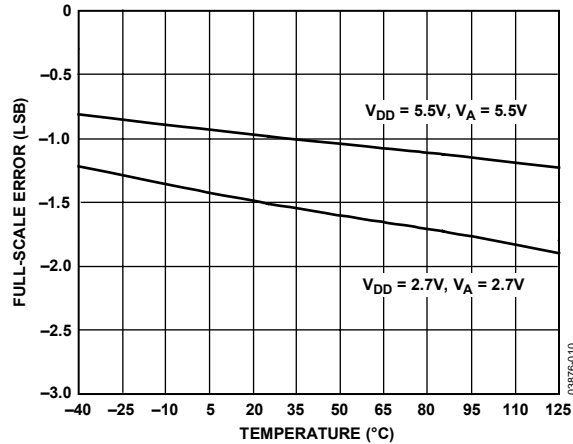


Figure 12. Full-Scale Error vs. Temperature

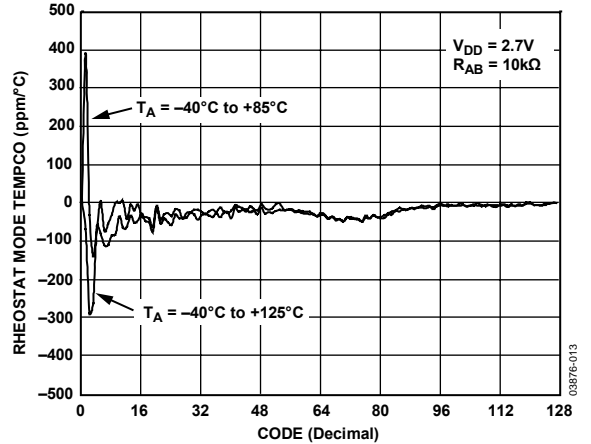


Figure 15.  $\Delta R_{WB}/\Delta T$  vs. Code

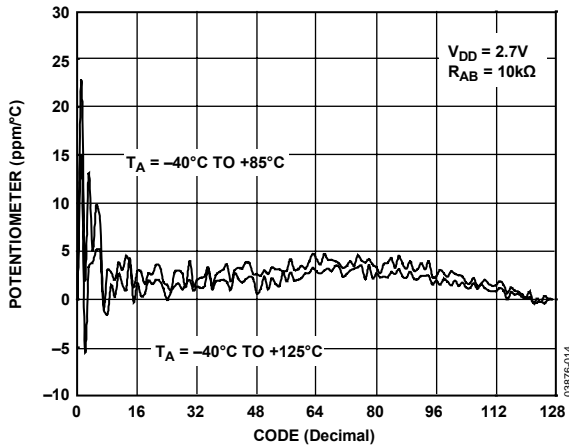


Figure 16.  $\Delta V_{WR}/\Delta T$  vs. Code

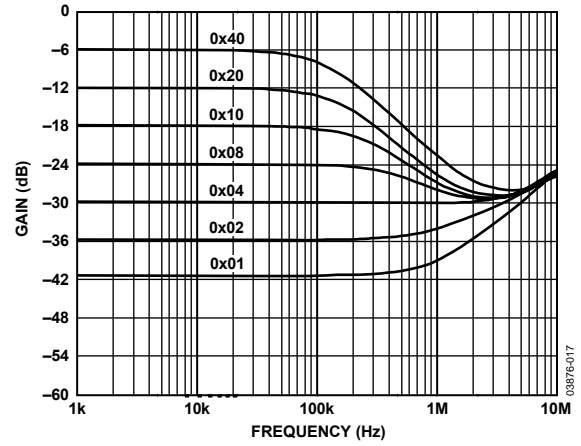


Figure 19. Gain vs. Frequency vs. Code,  $R_{AB} = 50 \text{ k}\Omega$

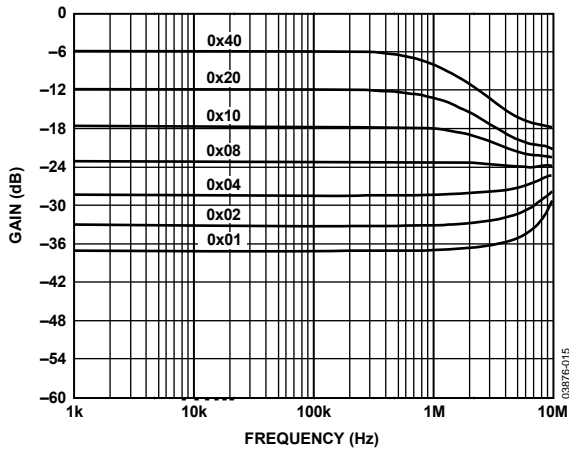


Figure 17. Gain vs. Frequency vs. Code,  $R_{AB} = 5 \text{ k}\Omega$

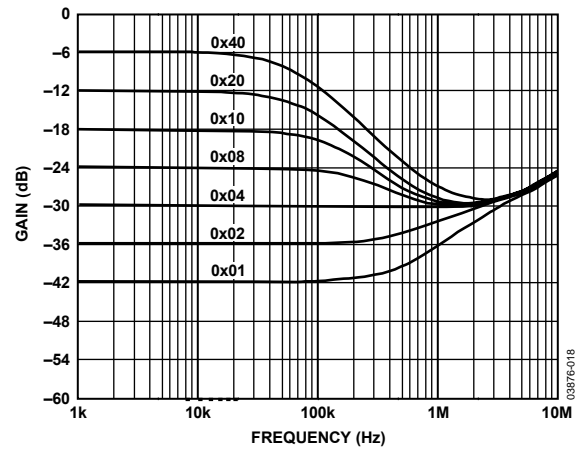


Figure 20. Gain vs. Frequency vs. Code,  $R_{AB} = 100 \text{ k}\Omega$

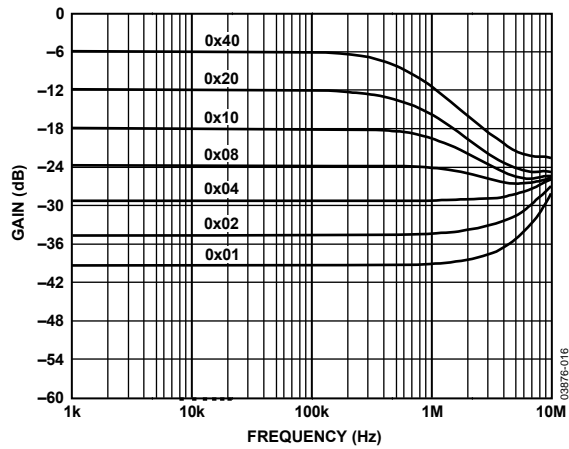


Figure 18. Gain vs. Frequency vs. Code,  $R_{AB} = 10 \text{ k}\Omega$

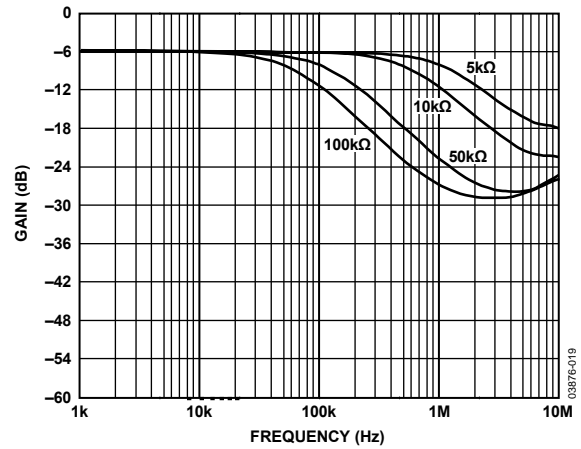


Figure 21.  $-3 \text{ dB}$  Bandwidth @ Code = 0x80

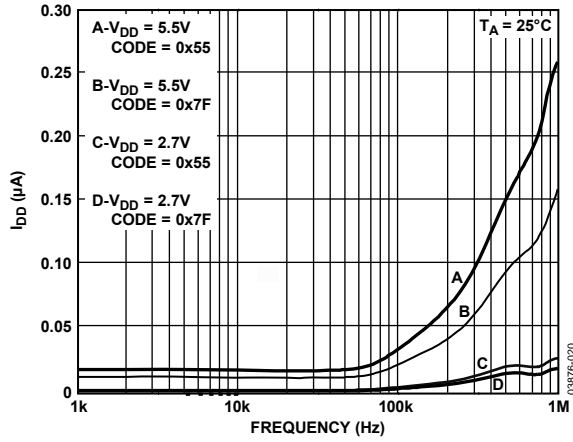


Figure 22.  $I_{DD}$  vs. Frequency

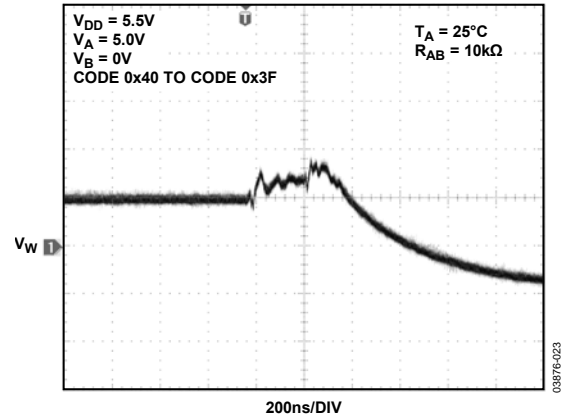


Figure 25. Midscale Glitch, Code 0x40 to Code 0x3F

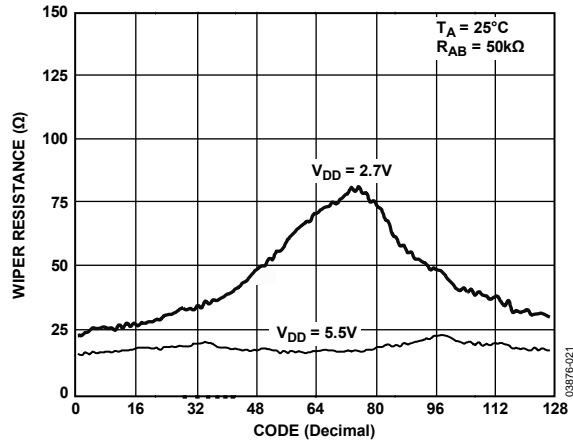


Figure 23. Wiper Resistance vs. Code vs.  $V_{DD}$

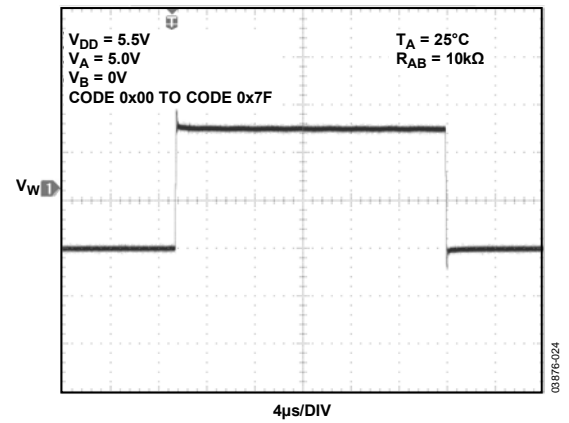


Figure 26. Large Signal Settling Time

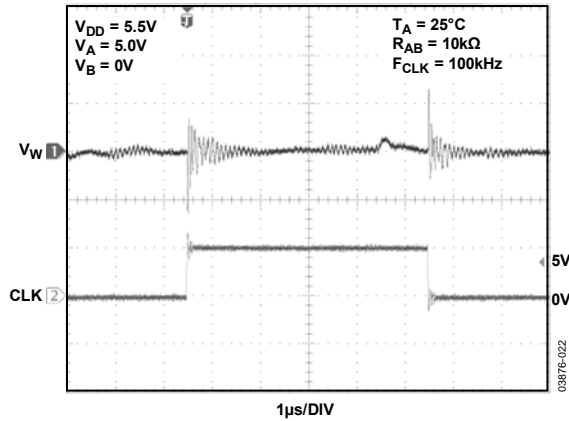


Figure 24. Digital Feedthrough

## TEST CIRCUITS

Figure 27 to Figure 32 define the test conditions used in the Specifications section.

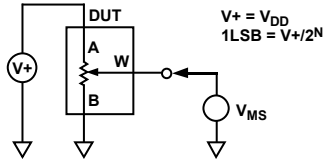


Figure 27. Potentiometer Divider Nonlinearity Error (INL, DNL)

03876-025

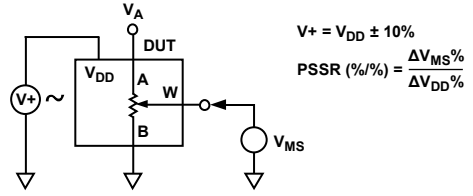


Figure 30. Power Supply Sensitivity (PSS, PSSR)

03876-028

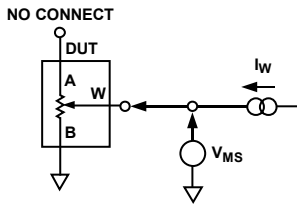


Figure 28. Resistor Position Nonlinearity Error (R-INL, R-DNL)

03876-026

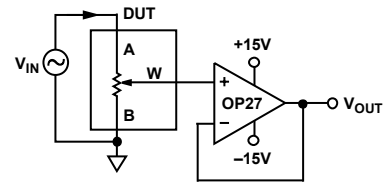


Figure 31. Gain vs. Frequency

03876-029

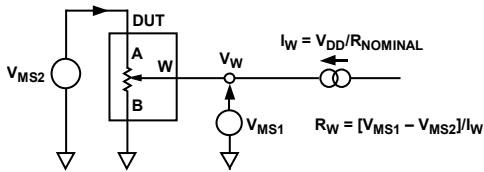


Figure 29. Wiper Resistance

03876-027

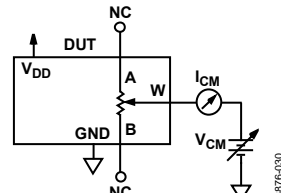


Figure 32. Common-Mode Leakage Current

03876-030

## I<sup>2</sup>C INTERFACE

The following abbreviations are used in this section:

- S = start condition
- P = stop condition
- A = acknowledge
- X = don't care
- $\bar{W}$  = write
- R = read
- A6, A5, A4, A3, A2, A1, A0 = address bits
- D6, D5, D4, D3, D2, D1, D0 = data bits

Table 6. Write Mode

S	A6	A5	A4	A3	A2	A1	A0	$\bar{W}$	A	X	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

Table 7. Read Mode

S	A6	A5	A4	A3	A2	A1	A0	R	A	0	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

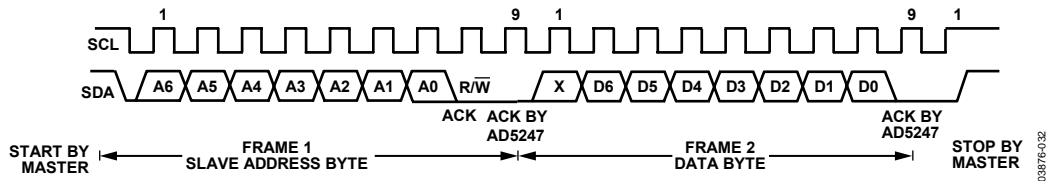


Figure 33. Writing to the RDAC Register

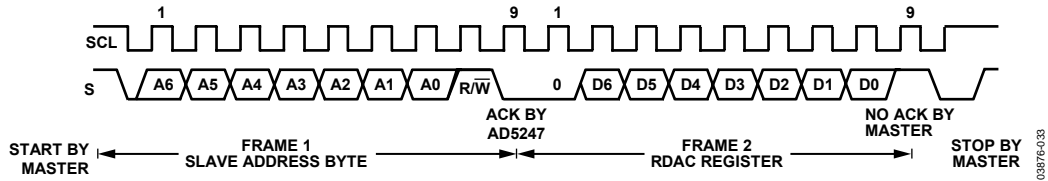


Figure 34. Reading from the RDAC Register

Table 8. I<sup>2</sup>C Slave Addresses

Model	Slave Addresses							Model	Slave Address						
	A6	A5	A4	A3	A2	A1	A0		A6	A5	A4	A3	A2	A1	A0
AD5247BKS5-R2	0	1	0	1	1	1	0	AD5247BKS50-RL7	0	1	0	1	1	1	0
AD5247BKS5-RL7	0	1	0	1	1	1	0	AD5247BKSZ50-RL7	0	1	0	1	1	1	0
AD5247BKSZ5-RL7	0	1	0	1	1	1	0	AD5247BKS100-R2	0	1	0	1	1	1	0
AD5247BKS10-R2	0	1	0	1	1	1	0	AD5247BKSZ100-R2	0	1	0	1	1	1	0
AD5247BKS10-RL7	0	1	0	1	1	1	0	AD5247BKS100-RL7	0	1	0	1	1	1	0
AD5247BKSZ10-RL7	0	1	0	1	1	1	0	AD5247BKSZ100-RL7	0	1	0	1	1	1	0
AD5247BKSZ10-1RL7	0	0	1	0	1	1	1	AD5247BKSZ100-1RL7	0	0	1	0	1	1	1
AD5247BKSZ10-2RL7	0	0	1	0	1	1	0	AD5247BKSZ100-2RL7	0	0	1	0	1	1	0
AD5247BKS50-R2	0	1	0	1	1	1	0								

## THEORY OF OPERATION

The AD5247 is a 128-position, digitally-controlled variable resistor (VR) device. An internal power-on preset places the wiper at midscale during power-on, which simplifies the default condition recovery at power-up.

### PROGRAMMING THE VARIABLE RESISTOR

#### Rheostat Operation

The nominal resistance ( $R_{AB}$ ) of the RDAC between Terminal A and Terminal B is available in 5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ . The final two or three digits of the part number determine the nominal resistance value; for example, 10 k $\Omega$  = 10 and 50 k $\Omega$  = 50. The  $R_{AB}$  of the VR has 128 contact points accessed by the wiper terminal, plus the B terminal contact. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible settings.

Assuming a 10 k $\Omega$  part is used, the wiper's first connection starts at the B terminal for Data 0x00. Because there is a 50  $\Omega$  wiper contact resistance, such a connection yields a minimum of 100  $\Omega$  ( $2 \times 50 \Omega$ ) resistance between Terminal W and Terminal B. The second connection is the first tap point, corresponding to 178  $\Omega$  ( $R_{WB} = R_{AB}/128 + R_W = 78 \Omega + 2 \times 50 \Omega$ ) for Data 0x01. The third connection is the next tap point, representing 256  $\Omega$  ( $2 \times 78 \Omega + 2 \times 50 \Omega$ ) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100  $\Omega$  ( $R_{AB} + 2 \times R_W$ ).

Figure 35 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string is not accessed.

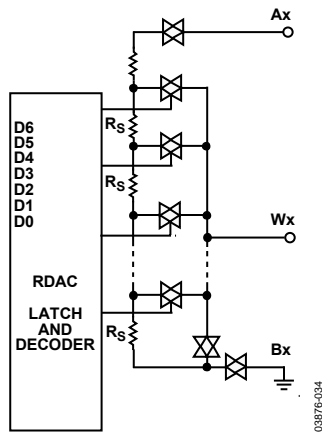


Figure 35. AD5247 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$  is the decimal equivalent of the binary code loaded in the 7-bit RDAC register.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if  $R_{AB} = 10 \text{ k}\Omega$  and the Terminal A is open-circuited, the output resistance  $R_{WB}$ , shown in Table 9, is set for the indicated RDAC latch codes.

Table 9. Codes and Corresponding  $R_{WB}$  Resistance

D (Decimal)	$R_{WB}$ ( $\Omega$ )	Output State
127	10,100	Full scale ( $R_{AB} + 2 \times R_W$ )
64	5100	Midscale
1	178	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite resistance of 100  $\Omega$  between Terminal W and Terminal B is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance,  $R_{WA}$ . When these terminals are used, the Terminal B can be opened. Set the resistance value for  $R_{WA}$  to start at a maximum value of resistance and to decrease the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{128 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

If  $R_{AB} = 10 \text{ k}\Omega$  and the B terminal is open-circuited, the output resistance,  $R_{WA}$ , shown in Table 10, is set for the indicated RDAC latch codes.

Table 10. Codes and Corresponding  $R_{WA}$  Resistance

D (Decimal)	$R_{WA}$ ( $\Omega$ )	Output State
127	178	Full scale
64	5100	Midscale
1	9961	1 LSB
0	10,100	Zero scale

Typical device-to-device matching is process lot dependent and can vary by up to  $\pm 30\%$ . Because the resistance element is processed in thin film technology, the change in  $R_{AB}$  with temperature has a very low 45 ppm/ $^{\circ}\text{C}$  temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A, proportional to the input voltage at A-to-B. Unlike the polarity of  $V_{DD}$  to GND, which must be positive, voltage across A-to-B, W-to-A, and W-to-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the Terminal A to 5 V and the Terminal B to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 128 positions of the potentiometer divider. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{128} \times V_A \quad (3)$$

A more accurate calculation that includes the effect of wiper resistance,  $V_W$ , is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike rheostat mode, divider mode makes the output voltage mainly on the ratio of Internal Resistor  $R_{WA}$  to Internal Resistor  $R_{WB}$ , and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/ $^{\circ}\text{C}$ .

## I<sup>2</sup>C-COMPATIBLE 2-WIRE SERIAL BUS

The first byte of the AD5247 is a slave address byte (see the I<sup>2</sup>C Interface section). It has a 7-bit slave address and an  $\overline{R/W}$  bit. The 5 k $\Omega$  and 50 k $\Omega$  options support one 7-bit slave address while the 10 k $\Omega$  and 100 k $\Omega$  options each have three hard-coded slave address options available (see Table 8 for a full list of slave address locations). The extra hard coded slave addresses on the 10 k $\Omega$  and 100 k $\Omega$  options allow users to employ up to three of these devices on one I<sup>2</sup>C bus. The seven MSBs of the slave address are followed by 0 for a write command or 1 to place the device in read mode.

The 2-wire I<sup>2</sup>C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 33). The following byte is the slave address byte, consisting of the 7-bit slave address followed by an  $\overline{R/W}$  bit (this bit determines whether data is read from or written to the slave device). The slave, whose address corresponds to the transmitted address, responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the  $\overline{R/W}$  bit is high, the master reads from the slave device. If the  $\overline{R/W}$  bit is low, the master writes to the slave device.
2. In write mode, after acknowledgement of the slave address byte, the next byte is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 33).
3. In read mode, after acknowledgment of the slave address byte, data is received over the serial bus in sequences of nine clock pulses (a slight difference from write mode, where eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 34).
4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10<sup>th</sup> clock pulse to establish a stop condition (see Figure 33). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10<sup>th</sup> clock pulse, which goes high to establish a stop condition (see Figure 34).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing the part only once. For example, after the RDAC has acknowledged its slave address in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address and data byte. Similarly, a repeated read function of the RDAC is also allowed.











