1 TMS320C6748 Fixed/Floating-Point DSP

1.1 Features

- 300-MHz C674x VLIW DSP
- C674x Instruction Set Features
  - Superset of the C67x+™ and C64x+™ ISAs
  - 2400/1800 C674x MIPS/MFLOPS
  - Byte-Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
- C674x Two Level Cache Memory Architecture
  - 32K-Byte L1P Program RAM/Cache
  - 32K-Byte L1D Data RAM/Cache
  - 256K-Byte L2 Unified Mapped RAM/Cache
  - Flexible RAM/Cache Partition (L1 and L2)
  - 1024K-Byte Boot ROM
- Enhanced Direct-Memory-Access Controller 3 (EDMA3):
  - 2 Channel Controllers
  - 3 Transfer Controllers
  - 64 Independent DMA Channels
  - 16 Quick DMA Channels
  - Programmable Transfer Burst Size
- TMS320C674x Floating-Point VLIW DSP Core
  - Load-Store Architecture With Non-Aligned Support
  - 64 General-Purpose Registers (32 Bit)
  - Six ALU (32-/40-Bit) Functional Units
    - Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point
    - Supports up to Four SP Additions Per Clock, Four DP Additions Every 2 Clocks
    - Supports up to Two Floating Point (SP or DP) Reciprocal Approximation (RCPxP) and Square-Root Reciprocal Approximation (RSQRxP) Operations Per Cycle
  - Two Multiply Functional Units
    - Mixed-Precision IEEE Floating Point Multiply Supported up to:
      - 2 SP x SP -> SP Per Clock
      - 2 SP x SP -> DP Every Two Clocks
      - 2 SP x DP -> DP Every Three Clocks
      - 2 DP x DP -> DP Every Four Clocks
    - Fixed Point Multiply Supports Two 32 x 32-Bit Multiplies, Four 16 x 16-Bit Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle, and Complex Multiples
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
  - Hardware Support for Modulo Loop Operation
  - Protected Mode Operation
  - Exceptions Support for Error Detection and Program Redirection
- Software Support
  - TI DSP/BIOS™
  - Chip Support Library and DSP Library
- 128K-Byte RAM Shared Memory
- 1.8V or 3.3V LVCMOS IOs (except for USB and DDR2 interfaces)
- Two External Memory Interfaces:
  - EMIFA
    - NOR (8-/16-Bit-Wide Data)
    - NAND (8-/16-Bit-Wide Data)
    - 16-Bit SDRAM With 128 MB Address Space
  - DDR2/Mobile DDR Memory Controller
    - 16-Bit DDR2 SDRAM With 512 MB Address Space or
    - 16-Bit mDDR SDRAM With 256 MB Address Space
- Three Configurable 16550 type UART Modules:
  - With Modem Control Signals
  - 16-byte FIFO
  - 16x or 13x Oversampling Option
- LCD Controller
- Two Serial Peripheral Interfaces (SPI) Each With Multiple Chip-Selects
- Two Multimedia Card (MMC)/Secure Digital (SD) Card Interface with Secure Data I/O (SDIO) Interfaces
- Two Master/Slave Inter-Integrated Circuit (I^2C Bus™)
- One Host-Port Interface (HPI) With 16-Bit-Wide Muxed Address/Data Bus For High Bandwidth
- USB 1.1 OHCI (Host) With Integrated PHY (USB1)

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- USB 2.0 OTG Port With Integrated PHY (USB0)
  - USB 2.0 High-/Full-Speed Client
  - USB 2.0 High-/Full-/Low-Speed Host
  - End Point 0 (Control)
  - End Points 1,2,3,4 (Control, Bulk, Interrupt or ISOC) Rx and Tx
- One Multichannel Audio Serial Port:
  - Transmit/Receive Clocks up to 50 MHz
  - Two Clock Zones and 16 Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
  - DIT-Capable
  - FIFO buffers for Transmit and Receive
- Two Multichannel Buffered Serial Ports:
  - Transmit/Receive Clocks up to 50 MHz
  - Two Clock Zones and 16 Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
  - AC97 Audio Codec Interface
  - Telecom Interfaces (ST-Bus, H100)
  - 128-channel TDM
  - FIFO buffers for Transmit and Receive
- 10/100 Mb/s Ethernet MAC (EMAC):
  - IEEE 802.3 Compliant
  - MII Media Independent Interface
  - RMII Reduced Media Independent Interface
  - Management Data I/O (MDIO) Module
- Video Port Interface (VPIF):
  - Two 8-bit SD (BT.656), Single 16-bit or Single Raw (8-/10-/12-bit) Video Capture Channels
  - Two 8-bit SD (BT.656), Single 16-bit Video Display Channels
- Universal Parallel Port (uPP):
  - High-Speed Parallel Interface to FPGAs and Data Converters
  - Data Width on Each of Two Channels is 8- to 16-bit Inclusive
  - Single Data Rate or Dual Data Rate Transfers
  - Supports Multiple Interfaces with START, ENABLE and WAIT Controls
- Serial ATA (SATA) Controller:
  - Supports SATA I (1.5 Gbps) and SATA II (3.0 Gbps)
  - Supports all SATA Power Management Features
  - Hardware-Assisted Native Command Queueing (NCQ) for up to 32 Entries
  - Supports Port Multiplier and Command-Based Switching
- Real-Time Clock With 32 KHz Oscillator and Separate Power Rail
- Three 64-Bit General-Purpose Timers (Configurable as Two 32-Bit Timers)
- One 64-Bit General-Purpose Timer (Watch Dog)
- Two Enhanced Pulse Width Modulators (eHRPWM):
  - Dedicated 16-Bit Time-Base Counter With Period And Frequency Control
  - 6 Single Edge, 6 Dual Edge Symmetric or 3 Dual Edge Asymmetric Outputs
  - Dead-Band Generation
  - PWM Chopping by High-Frequency Carrier
  - Trip Zone Input
- Three 32-Bit Enhanced Capture Modules (eCAP):
  - Configurable as 3 Capture Inputs or 3 Auxiliary Pulse Width Modulator (APWM) outputs
  - Single Shot Capture of up to Four Event Time-Stamps
- 361-Ball Pb-Free Plastic Ball Grid Array (PBGA) [ZCE Suffix], 0.65-mm Ball Pitch
- 361-Ball Pb-Free Plastic Ball Grid Array (PBGA) [ZWT Suffix], 0.80-mm Ball Pitch
- Commercial or Extended Temperature

1.2 Trademarks

DSP/BIOS, TMS320C6000, C6000, TMS320, TMS320C62x, and TMS320C67x are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

1.3 Description

The device is a Low-power applications processor based on a C674x DSP core. It provides significantly lower power than other members of the TMS320C6000™ platform of DSPs.

The device enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution.

The device DSP core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 also has a 1024KB Boot ROM. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

The peripheral set includes: a 10/100 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; one USB2.0 OTG interface; one USB1.1 OHCI interface; two inter-integrated circuit (I2C) Bus interfaces; one multichannel audio serial port (McASP) with 16 serializers and FIFO buffers; two multichannel buffered serial ports (McBSP) with FIFO buffers; two SPI interfaces with multiple chip selects; four 64-bit general-purpose timers each configurable (one configurable as watchdog); a configurable 16-bit host port interface (HPI) ; up to 9 banks of 16 pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; three UART interfaces (each with $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$); two enhanced high-resolution pulse width modulator (eHRPWM) peripherals; 3 32-bit enhanced capture (eCAP) module peripherals which can be configured as 3 capture inputs or 3 auxiliary pulse width modulator (APWM) outputs; and 2 external memory interfaces: an asynchronous and SDRAM external memory interface (EMIFA) for slower memories or peripherals, and a higher speed DDR2/Mobile DDR controller.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the device and a network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode. Additionally an Management Data Input/Output (MDIO) interface is available for PHY configuration. The EMAC supports both MII and RMII interfaces.

The SATA controller provides a high-speed interface to mass data storage devices. The SATA controller supports both SATA I (1.5 Gbps) and SATA II (3.0 Gbps).

The Universal Parallel Port (uPP) provides a high-speed interface to many types of data converters, FPGAs or other parallel devices. The UPP supports programmable data widths between 8- to 16-bits on each of two channels. Single-date rate and double-data rate transfers are supported as well as START, ENABLE and WAIT signals to provide control for a variety of data converters.

A Video Port Interface (VPIF) is included providing a flexible video input/output port.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.

The device has a complete set of development tools for the DSP. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

1.4 Functional Block Diagram

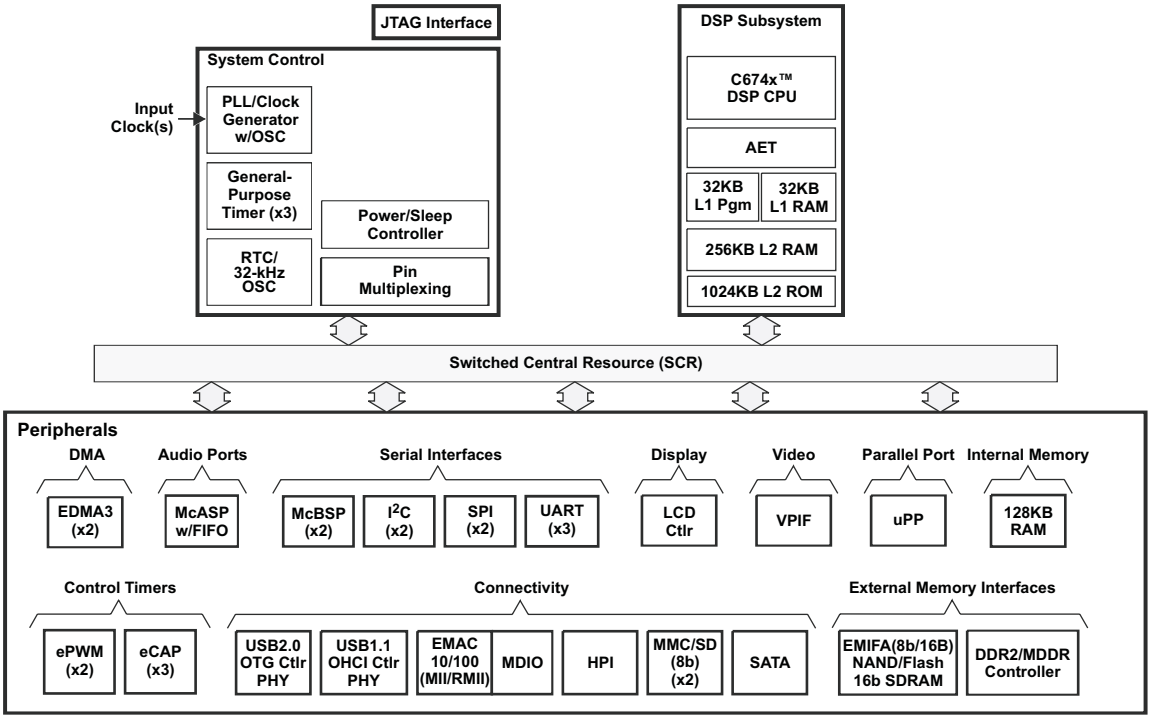

Figure 1-1. Functional Block Diagram

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Contents

2 Revision History

NOTE: This is a placeholder for the Revision History Table for future revisions of the document.

3 Device Overview

3.1 Documentation Support

3.1.1 Related Documentation From Texas Instruments

The following documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

DSP Reference Guides

SPRUG82 ***TMS320C674x DSP Cache User's Guide.*** Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

SPRUFE8 ***TMS320C674x DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

SPRUFK5 ***TMS320C674x DSP Megamodule Reference Guide.*** Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRUFK9 ***TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the device.

3.2 Device Characteristics

Table 3-1 provides an overview of the device. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

Table 3-1. Characteristics of C6748

HARDWARE FEATURES		C6748
Peripherals Not all peripherals pins are available at the same time (for more detail, see the Device Configurations section).	DDR2/mDDR Controller	DDR2 or Mobile DDR, 16-bit bus width, up to 150 MHz
	EMIFA	Asynchronous (8/16-bit bus width) RAM, Flash, 16-bit SDRAM, NOR, NAND
	Flash Card Interface	MMC and SD cards supported.
	EDMA3	64 independent channels, 16 QDMA channels, 2 channel controllers, 3 transfer controllers
	Timers	4 64-Bit General Purpose (configurable as 2 separate 32-bit timers, 1 configurable as Watch Dog)
	UART	3 (each with RTS and CTS flow control)
	SPI	2 (Each with one hardware chip select)
	I^2C	2 (both Master/Slave)
	Multichannel Audio Serial Port [McASP]	1 (each with transmit/receive, FIFO buffer, 16 serializers)
	Multichannel Buffered Serial Port [McBSP]	2 (each with transmit/receive, FIFO buffer, 16)
	10/100 Ethernet MAC with Management Data I/O	1 (MII or RMII Interface)
	eHRPWM	4 Single Edge, 4 Dual Edge Symmetric, or 2 Dual Edge Asymmetric Outputs
	eCAP	3 32-bit capture inputs or 3 32-bit auxiliary PWM outputs
	UHPI	1 (16-bit multiplexed address/data)
	USB 2.0 (USB0)	High-Speed OTG Controller with on-chip OTG PHY
	USB 1.1 (USB1)	Full-Speed OHCI (as host) with on-chip PHY
	General-Purpose Input/Output Port	9 banks of 16-bit
	LCD Controller	1
	SATA Controller	1 (Support both SATA I and SATAII)
	Universal Parallel Port (uPP)	1
	Video Port Interface (VPIF)	1 (video in and video out)
On-Chip Memory	Size (Bytes)	488KB RAM, 1088KB Boot ROM
	Organization	**DSP** 32KB L1 Program (L1P)/Cache (up to 32KB) 32KB L1 Data (L1D)/Cache (up to 32KB) 256KB Unified Mapped RAM/Cache (L2) 1024KB ROM (L2) DSP Memories can be made accessible to EDMA3 and other peripherals. **ADDITIONAL SHARED MEMORY** 128KB RAM
C674x CPU ID + CPU Rev ID	Control Status Register (CSR.[31:16])	0x1400
C674x Megamodule Revision	Revision ID Register (MM_REVID[15:0])	0x0000
JTAG BSDL_ID	DEVIDR0 Register	0x0B7D_102F
CPU Frequency	MHz	674x DSP 300 MHz
Cycle Time	ns	674x DSP $3.3\overline{3}$ ns
CPU Frequency	MHz	674x DSP 300 MHz
Cycle Time	ns	674x DSP $3.3\overline{3}$ ns
Voltage	Core (V)	1.2 V
	I/O (V)	1.8V or 3.3 V
Packages		13 mm x 13 mm, 361-Ball 0.65 mm pitch, PBGA (ZCE)
		16 mm x 16 mm, 361-Ball 0.80 mm pitch, PBGA (ZWT)

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Table 3-1. Characteristics of C6748 (continued)

HARDWARE FEATURES		C6748
Product Status(1)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PP

(1) PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals.

3.3 Device Compatibility

The C674x DSP core is code-compatible with the C6000™ DSP platform and supports features of both the C64x+ and C67x+ DSP families.

3.4 DSP Subsystem

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 256KB Unified Mapped RAM/Cache (L2)
- 1MB Mask-programmable ROM
- Little endian

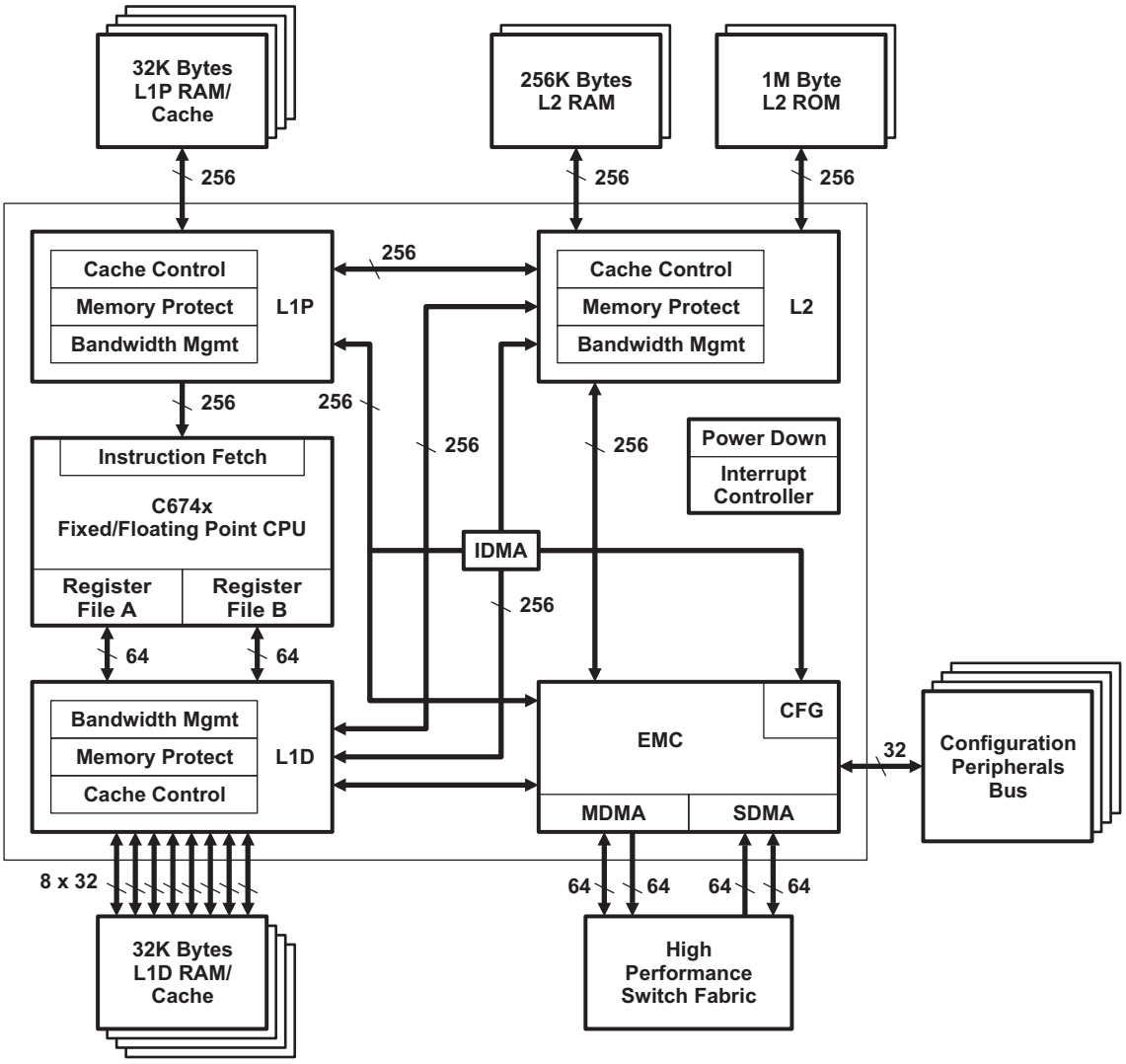

Figure 3-1. C674x Megamodule Block Diagram

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3.4.1 C674x DSP CPU Description

The C674x Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 3-2. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x+ core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On the previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

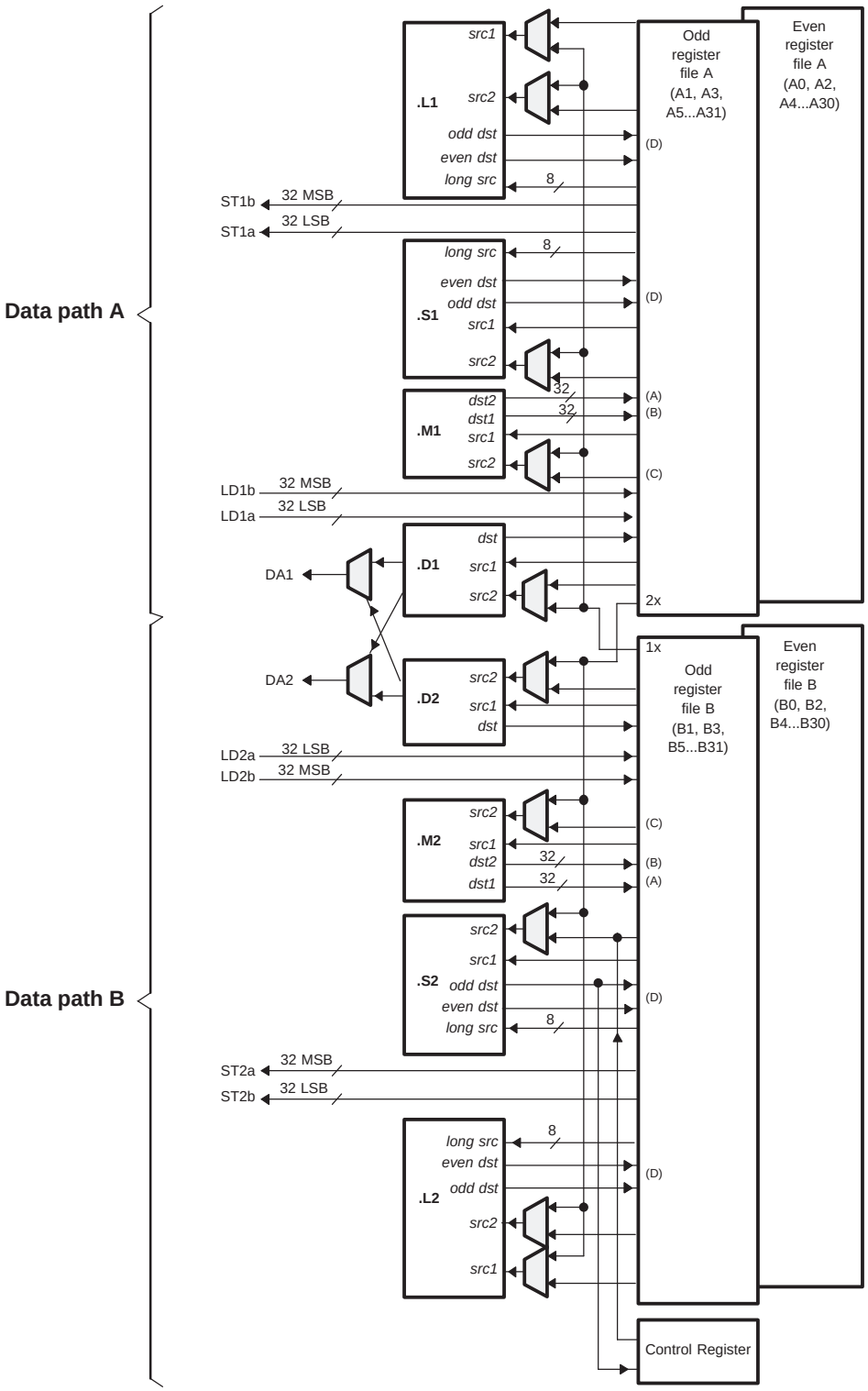
Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.

- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRUFE8)
- *TMS320C64x Technical Overview* (literature number SPRU395)



A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

Figure 3-2. TMS320C674x CPU (DSP Core) Data Paths

3.4.2 DSP Memory Mapping

The DSP memory map is shown in .

By default the DSP also has access to most on and off chip memory areas.

Additionally, the DSP megamodule includes the capability to limit access to its internal memories through its SDMA port; without needing an external MPU unit.

3.4.2.1 External Memories

The DSP has access to the following External memories:

- Asynchronous EMIF / SDRAM / NAND / NOR Flash (EMIFA)
- SDRAM (DDR2)

3.4.2.2 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

3.4.2.3 C674x CPU

The C674x core uses a two-level cache-based architecture. The Level 1 Program cache (L1P) is 32 KB direct mapped cache and the Level 1 Data cache (L1D) is 32 KB 2-way set associated cache. The Level 2 memory/cache (L2) consists of a 256 KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both.

Table 3-2 shows a memory map of the C674x CPU cache registers for the device.

Table 3-2. C674x Cache Registers

Byte Address	Register Name	Register Description
0x0184 0000	L2CFG	L2 Cache configuration register
0x0184 0020	L1PCFG	L1P Size Cache configuration register
0x0184 0024	L1PCC	L1P Freeze Mode Cache configuration register
0x0184 0040	L1DCFG	L1D Size Cache configuration register
0x0184 0044	L1DCC	L1D Freeze Mode Cache configuration register
0x0184 0048 - 0x0184 0FFC	-	Reserved
0x0184 1000	EDMAWEIGHT	L2 EDMA access control register
0x0184 1004 - 0x0184 1FFC	-	Reserved
0x0184 2000	L2ALLOC0	L2 allocation register 0
0x0184 2004	L2ALLOC1	L2 allocation register 1
0x0184 2008	L2ALLOC2	L2 allocation register 2
0x0184 200C	L2ALLOC3	L2 allocation register 3
0x0184 2010 - 0x0184 3FFF	-	Reserved
0x0184 4000	L2WBAR	L2 writeback base address register
0x0184 4004	L2WWC	L2 writeback word count register
0x0184 4010	L2WIBAR	L2 writeback invalidate base address register
0x0184 4014	L2WIWC	L2 writeback invalidate word count register
0x0184 4018	L2IBAR	L2 invalidate base address register
0x0184 401C	L2IWC	L2 invalidate word count register
0x0184 4020	L1PIBAR	L1P invalidate base address register
0x0184 4024	L1PIWC	L1P invalidate word count register
0x0184 4030	L1DWIBAR	L1D writeback invalidate base address register
0x0184 4034	L1DWIWC	L1D writeback invalidate word count register

Table 3-2. C674x Cache Registers (continued)

Byte Address	Register Name	Register Description
0x0184 4038	-	Reserved
0x0184 4040	L1DWBAR	L1D Block Writeback
0x0184 4044	L1DWWC	L1D Block Writeback
0x0184 4048	L1DIBAR	L1D invalidate base address register
0x0184 404C	L1DIWC	L1D invalidate word count register
0x0184 4050 - 0x0184 4FFF	-	Reserved
0x0184 5000	L2WB	L2 writeback all register
0x0184 5004	L2WBINV	L2 writeback invalidate all register
0x0184 5008	L2INV	L2 Global Invalidate without writeback
0x0184 500C - 0x0184 5027	-	Reserved
0x0184 5028	L1PINV	L1P Global Invalidate
0x0184 502C - 0x0184 5039	-	Reserved
0x0184 5040	L1DWB	L1D Global Writeback
0x0184 5044	L1DWBINV	L1D Global Writeback with Invalidate
0x0184 5048	L1DINV	L1D Global Invalidate without writeback
0x0184 8000 – 0x0184 80FF	MAR0 - MAR63	Reserved 0x0000 0000 – 0x3FFF FFFF
0x0184 8100 – 0x0184 817F	MAR64 – MAR95	Memory Attribute Registers for EMIFA SDRAM Data (CS0) 0x4000 0000 – 0x5FFF FFFF
0x0184 8180 – 0x0184 8187	MAR96 - MAR97	Memory Attribute Registers for EMIFA Async Data (CS2) 0x6000 0000 – 0x61FF FFFF
0x0184 8188 – 0x0184 818F	MAR98 – MAR99	Memory Attribute Registers for EMIFA Async Data (CS3) 0x6200 0000 – 0x63FF FFFF
0x0184 8190 – 0x0184 8197	MAR100 – MAR101	Memory Attribute Registers for EMIFA Async Data (CS4) 0x6400 0000 – 0x65FF FFFF
0x0184 8198 – 0x0184 819F	MAR102 – MAR103	Memory Attribute Registers for EMIFA Async Data (CS5) 0x6600 0000 – 0x67FF FFFF
0x0184 81A0 – 0x0184 81FF	MAR104 – MAR127	Reserved 0x6800 0000 – 0x7FFF FFFF
0x0184 8200	MAR128	Memory Attribute Register for Shared RAM 0x8000 0000 – 0x8001 FFFF
		Reserved 0x8002 0000 – 0x81FF FFFF
0x0184 8204 – 0x0184 82FF	MAR129 – MAR191	Reserved 0x8200 0000 – 0xBFFF FFFF
0x0184 8300 – 0x0184 837F	MAR192 – MAR223	Memory Attribute Registers for DDR2 Data (CS2) 0xC000 0000 – 0xDFFF FFFF
0x0184 8380 – 0x0184 83FF	MAR224 – MAR255	Reserved 0xE000 0000 – 0xFFFF FFFF

See the following table for a detailed top level device memory map that includes the DSP memory space.

3.5 Memory Map Summary

Table 3-3. C6748 Top Level Memory Map

Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x0000 0000	0x006F FFFF					
0x0070 0000	0x007F FFFF	1024K	DSP L2 ROM			
0x0080 0000	0x0083 FFFF	256K	DSP L2 RAM			
0x0084 0000	0x00DF FFFF					
0x00E0 0000	0x00E0 7FFF	32K	DSP L1P RAM			
0x00E0 8000	0x00EF FFFF					
0x00F0 0000	0x00F0 7FFF	32K	DSP L1D RAM			
0x00F0 8000	0x017F FFFF					
0x0180 0000	0x0180 FFFF	64K	DSP Interrupt Controller			
0x0181 0000	0x0181 0FFF	4K	DSP Powerdown Controller			
0x0181 1000	0x0181 1FFF	4K	DSP Security ID			
0x0181 2000	0x0181 2FFF	4K	DSP Revision ID			
0x0181 3000	0x0181 FFFF	52K	-			
0x0182 0000	0x0182 FFFF	64K	DSP EMC			
0x0183 0000	0x0183 FFFF	64K	DSP Internal Reserved			
0x0184 0000	0x0184 FFFF	64K	DSP Memory System			
0x0185 0000	0x01BB FFFF					
0x01BC 0000	0x01BC 0FFF	4K				
0x01BC 1000	0x01BC 17FF	2K				
0x01BC 1800	0x01BC 18FF	256				
0x01BC 1900	0x01BF FFFF					
0x01C0 0000	0x01C0 7FFF	32K	EDMA3 CC			
0x01C0 8000	0x01C0 83FF	1K	EDMA3 TC0			
0x01C0 8400	0x01C0 87FF	1K	EDMA3 TC1			
0x01C0 8800	0x01C0 FFFF					
0x01C1 0000	0x01C1 0FFF	4K	PSC 0			
0x01C1 1000	0x01C1 1FFF	4K	PLL Controller 0			
0x01C1 2000	0x01C1 3FFF					
0x01C1 4000	0x01C1 4FFF	4K	SYSCFG0			
0x01C1 5000	0x01C1 FFFF					
0x01C2 0000	0x01C2 0FFF	4K	Timer0			
0x01C2 1000	0x01C2 1FFF	4K	Timer1			
0x01C2 2000	0x01C2 2FFF	4K	I2C 0			
0x01C2 3000	0x01C2 3FFF	4K	RTC			
0x01C2 4000	0x01C3 FFFF					
0x01C4 0000	0x01C4 0FFF	4K	MMC/SD 0			
0x01C4 1000	0x01C4 1FFF	4K	SPI 0			
0x01C4 2000	0x01C4 2FFF	4K	UART 0			
0x01C4 3000	0x01CF FFFF					
0x01D0 0000	0x01D0 0FFF	4K	McASP 0 Control			
0x01D0 1000	0x01D0 1FFF	4K	McASP 0 AFIFO Ctrl			
0x01D0 2000	0x01D0 2FFF	4K	McASP 0 Data			
0x01D0 3000	0x01D0 BFFF					
0x01D0 C000	0x01D0 CFFF	4K	UART 1			

Table 3-3. C6748 Top Level Memory Map (continued)

Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01D0 D000	0x01D0 DFFF	4K	UART 2			
0x01D0 E000	0x01D0 FFFF					
0x01D1 0000	0x01D1 07FF	2K	McBSP0			
0x01D1 0800	0x01D1 0FFF	2K	McBSP0 FIFO Ctrl			
0x01D1 1000	0x01D1 17FF	2K	McBSP1			
0x01D1 1800	0x01D1 1FFF	2K	McBSP1 FIFO Ctrl			
0x01D1 2000	0x01DF FFFF					
0x01E0 0000	0x01E0 FFFF	64K	USB0			
0x01E1 0000	0x01E1 0FFF	4K	UHPI			
0x01E1 1000	0x01E1 2FFF					
0x01E1 3000	0x01E1 3FFF	4K	LCD Controller			
0x01E1 4000	0x01E1 5FFF					
0x01E1 6000	0x01E1 6FFF	4K	UPP			
0x01E1 7000	0x01E1 7FFF	4K	VPIF			
0x01E1 8000	0x01E1 9FFF	8K	SATA			
0x01E1 A000	0x01E1 AFFF	4K	PLL Controller 1			
0x01E1 B000	0x01E1 BFFF	4K	MMCSD1			
0x01E1 C000	0x01E1 FFFF					
0x01E2 0000	0x01E2 1FFF	8K	EMAC Control Module RAM			
0x01E2 2000	0x01E2 2FFF	4K	EMAC Control Module Registers			
0x01E2 3000	0x01E2 3FFF	4K	EMAC Control Registers			
0x01E2 4000	0x01E2 4FFF	4K	EMAC MDIO port			
0x01E2 5000	0x01E2 5FFF	4K	USB1			
0x01E2 6000	0x01E2 6FFF	4K	GPIO			
0x01E2 7000	0x01E2 7FFF	4K	PSC 1			
0x01E2 8000	0x01E2 8FFF	4K	I2C 1			
0x01E2 9000	0x01E2 BFFF					
0x01E2 C000	0x01E2 CFFF	4K	SYSCFG1			
0x01E2 D000	0x01E2 FFFF					
0x01E3 0000	0x01E3 7FFF	32K	EDMA3 CC1			
0x01E3 8000	0x01E3 83FF	1K	EDMA3 TC2			
0x01E3 8400	0x01EF FFFF					
0x01F0 0000	0x01F0 0FFF	4K	eHRPWM 0			
0x01F0 1000	0x01F0 1FFF	4K	HRPWM 0			
0x01F0 2000	0x01F0 2FFF	4K	eHRPWM 1			
0x01F0 3000	0x01F0 3FFF	4K	HRPWM 1			
0x01F0 4000	0x01F0 5FFF					
0x01F0 6000	0x01F0 6FFF	4K	ECAP 0			
0x01F0 7000	0x01F0 7FFF	4K	ECAP 1			
0x01F0 8000	0x01F0 8FFF	4K	ECAP 2			
0x01F0 9000	0x01F0 BFFF					
0x01F0 C000	0x01F0 CFFF	4K	Timer2			
0x01F0 D000	0x01F0 DFFF	4K	Timer3			
0x01F0 E000	0x01F0 EFFF	4K	SPI1			
0x01F0 F000	0x01F0 FFFF					
0x01F1 0000	0x01F1 0FFF	4K	McBSP0 FIFO Data			

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Table 3-3. C6748 Top Level Memory Map (continued)

Start Address	End Address	Size	DSP Mem Map	EDMA Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01F1 1000	0x01F1 1FFF	4K	McBSP1 FIFO Data			
0x01F1 2000	0x116F FFFF					
0x1170 0000	0x117F FFFF	1024K	DSP L2 ROM			
0x1180 0000	0x1183 FFFF	256K	DSP L2 RAM			
0x1184 0000	0x11DF FFFF					
0x11E0 0000	0x11E0 7FFF	32K	DSP L1P RAM			
0x11E0 8000	0x11EF FFFF					
0x11F0 0000	0x11F0 7FFF	32K	DSP L1D RAM			
0x11F0 8000	0x3FFF FFFF					
0x4000 0000	0x5FFF FFFF	512M	EMIFA SDRAM data (CS0)			
0x6000 0000	0x61FF FFFF	32M	EMIFA async data (CS2)			
0x6200 0000	0x63FF FFFF	32M	EMIFA async data (CS3)			
0x6400 0000	0x65FF FFFF	32M	EMIFA async data (CS4)			
0x6600 0000	0x67FF FFFF	32M	EMIFA async data (CS5)			
0x6800 0000	0x6800 7FFF	32K	EMIFA Control Regs			
0x6800 8000	0x7FFF FFFF					
0x8000 0000	0x8001 FFFF	128K	Shared RAM			
0x8002 0000	0xAFFF FFFF					
0xB000 0000	0xB000 7FFF	32K	DDR2 Control Regs			
0xB000 8000	0xBFFF FFFF					
0xC000 0000	0xDFFF FFFF	512M	DDR2 Data			
0xE000 0000	0xFFFC FFFF					
0xFFFD 0000	0xFFFD FFFF	64K				
0xFFFE 0000	0xFFFE DFFF					
0xFFFE E000	0xFFFE FFFF	8K				
0xFFFF 0000	0xFFFF 1FFF	8K				
0xFFFF 2000	0xFFFF FFFF					

3.6 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

3.6.1 Pin Map (Bottom View)

The following graphics show the bottom view of the ZCE and ZWT packages pin assignments in four quadrants (A, B, C, and D). The pin assignments for both packages are identical.

	1	2	3	4	5	6	7	8	9	10	
W	VP_DOUT[0]/ LCD_D[0]/ UPP_XD[8]/ GP7[8]	VP_DOUT[1]/ LCD_D[1]/ UPP_XD[9]/ GP7[9]	VP_DOUT[2]/ LCD_D[2]/ UPP_XD[10]/ GP7[10]	DDR_A[10]	DDR_A[6]	DDR_A[2]	DDR_CLKN	DDR_CLKP	DDR_RAS	DDR_D[15]	W
V	VP_DOUT[3]/ LCD_D[3]/ UPP_XD[11]/ GP7[11]	VP_DOUT[4]/ LCD_D[4]/ UPP_XD[12]/ GP7[12]	VP_DOUT[5]/ LCD_D[5]/ UPP_XD[13]/ GP7[13]	DDR_A[12]	DDR_A[5]	DDR_A[3]	DDR_CKE	DDR_BA[0]	DDR_CS	DDR_D[13]	V
U	VP_DOUT[6]/ LCD_D[6]/ UPP_XD[14]/ GP7[14]	VP_DOUT[7]/ LCD_D[7]/ UPP_XD[15]/ GP7[15]	VP_DOUT[8]/ LCD_D[8]/ UPP_XD[0]/ GP7[0]/ BOOT[0]	DDR_A[8]	DDR_A[4]	DDR_A[7]	DDR_A[0]	DDR_BA[2]	DDR_CAS	DDR_D[12]	U
T	VP_DOUT[9]/ LCD_D[9]/ UPP_XD[1]/ GP7[1]/ BOOT[1]	VP_DOUT[10]/ LCD_D[10]/ UPP_XD[2]/ GP7[2]/ BOOT[2]	VP_DOUT[11]/ LCD_D[11]/ UPP_XD[3]/ GP7[3]/ BOOT[3]	DDR_A[11]	DDR_A[13]	DDR_A[9]	DDR_A[1]	DDR_WE	DDR_BA[1]	DDR_D[10]	T
R	VP_DOUT[12]/ LCD_D[12]/ UPP_XD[4]/ GP7[4]/ BOOT[4]	VP_DOUT[13]/ LCD_D[13]/ UPP_XD[5]/ GP7[5]/ BOOT[5]	VP_DOUT[14]/ LCD_D[14]/ UPP_XD[6]/ GP7[6]/ BOOT[6]	DVDD3313_C	LCD_AC_ENB_CS/ GP6[0]	DDR_VREF	DDR_DVDD18	DDR_DVDD18	DDR_DVDD18	DDR_DQM[1]	R
P	SATA_VDD	SATA_VDD	SATA_VDDR	VP_DOUT[15]/ LCD_D[15]/ UPP_XD[7]/ GP7[7]/ BOOT[7]	DVDD3318_C	DVDD3318_C	DDR_DVDD18	DDR_DVDD18	DDR_DVDD18	DDR_DVDD18	P
N	SATA_REFCLKN	SATA_REFCLKP	SATA_REG	SATA_VDD	VSS	DDR_DVDD18	RVDD	CVDD	DDR_DVDD18	DDR_DVDD18	N
M	SATA_VSS	SATA_VDD	NC	VSS	VSS	VSS	VSS	CVDD	CVDD	VSS	M
L	SATA_RXP	SATA_RXN	SATA_VSS	DVDD3318_C	VSS	DVDD18	VSS	VSS	VSS	VSS	L
K	SATA_VSS	SATA_VSS	VP_CLKOUT2/ MMCSD1_DAT2/ GP6[3]	VP_CLKOUT3/ GP6[1]	DVDD18	CVDD	VSS	VSS	VSS	VSS	K
	1	2	3	4	5	6	7	8	9	10	

Figure 3-3. Pin Map (Quad A)

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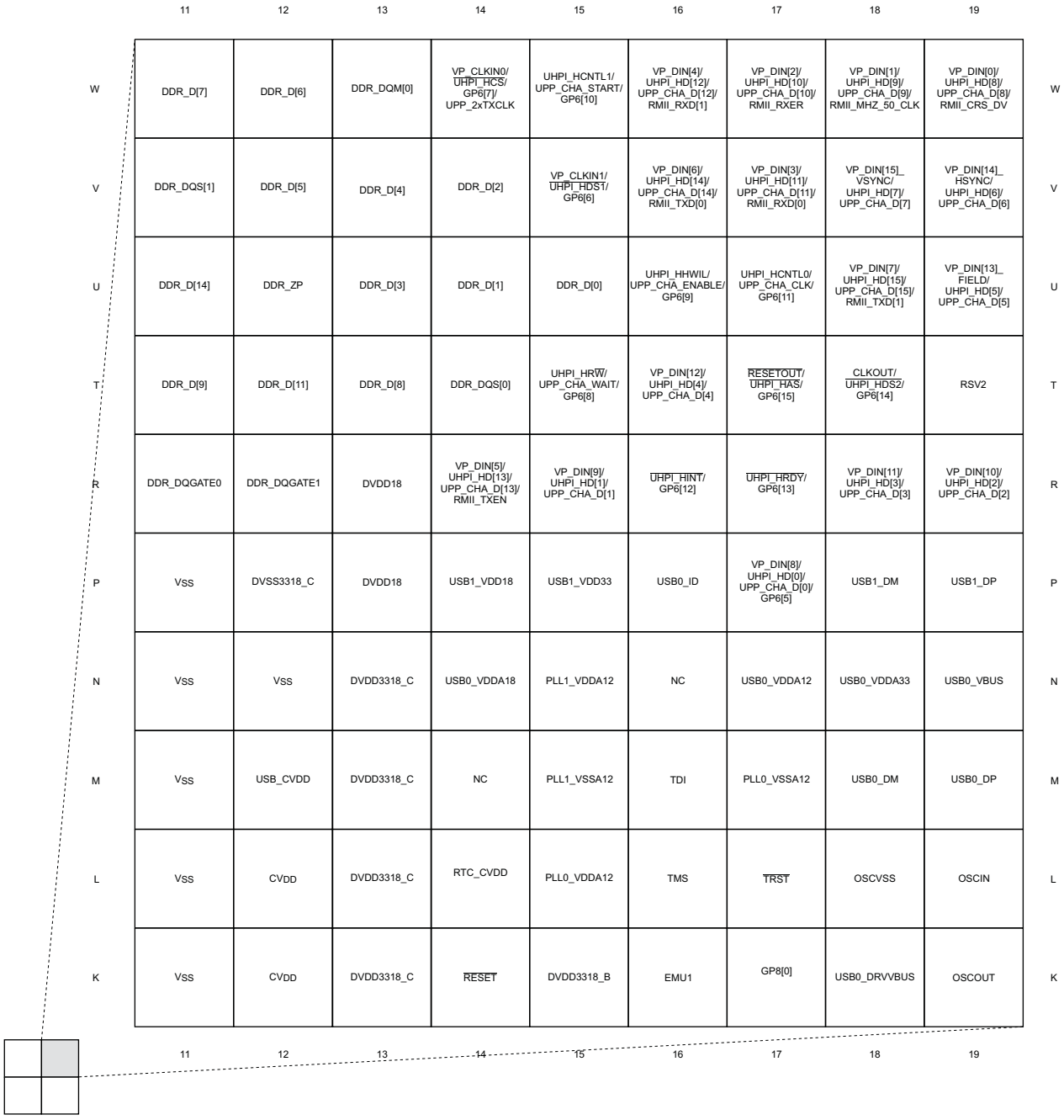
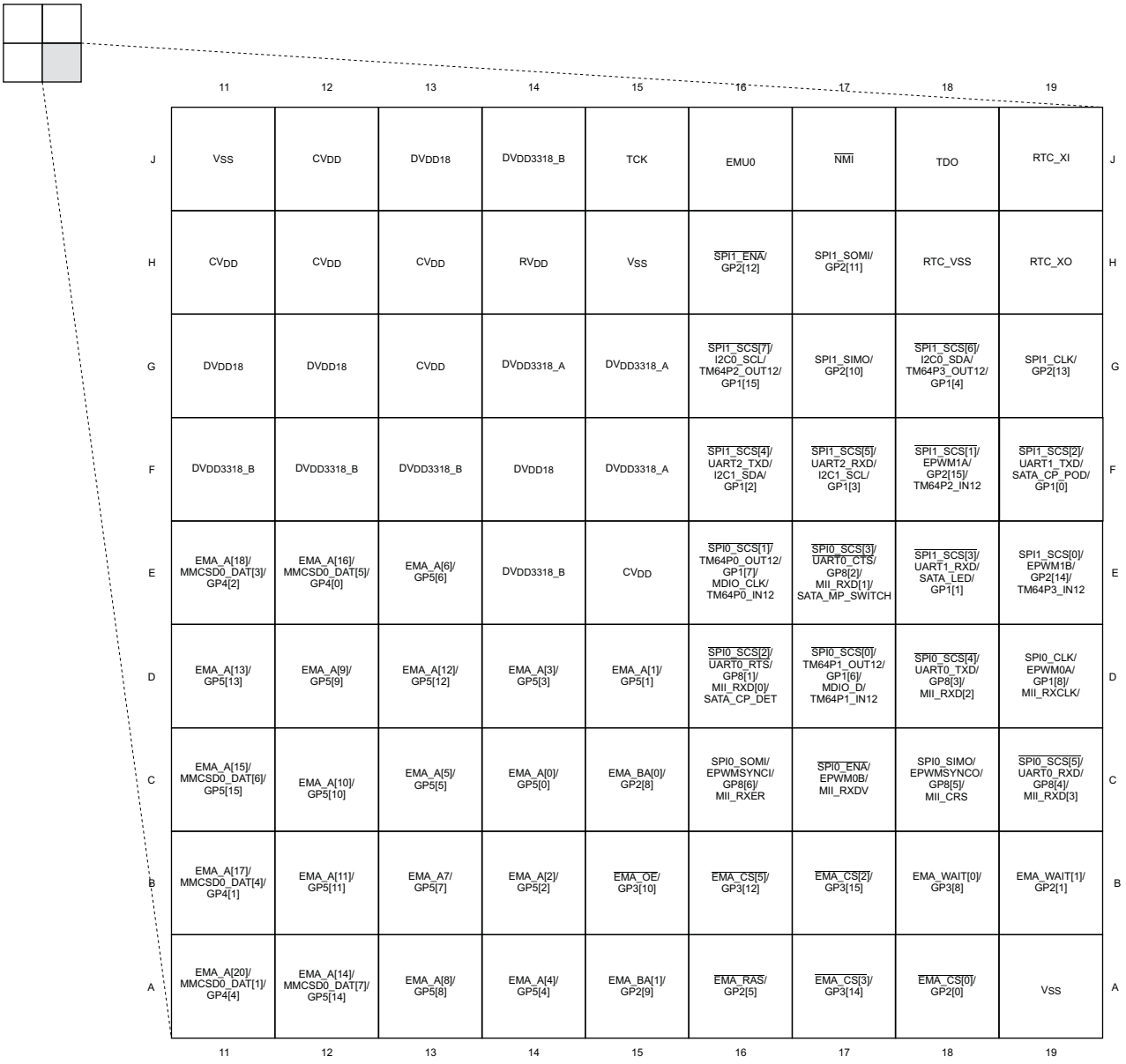


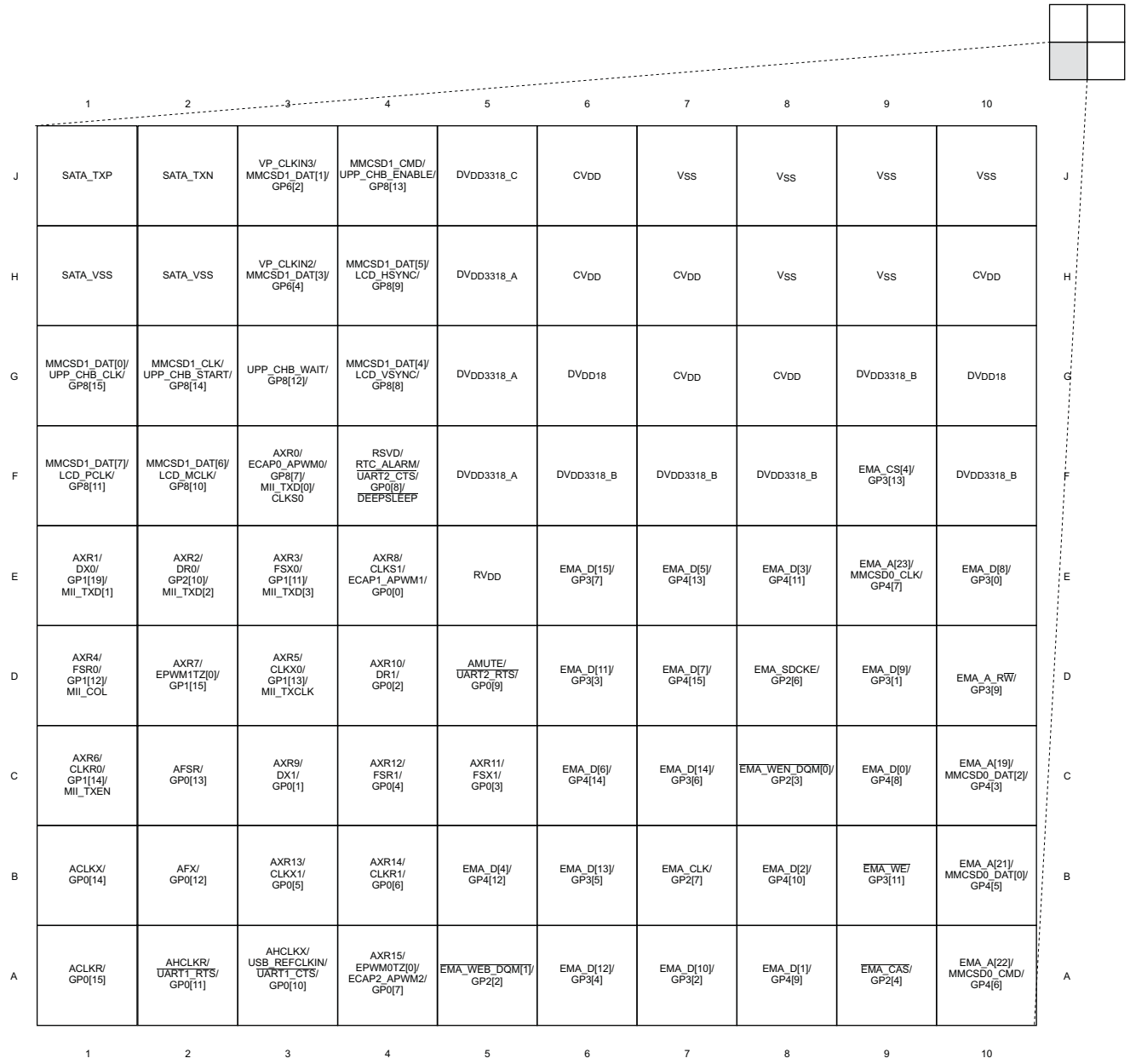
	11	12	13	14	15	16	17	18	19	
W	DDR_D[7]	DDR_D[6]	DDR_DQM[0]	VP_CLKIN0/ UHPI_HCS/ GP6[7]/ UPP_2xTXCLK	UHPI_HCNTL1/ UPP_CHA_START/ GP6[10]	VP_DIN[4]/ UHPI_HD[12]/ UPP_CHA_D[12]/ RMII_RXD[1]	VP_DIN[2]/ UHPI_HD[10]/ UPP_CHA_D[10]/ RMII_RXER	VP_DIN[1]/ UHPI_HD[9]/ UPP_CHA_D[9]/ RMII_MHZ_50_CLK	VP_DIN[0]/ UHPI_HD[8]/ UPP_CHA_D[8]/ RMII_CRS_DV	W
V	DDR_DQS[1]	DDR_D[5]	DDR_D[4]	DDR_D[2]	VP_CLKIN1/ UHPI_HDS1/ GP6[6]	VP_DIN[6]/ UHPI_HD[14]/ UPP_CHA_D[14]/ RMII_TXD[0]	VP_DIN[3]/ UHPI_HD[11]/ UPP_CHA_D[11]/ RMII_RXD[0]	VP_DIN[15]_ VSYNC/ UHPI_HD[7]/ UPP_CHA_D[7]	VP_DIN[14]_ HSYNC/ UHPI_HD[6]/ UPP_CHA_D[6]	V
U	DDR_D[14]	DDR_ZP	DDR_D[3]	DDR_D[1]	DDR_D[0]	UHPI_HHWIL/ UPP_CHA_ENABLE/ GP6[9]	UHPI_HCNTL0/ UPP_CHA_CLK/ GP6[11]	VP_DIN[7]/ UHPI_HD[15]/ UPP_CHA_D[15]/ RMII_TXD[1]	VP_DIN[13]_ FIELD/ UHPI_HD[5]/ UPP_CHA_D[5]	U
T	DDR_D[9]	DDR_D[11]	DDR_D[8]	DDR_DQS[0]	UHPI_HRW/ UPP_CHA_WAIT/ GP6[8]	VP_DIN[12]/ UHPI_HD[4]/ UPP_CHA_D[4]	RESETOUT/ UHPI_HAS/ GP6[15]	CLKOUT/ UHPI_HDS2/ GP6[14]	RSV2	T
R	DDR_DQGATE0	DDR_DQGATE1	DVDD18	VP_DIN[5]/ UHPI_HD[13]/ UPP_CHA_D[13]/ RMII_TXEN	VP_DIN[9]/ UHPI_HD[1]/ UPP_CHA_D[1]	UHPI_HINT/ GP6[12]	UHPI_HRDY/ GP6[13]	VP_DIN[11]/ UHPI_HD[3]/ UPP_CHA_D[3]	VP_DIN[10]/ UHPI_HD[2]/ UPP_CHA_D[2]	R
P	VSS	DVSS3318_C	DVDD18	USB1_VDD18	USB1_VDD33	USB0_ID	VP_DIN[8]/ UHPI_HD[0]/ UPP_CHA_D[0]/ GP6[5]	USB1_DM	USB1_DP	P
N	VSS	VSS	DVDD3318_C	USB0_VDDA18	PLL1_VDDA12	NC	USB0_VDDA12	USB0_VDDA33	USB0_VBUS	N
M	VSS	USB_CVDD	DVDD3318_C	NC	PLL1_VSSA12	TDI	PLL0_VSSA12	USB0_DM	USB0_DP	M
L	VSS	CVDD	DVDD3318_C	RTC_CVDD	PLL0_VDDA12	TMS	TRST	OSCVSS	OSCIN	L
K	VSS	CVDD	DVDD3318_C	RESET	DVDD3318_B	EMU1	GP8[0]	USB0_DRVVBUS	OSCOUT	K
	11	12	13	14	15	16	17	18	19	

Figure 3-4. Pin Map (Quad B)



	11	12	13	14	15	16	17	18	19	
J	VSS	CVDD	DVDD18	DVDD3318_B	TCK	EMU0	NMI	TDO	RTC_XI	J
H	CVDD	CVDD	CVDD	RVDD	VSS	SPI1_ENA/ GP2[12]	SPI1_SOMI/ GP2[11]	RTC_VSS	RTC_XO	H
G	DVDD18	DVDD18	CVDD	DVDD3318_A	DVDD3318_A	SPI1_SCS[7]/ I2C0_SCL/ TM64P2_OUT12/ GP1[15]	SPI1_SIMO/ GP2[10]	SPI1_SCS[6]/ I2C0_SDA/ TM64P3_OUT12/ GP1[4]	SPI1_CLK/ GP2[13]	G
F	DVDD3318_B	DVDD3318_B	DVDD3318_B	DVDD18	DVDD3318_A	SPI1_SCS[4]/ UART2_TXD/ I2C1_SDA/ GP1[2]	SPI1_SCS[5]/ UART2_RXD/ I2C1_SCL/ GP1[3]	SPI1_SCS[1]/ EPWM1A/ GP2[15]/ TM64P2_IN12	SPI1_SCS[2]/ UART1_TXD/ SATA_CP_POD/ GP1[0]	F
E	EMA_A[18]/ MMCSD0_DAT[3]/ GP4[2]	EMA_A[16]/ MMCSD0_DAT[5]/ GP4[0]	EMA_A[6]/ GP5[6]	DVDD3318_B	CVDD	SPI0_SCS[1]/ TM64P0_OUT12/ GP1[7]/ MDIO_CLK/ TM64P0_IN12	SPI0_SCS[3]/ UART0_CTS/ GP8[2]/ MII_RXD[1]/ SATA_MP_SWITCH	SPI1_SCS[3]/ UART1_RXD/ SATA_LED/ GP1[1]	SPI1_SCS[0]/ EPWM1B/ GP2[14]/ TM64P3_IN12	E
D	EMA_A[13]/ GP5[13]	EMA_A[9]/ GP5[9]	EMA_A[12]/ GP5[12]	EMA_A[3]/ GP5[3]	EMA_A[1]/ GP5[1]	SPI0_SCS[2]/ UART0_RTS/ GP8[1]/ MII_RXD[0]/ SATA_CP_DET	SPI0_SCS[0]/ TM64P1_OUT12/ GP1[6]/ MDIO_D/ TM64P1_IN12	SPI0_SCS[4]/ UART0_TXD/ GP8[3]/ MII_RXD[2]	SPI0_CLK/ EPWM0A/ GP1[8]/ MII_RXCLK/	D
C	EMA_A[15]/ MMCSD0_DAT[6]/ GP5[15]	EMA_A[10]/ GP5[10]	EMA_A[5]/ GP5[5]	EMA_A[0]/ GP5[0]	EMA_BA[0]/ GP2[8]	SPI0_SOMI/ EPWMSYNCI/ GP8[6]/ MII_RXER	SPI0_ENA/ EPWM0B/ MII_RXDV	SPI0_SIMO/ EPWMSYNCO/ GP8[5]/ MII_CRS	SPI0_SCS[5]/ UART0_RXD/ GP8[4]/ MII_RXD[3]	C
B	EMA_A[17]/ MMCSD0_DAT[4]/ GP4[1]	EMA_A[11]/ GP5[11]	EMA_A7/ GP5[7]	EMA_A[2]/ GP5[2]	EMA_OE/ GP3[10]	EMA_CS[5]/ GP3[12]	EMA_CS[2]/ GP3[15]	EMA_WAIT[0]/ GP3[8]	EMA_WAIT[1]/ GP2[1]	B
A	EMA_A[20]/ MMCSD0_DAT[1]/ GP4[4]	EMA_A[14]/ MMCSD0_DAT[7]/ GP5[14]	EMA_A[8]/ GP5[8]	EMA_A[4]/ GP5[4]	EMA_BA[1]/ GP2[9]	EMA_RAS/ GP2[5]	EMA_CS[3]/ GP3[14]	EMA_CS[0]/ GP2[0]	VSS	A
	11	12	13	14	15	16	17	18	19	

Figure 3-5. Pin Map (Quad C)



	1	2	3	4	5	6	7	8	9	10	
J	SATA_TXP	SATA_TXN	VP_CLKIN3/ MMCSD1_DAT[1]/ GP6[2]	MMCSD1_CMD/ UPP_CHB_ENABLE/ GP8[13]	DVDD3318_C	CVDD	VSS	VSS	VSS	VSS	J
H	SATA_VSS	SATA_VSS	VP_CLKIN2/ MMCSD1_DAT[3]/ GP6[4]	MMCSD1_DAT[5]/ LCD_HSYNC/ GP8[9]	DVDD3318_A	CVDD	CVDD	VSS	VSS	CVDD	H
G	MMCSD1_DAT[0]/ UPP_CHB_CLK/ GP8[15]	MMCSD1_CLK/ UPP_CHB_START/ GP8[14]	UPP_CHB_WAIT/ GP8[12]/	MMCSD1_DAT[4]/ LCD_VSYNC/ GP8[8]	DVDD3318_A	DVDD18	CVDD	CVDD	DVDD3318_B	DVDD18	G
F	MMCSD1_DAT[7]/ LCD_PCLK/ GP8[11]	MMCSD1_DAT[6]/ LCD_MCLK/ GP8[10]	AXR0/ ECAP0_APWM0/ GP8[7]/ MII_TXD[0]/ CLKS0	RSVD/ RTC_ALARM/ UART2_CTS/ GP0[8]/ DEEPSLEEP	DVDD3318_A	DVDD3318_B	DVDD3318_B	DVDD3318_B	EMA_CS[4]/ GP3[13]	DVDD3318_B	F
E	AXR1/ DX0/ GP1[19]/ MII_TXD[1]	AXR2/ DR0/ GP2[10]/ MII_TXD[2]	AXR3/ FSX0/ GP1[11]/ MII_TXD[3]	AXR8/ CLKS1/ ECAP1_APWM1/ GP0[0]	RVDD	EMA_D[15]/ GP3[7]	EMA_D[5]/ GP4[13]	EMA_D[3]/ GP4[11]	EMA_A[23]/ MMCSD0_CLK/ GP4[7]	EMA_D[8]/ GP3[0]	E
D	AXR4/ FSR0/ GP1[12]/ MII_COL	AXR7/ EPWM1TZ[0]/ GP1[15]	AXR5/ CLKX0/ GP1[13]/ MII_TXCLK	AXR10/ DR1/ GP0[2]	AMUTE/ UART2_RTS/ GP0[9]	EMA_D[11]/ GP3[3]	EMA_D[7]/ GP4[15]	EMA_SDCKE/ GP2[6]	EMA_D[9]/ GP3[1]	EMA_A_RW/ GP3[9]	D
C	AXR6/ CLKR0/ GP1[14]/ MII_TXEN	AFSR/ GP0[13]	AXR9/ DX1/ GP0[1]	AXR12/ FSR1/ GP0[4]	AXR11/ FSX1/ GP0[3]	EMA_D[6]/ GP4[14]	EMA_D[14]/ GP3[6]	EMA_WEN_DQM[0]/ GP2[3]	EMA_D[0]/ GP4[8]	EMA_A[19]/ MMCSD0_DAT[2]/ GP4[3]	C
B	ACLKX/ GP0[14]	AFX/ GP0[12]	AXR13/ CLKX1/ GP0[5]	AXR14/ CLKR1/ GP0[6]	EMA_D[4]/ GP4[12]	EMA_D[13]/ GP3[5]	EMA_CLK/ GP2[7]	EMA_D[2]/ GP4[10]	EMA_WE/ GP3[11]	EMA_A[21]/ MMCSD0_DAT[0]/ GP4[5]	B
A	ACLKR/ GP0[15]	AHCLKR/ UART1_RTS/ GP0[11]	AHCLKX/ USB_REFCLKIN/ UART1_CTS/ GP0[10]	AXR15/ EPWM0TZ[0]/ ECAP2_APWM2/ GP0[7]	EMA_WEB_DQM[1]/ GP2[2]	EMA_D[12]/ GP3[4]	EMA_D[10]/ GP3[2]	EMA_D[1]/ GP4[9]	EMA_CAS/ GP2[4]	EMA_A[22]/ MMCSD0_CMD/ GP4[6]	A
	1	2	3	4	5	6	7	8	9	10	

Figure 3-6. Pin Map (Quad D)

3.7 Pin Multiplexing Control

Device level pin multiplexing is controlled by registers PINMUX0 - PINMUX19 in the SYSCFG module.

For the device family, pin multiplexing can be controlled on a pin-by-pin basis. Each pin that is multiplexed with several different functions has a corresponding 4-bit field in one of the PINMUX registers.

Pin multiplexing selects which of several peripheral pin functions controls the pin's IO buffer **output** data and **output enable** values only. The default pin multiplexing control for almost every pin is to select 'none' of the peripheral functions in which case the pin's IO buffer is held tri-stated.

Note that the **input** from each pin is always routed to **all** of the peripherals that share the pin; the PINMUX registers have no effect on input from a pin.

3.8 Terminal Functions

Table 3-4 to Table 3-28 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin type (I, O, IO, OZ, or PWR), whether the pin/ball has any internal pullup/pulldown resistors, whether the pin/ball is configurable as an IO in GPIO mode, and a functional pin description.

3.8.1 Device Reset, NMI and JTAG

Table 3-4. Reset, NMI and JTAG Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
RESET					
$\overline{\text{RESET}}$	K14	I	IPU	B	Device reset input
$\overline{\text{NMI}}$	J17	I	IPU	B	Non-Maskable Interrupt
$\overline{\text{RESETOUT}}$ / $\overline{\text{UHPI\_HAS}}$/ GP6[15]	T17	O(4)	IPD	C	Reset output
JTAG					
TMS	L16	I	IPU	B	JTAG test mode select
TDI	M16	I	IPU	B	JTAG test data input
TDO	J18	O	IPU	B	JTAG test data output
TCK	J15	I	IPU	B	JTAG test clock
$\overline{\text{TRST}}$	L17	I	IPD	B	JTAG test reset
EMU[0]	J16	I/O	IPU	B	Emulation pin
EMU[1]	K16	I/O	IPU	B	Emulation pin
GP8[0]	K17	I/O	IPD	B	General-purpose input/output

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.
(4) Open drain mode for $\overline{\text{RESETOUT}}$ function.

3.8.2 High-Frequency Oscillator and PLL

Table 3-5. High-Frequency Oscillator and PLL Terminal Functions

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
CLKOUT / UHPI_HDS2 / GP6[14]	T18	O	IPU	C	PLL Observation Clock
1.2-V OSCILLATOR					
OSCIN	L19	I	—	—	Oscillator input
OSCOUT	K19	O	—	—	Oscillator output
OSCVSS	L18	GND	—	—	Oscillator ground (for filter only)
1.2-V PLL0					
PLL0_VDDA	L15	PWR	—	—	PLL analog V_{DD} (1.2-V filtered supply)
PLL0_VSSA	M17	GND	—	—	PLL analog V_{SS} (for filter)
1.2-V PLL1					
PLL1_VDDA	N15	PWR	—	—	PLL analog V_{DD} (1.2-V filtered supply)
PLL1_VSSA	M15	GND	—	—	PLL analog V_{SS} (for filter)

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.3 Real-Time Clock and 32-kHz Oscillator

Table 3-6. Real-Time Clock (RTC) and 1.2-V, 32-kHz Oscillator Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
RTC_XI	J19	I	—	—	RTC 32-kHz oscillator input
RTC_XO	H19	O	—	—	RTC 32-kHz oscillator output
RTC_ALARM / $\overline{\text{UART2\_CTS}}$ / GP0[8] /$\overline{\text{DEEPSLEEP}}$	F4	O	CP[0]	A	RTC Alarm
RTC_CVDD	L14	PWR	—	—	RTC module core power (isolated from chip CV_{DD})
RTC_V_{ss}	H18	GND	—	—	Oscillator ground (for filter)

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.4 DEEPSLEEP Power Control

Table 3-7. DEEPSLEEP Power Control Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
RTC_ALARM / $\overline{\text{UART2\_CTS}}$ / GP0[8] /**DEEPSLEEP**	F4	I	CP[0]	A	DEEPSLEEP power control output

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.5 External Memory Interface A (EMIFA)

Table 3-8. External Memory Interface A (EMIFA) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
EMA_D[15] / GP3[7]	E6	I/O	CP[17]	B	EMIFA data bus
EMA_D[14] / GP3[6]	C7	I/O	CP[17]	B	
EMA_D[13] / GP3[5]	B6	I/O	CP[17]	B	
EMA_D[12] / GP3[4]	A6	I/O	CP[17]	B	
EMA_D[11] / GP3[3]	D6	I/O	CP[17]	B	
EMA_D[10] / GP3[2]	A7	I/O	CP[17]	B	
EMA_D[9] / GP3[1]	D9	I/O	CP[17]	B	
EMA_D[8] / GP3[0]	E10	I/O	CP[17]	B	
EMA_D[7] / GP4[15]	D7	I/O	CP[17]	B	
EMA_D[6] / GP4[14]	C6	I/O	CP[17]	B	
EMA_D[5] / GP4[13]	E7	I/O	CP[17]	B	
EMA_D[4] / GP4[12]	B5	I/O	CP[17]	B	
EMA_D[3] / GP4[11]	E8	I/O	CP[17]	B	
EMA_D[2] / GP4[10]	B8	I/O	CP[17]	B	
EMA_D[1] / GP4[9]	A8	I/O	CP[17]	B	
EMA_D[0] / GP4[8]	C9	I/O	CP[17]	B	

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

Table 3-8. External Memory Interface A (EMIFA) Terminal Functions (continued)

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
EMA_A[23] / MMCSD0_CLK /GP4[7]	E9	O	CP[18]	B	EMIFA address bus
EMA_A[22] / MMCSD0_CMD/GP4[6]	A10	O	CP[18]	B	
EMA_A[21] / MMCSD0_DAT[0] /GP4[5]	B10	O	CP[18]	B	
EMA_A[20] / MMCSD0_DAT[1] /GP4[4]	A11	O	CP[18]	B	
EMA_A[19] / MMCSD0_DAT[2] /GP4[3]	C10	O	CP[18]	B	
EMA_A[18] / MMCSD0_DAT[3] /GP4[2]	E11	O	CP[18]	B	
EMA_A[17] / MMCSD0_DAT[4] /GP4[1]	B11	O	CP[18]	B	
EMA_A[16] / MMCSD0_DAT[5] /GP4[0]	E12	O	CP[18]	B	
EMA_A[15] / MMCSD0_DAT[6] /GP5[15]	C11	O	CP[19]	B	
EMA_A[14] / MMCSD0_DAT[7] /GP5[14]	A12	O	CP[19]	B	
EMA_A[13] / GP5[13]	D11	O	CP[19]	B	
EMA_A[12] / GP5[12]	D13	O	CP[19]	B	
EMA_A[11] / GP5[11]	B12	O	CP[19]	B	
EMA_A[10] / GP5[10]	C12	O	CP[19]	B	
EMA_A[9] / GP5[9]	D12	O	CP[19]	B	
EMA_A[8] / GP5[8]	A13	O	CP[19]	B	
EMA_A[7] / GP5[7]	B13	O	CP[20]	B	
EMA_A[6] / GP5[6]	E13	O	CP[20]	B	
EMA_A[5] / GP5[5]	C13	O	CP[20]	B	
EMA_A[4] / GP5[4]	A14	O	CP[20]	B	
EMA_A[3] / GP5[3]	D14	O	CP[20]	B	
EMA_A[2] / GP5[2]	B14	O	CP[20]	B	
EMA_A[1] / GP5[1]	D15	O	CP[20]	B	
EMA_A[0] / GP5[0]	C14	O	CP[20]	B	
EMA_BA[0] / GP2[8]	C15	O	CP[16]	B	EMIFA bank address
EMA_BA[1] / GP2[9]	A15	O	CP[16]	B	
EMA_CLK / GP2[7]	B7	O	CP[16]	B	EMIFA clock
EMA_SDCKE / GP2[6]	D8	O	CP[16]	B	EMIFA SDRAM clock enable
$\overline{\text{EMA\_RAS}}$ / GP2[5]	A16	O	CP[16]	B	EMIFA SDRAM row address strobe
$\overline{\text{EMA\_CAS}}$ / GP2[4]	A9	O	CP[16]	B	EMIFA SDRAM column address strobe
$\overline{\text{EMA\_CS[0]}}$ / GP2[0]	A18	O	CP[16]	B	EMIFA Async Chip Select
$\overline{\text{EMA\_CS[2]}}$ / GP3[15]	B17	O	CP[16]	B	
$\overline{\text{EMA\_CS[3]}}$ / GP3[14]	A17	O	CP[16]	B	
$\overline{\text{EMA\_CS[4]}}$ / GP3[13]	F9	O	CP[16]	B	
$\overline{\text{EMA\_CS[5]}}$ / GP3[12]	B16	O	CP[16]	B	
EMA_A_$\overline{\text{RW}}$ / GP3[9]	D10	O	CP[16]	B	EMIFA Async Read/Write control
$\overline{\text{EMA\_WE}}$ / GP3[11]	B9	O	CP[16]	B	EMIFA SDRAM write enable
$\overline{\text{EMA\_WEN\_DQM[1]}}$ / GP2[2]	A5	O	CP[16]	B	EMIFA write enable/data mask for EMA_D[15:8]
$\overline{\text{EMA\_WEN\_DQM[0]}}$ / GP2[3]	C8	O	CP[16]	B	EMIFA write enable/data mask for EMA_D[7:0]
$\overline{\text{EMA\_OE}}$ / GP3[10]	B15	O	CP[16]	B	EMIFA output enable
EMA_WAIT[0] / GP3[8]	B18	I	CP[16]	B	EMIFA wait input/interrupt
EMA_WAIT[1] / GP2[1]	B19	I	CP[16]	B	

3.8.6 DDR2 Controller (DDR2)

Table 3-9. DDR2 Controller (DDR2) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE[1]	PULL[2]	DESCRIPTION
DDR_D[15]	W10	I/O	IPD	DDR2 SDRAM data bus
DDR_D[14]	U11	I/O	IPD	
DDR_D[13]	V10	I/O	IPD	
DDR_D[12]	U10	I/O	IPD	
DDR_D[11]	T12	I/O	IPD	
DDR_D[10]	T10	I/O	IPD	
DDR_D[9]	T11	I/O	IPD	
DDR_D[8]	T13	I/O	IPD	
DDR_D[7]	W11	I/O	IPD	
DDR_D[6]	W12	I/O	IPD	
DDR_D[5]	V12	I/O	IPD	
DDR_D[4]	V13	I/O	IPD	
DDR_D[3]	U13	I/O	IPD	
DDR_D[2]	V14	I/O	IPD	
DDR_D[1]	U14	I/O	IPD	
DDR_D[0]	U15	I/O	IPD	
DDR_A[13]	T5	O	IPD	DDR2 row/column address
DDR_A[12]	V4	O	IPD	
DDR_A[11]	T4	O	IPD	
DDR_A[10]	W4	O	IPD	
DDR_A[9]	T6	O	IPD	
DDR_A[8]	U4	O	IPD	
DDR_A[7]	U6	O	IPD	
DDR_A[6]	W5	O	IPD	
DDR_A[5]	V5	O	IPD	
DDR_A[4]	U5	O	IPD	
DDR_A[3]	V6	O	IPD	
DDR_A[2]	W6	O	IPD	
DDR_A[1]	T7	O	IPD	
DDR_A[0]	U7	O	IPD	
DDR_CLKP	W8	O	IPD	DDR2 clock (positive)
$\overline{\text{DDR\_CLKN}}$	W7	O	IPD	DDR2 clock (negative)
DDR_CKE	V7	O	IPD	DDR2 clock enable
$\overline{\text{DDR\_WE}}$	T8	O	IPD	DDR2 write enable
$\overline{\text{DDR\_RAS}}$	W9	O	IPD	DDR2 row address strobe
$\overline{\text{DDR\_CAS}}$	U9	O	IPD	DDR2 column address strobe
$\overline{\text{DDR\_CS}}$	V9	O	IPD	DDR2 chip select
DDR_DQM[0]	W13	O	IPD	DDR2 data mask outputs
DDR_DQM[1]	R10	O	IPD	

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.

Table 3-9. DDR2 Controller (DDR2) Terminal Functions (continued)

SIGNAL		TYPE[1]	PULL[2]	DESCRIPTION
NAME	NO.			
DDR_DQS[0]	T14	I/O	IPD	DDR2 data strobe inputs/outputs
DDR_DQS[1]	V11	I/O	IPD	
DDR_BA[2]	U8	O	IPD	DDR2 SDRAM bank address
DDR_BA[1]	T9	O	IPD	
DDR_BA[0]	V8	O	IPD	
DDR_DQGATE0	R11	O	IPD	DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE1 with same constraints as used for DDR clock and data.
DDR_DQGATE1	R12	I	IPD	DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data.
DDR_ZP	U12	O	—	DDR2 reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm resistor @ 0.5% tolerance.
DDR_VREF	R6	I	—	DDR voltage input for the DDR2/mDDR I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary.
DDR_DVDD18	N6, N9, N10, P7, P8, P9, P10, R7, R8, R9	PWR	—	DDR PHY 1.8V power supply pins

3.8.7 Serial Peripheral Interface Modules (SPI)

Table 3-10. Serial Peripheral Interface (SPI) Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
SPI0					
SPI0_CLK / EPWM0A / GP1[8] / MII_RXCLK	D19	O	CP[7]	A	SPI0 clock
SPI0_ENA / EPWM0B / MII_RXDV	C17	O	CP[7]	A	SPI0 enable
$\overline{\text{SPI0\_SCS[0]}}$ / TM64P1_OUT12 / GP1[6] / MDIO_D / TM64P1_IN12	D17	O	CP[10]	A	SPI0 chip selects
$\overline{\text{SPI0\_SCS[1]}}$ / TM64P0_OUT12 / GP1[7] / MDIO_CLK / TM64P0_IN12	E16	O	CP[10]	A	
$\overline{\text{SPI0\_SCS[2]}}$ / $\overline{\text{UART0\_RTS}}$ / GP8[1] / MII_RXD[0] /SATA_CP_DET	D16	O	CP[9]	A	
$\overline{\text{SPI0\_SCS[3]}}$ / $\overline{\text{UART0\_CTS}}$ / GP8[2] / MII_RXD[1] / SATA_MP_SWITCH	E17	O	CP[9]	A	
$\overline{\text{SPI0\_SCS[4]}}$ / UART0_TXD / GP8[3] / MII_RXD[2]	D18	O	CP[8]	A	
$\overline{\text{SPI0\_SCS[5]}}$ / UART0_RXD / GP8[4] / MII_RXD[3]	C19	O	CP[8]	A	
SPI0_SIMO / EPWMSYNCO / GP8[5] / MII_CRS	C18	I/O/Z	CP[7]	A	SPI0 data slave-in-master-out
SPI0_SOMI / EPWMSYNCI / GP8[6] / MII_RXER	C16	I/O/Z	CP[7]	A	SPI0 data slave-out-master-in
SPI1					
SPI1_CLK / GP2[13]	G19	O	CP[15]	A	SPI1 clock
SPI1_ENA / GP2[12]	H16	O	CP[15]	A	SPI1 enable
$\overline{\text{SPI1\_SCS[0]}}$ / EPWM1B / GP2[14] / TM64P3_IN12	E19	O	CP[14]	A	SPI1 chip selects
$\overline{\text{SPI1\_SCS[1]}}$ / EPWM1A / GP2[15] / TM64P2_IN12	F18	O	CP[14]	A	
$\overline{\text{SPI1\_SCS[2]}}$ / UART1_TXD /SATA_CP_POD /GP1[0]	F19	O	CP[13]	A	
$\overline{\text{SPI1\_SCS[3]}}$ / UART1_RXD /SATA_LED /GP1[1]	E18	O	CP[13]	A	
$\overline{\text{SPI1\_SCS[4]}}$ / UART2_TXD /I2C1_SDA /GP1[2]	F16	O	CP[12]	A	
$\overline{\text{SPI1\_SCS[5]}}$ / UART2_RXD /I2C1_SCL /GP1[3]	F17	O	CP[12]	A	
$\overline{\text{SPI1\_SCS[6]}}$ / I2C0_SDA / TM64P3_OUT12 / GP1[4]	G18	O	CP[11]	A	
$\overline{\text{SPI1\_SCS[7]}}$ / I2C0_SCL / TM64P2_OUT12 / GP1[5]	G16	O	CP[11]	A	
SPI1_SIMO / GP2[10]	G17	I/O/Z	CP[15]	A	SPI1 data slave-in-master-out
SPI1_SOMI / GP2[11]	H17	I/O/Z	CP[15]	A	SPI1 data slave-out-master-in

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.8 Enhanced Capture/Auxiliary PWM Modules (eCAP0)

The eCAP Module pins function as either input captures or auxiliary PWM 32-bit outputs, depending upon how the eCAP module is programmed.

Table 3-11. Enhanced Capture Module (eCAP) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
eCAP0					
AXR0 / **ECAP0_APWM0** / GP8[7] / MII_TXD[0] / CLKS0	F3	I/O	CP[6]	A	enhanced capture 0 input or auxiliary PWM 0 output
eCAP1					
AXR8 / CLKS1 / **ECAP1_APWM1** / GP0[0]	E4	I/O	CP[3]	A	enhanced capture 1 input or auxiliary PWM 1 output
eCAP2					
AXR15 / EPWM0TZ[0] / **ECAP2_APWM2** / GP0[7]	A4	I/O	CP[1]	A	enhanced capture 2 input or auxiliary PWM 2 output

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.9 Enhanced Pulse Width Modulators (eHRPWM)

Table 3-12. Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
eHRPWM0					
SPI0_CLK / **EPWM0A** / GP1[8] / MII_RXCLK	D19	I/O	CP[7]	A	eHRPWM0 A output (with high-resolution)
SPI0_ENA / **EPWM0B** / MII_RXDV	C17	I/O	CP[7]	A	eHRPWM0 B output
AXR15 / **EPWM0TZ[0]** / ECAP2_APWM2 / GP0[7]	A4	I/O	CP[1]	A	eHRPWM0 trip zone input
SPI0_SOMI /**EPWMSYNCI** / GP8[6] / MII_RXER	C16	I/O	CP[7]	A	eHRPWM0 sync input
SPI0_SIMO /**EPWMSYNCO** / GP8[5] / MII_CRS	C18	I/O	CP[7]	A	eHRPWM0 sync output
eHRPWM1					
$\overline{\text{SPI1\_SCS[1]}}$ / **EPWM1A** / GP2[15] / TM64P2_IN12	F18	I/O	CP[14]	A	eHRPWM1 A output (with high-resolution)
$\overline{\text{SPI1\_SCS[0]}}$ / **EPWM1B** / GP2[14] / TM64P3_IN12	E19	I/O	CP[14]	A	eHRPWM1 B output
AXR7 / **EPWM1TZ[0]** / GP1[15]	D2	I/O	CP[4]	A	eHRPWM1 trip zone input

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.10 Boot

Table 3-13. Boot Mode Selection Terminal Functions(1)

SIGNAL NAME	NO.	TYPE(2)	PULL(3)	POWER GROUP(4)	DESCRIPTION
VP_DOUT[15/]/ LCD_D[15]/ UPP_XD[7] /GP7[7] / **BOOT[7]**	P4	I	CP[29]	C	Boot Mode Selection Pins
VP_DOUT[14] /LCD_D[14] /UPP_XD[6] /GP7[6] / **BOOT[6]**	R3	I	CP[29]	C	
VP_DOUT[13] /LCD_D[13] /UPP_XD[5] /GP7[5] / **BOOT[5]**	R2	I	CP[29]	C	
VP_DOUT[12] /LCD_D[12] /UPP_XD[4] / GP7[4] / **BOOT[4]**	R1	I	CP[29]	C	
VP_DOUT[11] /LCD_D[11] /UPP_XD[3] /GP7[3] / **BOOT[3]**	T3	I	CP[29]	C	
VP_DOUT[10] /LCD_D[10] /UPP_XD[2] /GP7[2] / **BOOT[2]**	T2	I	CP[29]	C	
VP_DOUT[9] /LCD_D[9] /UPP_XD[1] /GP7[1] / **BOOT[1]**	T1	I	CP[29]	C	
VP_DOUT[8] /LCD_D[8] /UPP_XD[0] /GP7[0] / **BOOT[0]**	U3	I	CP[29]	C	

(1) Boot decoding is defined in the bootloader application report.
(2) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(3) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.
(4) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.11 Universal Asynchronous Receiver/Transmitters (UART0, UART1, UART2)

Table 3-14. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
UART0					
SPI0_SCS[5] /**UART0_RXD** / GP8[4] / MII_RXD[3]	C19	I	CP[8]	A	UART0 receive data
SPI0_SCS[4] /**UART0_TXD** / GP8[3] / MII_RXD[2]	D18	O	CP[8]	A	UART0 transmit data
SPI0_SCS[2] /**UART0_RTS** / GP8[1] / MII_RXD[0] / SATA_CP_DET	D16	O	CP[9]	A	UART0 ready-to-send output
SPI0_SCS[3] /**UART0_CTS** / GP8[2] / MII_RXD[1] / SATA_MP_SWITCH	E17	I	CP[9]	A	UART0 clear-to-send input
UART1					
SPI1_SCS[3] / **UART1_RXD** / SATA_LED / GP1[1]	E18	I	CP[13]	A	UART1 receive data
SPI1_SCS[2] / **UART1_TXD** / SATA_CP_POD / GP1[0]	F19	O	CP[13]	A	UART1 transmit data
AHCLKR / **UART1_RTS** /GP0[11]	A2	O	CP[0]	A	UART1 ready-to-send output
AHCLKX / USB_REFCLKIN / **UART1_CTS** / GP0[10]	A3	I	CP[0]	A	UART1 clear-to-send input
UART2					
SPI1_SCS[5] / **UART2_RXD** / I2C1_SCL /GP1[3]	F17	I	CP[12]	A	UART2 receive data
SPI1_SCS[4] / **UART2_TXD** / I2C1_SDA /GP1[2]	F16	O	CP[12]	A	UART2 transmit data
AMUTE / **UART2_RTS** / GP0[9]	D5	O	CP[0]	A	UART2 ready-to-send output
RSVD /RTC_ALARM / **UART2_CTS** / GP0[8] /DEEPSLEEP	F4	I	CP[0]	A	UART2 clear-to-send input

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.12 Inter-Integrated Circuit Modules(I2C0, I2C1)

Table 3-15. Inter-Integrated Circuit (I2C) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
I2C0					
$\overline{\text{SPI1\_SCS[6]}}$ / **I2C0_SDA** / TM64P3_OUT12 / GP1[4]	G18	I/O	CP[11]	A	I2C0 serial data
$\overline{\text{SPI1\_SCS[7]}}$ / **I2C0_SCL** / TM64P2_OUT12 / GP1[5]	G16	I/O	CP[11]	A	I2C0 serial clock
I2C1					
$\overline{\text{SPI1\_SCS[4]}}$ / UART2_TXD / **I2C1_SDA** / GP1[2]	F16	I/O	CP[12]	A	I2C1 serial data
$\overline{\text{SPI1\_SCS[5]}}$ / UART2_RXD / **I2C1_SCL** / GP1[3]	F17	I/O	CP[12]	A	I2C1 serial clock

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.13 Timers

Table 3-16. Timers Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
TIMER0					
$\overline{\text{SPI0\_SCS[1]}}$ /TM64P0_OUT12 / GP1[7] /MDIO_CLK /**TM64P0_IN12**	E16	I	CP[10]	A	Timer0 lower input.
$\overline{\text{SPI0\_SCS[1]}}$ /**TM64P0_OUT12** / GP1[7] / MDIO_CLK / TM64P0_IN12	E16	O	CP[10]	A	Timer0 lower output
TIMER1 (Watchdog)					
$\overline{\text{SPI0\_SCS[0]}}$ /TM64P1_OUT12 / GP1[6] / MDIO_D /**TM64P1_IN12**	D17	I	CP[10]	A	Timer1 lower input.
$\overline{\text{SPI0\_SCS[0]}}$ /**TM64P1_OUT12** / GP1[6] / MDIO_D /TM64P1_IN12	D17	O	CP[10]	A	Timer1 lower output
TIMER2					
$\overline{\text{SPI1\_SCS[1]}}$ / EPWM1A / GP2[15] / **TM64P2_IN12**	F18	I	CP[14]	A	Timer2 lower input.
$\overline{\text{SPI1\_SCS[7]}}$ / I2C0_SCL / **TM64P2_OUT12** / GP1[5]	G16	O	CP[11]	A	Timer2 lower output
TIMER3					
$\overline{\text{SPI1\_SCS[0]}}$ / EPWM1B / GP2[14] / **TM64P3_IN12**	E19	I	CP[14]	A	Timer3 lower input.
$\overline{\text{SPI1\_SCS[6]}}$ / I2C0_SDA / **TM64P3_OUT12** / GP1[4]	G18	O	CP[11]	A	Timer3 lower output

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.14 Multichannel Audio Serial Ports (McASP)

Table 3-17. Multichannel Audio Serial Ports Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
McASP0					
AXR15 / EPWM0TZ[0] / ECAP2_APWM2 / GP0[7]	A4	I/O	CP[1]	A	McASP0 serial data
AXR14 / CLKR1 / GP0[6]	B4	I/O	CP[2]	A	
AXR13 / CLKX1 / GP0[5]	B3	I/O	CP[2]	A	
AXR12 / FSR1 / GP0[4]	C4	I/O	CP[2]	A	
AXR11 / FSX1 / GP0[3]	C5	I/O	CP[2]	A	
AXR10 / DR1 / GP0[2]	D4	I/O	CP[2]	A	
AXR9 / DX1 / GP0[1]	C3	I/O	CP[2]	A	
AXR8 / CLKS1 / ECAP1_APWM1 / GP0[0]	E4	I/O	CP[3]	A	
AXR7 / EPWM1TZ[0] / GP1[15]	D2	I/O	CP[4]	A	
AXR6 / CLKR0 / GP1[14] / MII_TXEN	C1	I/O	CP[5]	A	
AXR5 / CLKX0 / GP1[13] / MII_TXCLK	D3	I/O	CP[5]	A	
AXR4 / FSR0 / GP1[12] / MII_COL	D1	I/O	CP[5]	A	
AXR3 / FSX0 / GP1[11] / MII_TXD[3]	E3	I/O	CP[5]	A	
AXR2 / DR0 / GP1[10] / MII_TXD[2]	E2	I/O	CP[5]	A	
AXR1 / DX0 / GP1[9] / MII_TXD[1]	E1	I/O	CP[5]	A	
AXR0 / ECAP0_APWM0 / GP8[7] / MII_TXD[0] / CLKS0	F3	I/O	CP[6]	A	
AHCLKX / USB_REFCLKIN / $\overline{\text{UART1\_CTS}}$ / GP0[10]	A3	I/O	CP[0]	A	McASP0 transmit master clock
ACLKX / GP0[14]	B1	I/O	CP[0]	A	McASP0 transmit bit clock
AFSX / GP0[12]	B2	I/O	CP[0]	A	McASP0 transmit frame sync
AHCLKR / UART1_RTS /GP0[11]	A2	I/O	CP[0]	A	McASP0 receive master clock
ACLKR / GP0[15]	A1	I/O	CP[0]	A	McASP0 receive bit clock
AFSR / GP0[13]	C2	I/O	CP[0]	A	McASP0 receive frame sync
AMUTE / UART2_RTS / GP0[9]	D5	I/O	CP[0]	A	McASP0 mute output

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.15 Multichannel Buffered Serial Ports (McBSP)

Table 3-18. Multichannel Buffered Serial Ports (McBSPs) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
McBSP0					
AXR0 / ECAP0_APWM0 / GP8[7] / MII_TXD[0] / **CLKS0**	F3	I	CP[6]	A	McBSP0 sample rate generator clock input
AXR6 / **CLKR0** / GP1[14] / MII_TXEN	C1	I/O	CP[5]	A	McBSP0 receive clock
AXR4 / **FSR0** / GP1[12] / MII_COL	D1	I/O	CP[5]	A	McBSP0 receive frame sync
AXR2 / **DR0** / GP1[10] / MII_TXD[2]	E2	I	CP[5]	A	McBSP0 receive data
AXR5 / **CLKX0** / GP1[13] / MII_TXCLK	D3	I/O	CP[5]	A	McBSP0 transmit clock
AXR3 / **FSX0** / GP1[11] / MII_TXD[3]	E3	I/O	CP[5]	A	McBSP0 transmit frame sync
AXR1 / **DX0** / GP1[9] / MII_TXD[1]	E1	O	CP[5]	A	McBSP0 transmit data
McBSP1					
AXR8 / **CLKS1** / ECAP1_APWM1 / GP0[0]	E4	I	CP[3]	A	McBSP1 sample rate generator clock input
AXR14 / **CLKR1** / GP0[6]	B4	I/O	CP[2]	A	McBSP1 receive clock
AXR12 / **FSR1** / GP0[4]	C4	I/O	CP[2]	A	McBSP1 receive frame sync
AXR10 / **DR1** / GP0[2]	D4	I	CP[2]	A	McBSP1 receive data
AXR13 / **CLKX1** / GP0[5]	B3	I/O	CP[2]	A	McBSP1 transmit clock
AXR11 / **FSX1** / GP0[3]	C5	I/O	CP[2]	A	McBSP1 transmit frame sync
AXR9 / **DX1** / GP0[1]	C3	O	CP[2]	A	McBSP1 transmit data

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.16 Universal Serial Bus Modules (USB0, USB1)

Table 3-19. Universal Serial Bus (USB) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
USB0 2.0 OTG (USB0)					
USB0_DM	M18	A	—	—	USB0 PHY data minus
USB0_DP	M19	A	—	—	USB0 PHY data plus
USB0_VDDA33	N18	PWR	—	—	USB0 PHY 3.3-V supply
USB0_ID	P16	A	—	—	USB0 PHY identification (mini-A or mini-B plug)
USB0_VBUS	N19	A	—	—	USB0 bus voltage
USB0_DRVVBUS	K18	0	—	B	USB0 controller VBUS control output.
AHCLKX / **USB_REFCLKIN** / $\overline{\text{UART1\_CTS}}$ / GP0[10]	A3	I	CP[0]	A	USB_REFCLKIN. Optional clock input
USB0_VDDA18	N14	PWR	—	—	USB0 PHY 1.8-V supply input
USB0_VDDA12	N17	PWR	—	—	USB0 PHY 1.2-V LDO output for bypass cap
USB_CVDD	M12	PWR	—	—	USB0 and USB1 core logic 1.2-V supply input
USB1 1.1 OHCI (USB1)					
USB1_DM	P18	A	—	—	USB1 PHY data minus
USB1_DP	P19	A	—	—	USB1 PHY data plus
AHCLKX / **USB_REFCLKIN** / $\overline{\text{UART1\_CTS}}$ / GP0[10]	A3	I	CP[0]	A	USB_REFCLKIN. Optional clock input
USB1_VDDA33	P15	PWR	—	—	USB1 PHY 3.3-V supply
USB1_VDDA18	P14	PWR	—	—	USB1 PHY 1.8-V supply
USB_CVDD	M12	PWR	—	—	USB0 and USB1 core logic 1.2-V supply input

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.17 Ethernet Media Access Controller (EMAC)

Table 3-20. Ethernet Media Access Controller (EMAC) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
MII					
AXR6 / CLKR0 / GP1[14] / **MII_TXEN**	C1	O	CP[5]	A	EMAC MII Transmit enable output
AXR5 / CLKX0 / GP1[13] / **MII_TXCLK**	D3	I	CP[5]	A	EMAC MII Transmit clock input
AXR4 / FSR0 / GP1[12] / **MII_COL**	D1	I	CP[5]	A	EMAC MII Collision detect input
AXR3 / FSX0 / GP1[11] / **MII_TXD[3]**	E3	O	CP[5]	A	EMAC MII transmit data
AXR2 / DR0 / GP1[10] / **MII_TXD[2]**	E2	O	CP[5]	A	
AXR1 / DX0 / GP1[9] / **MII_TXD[1]**	E1	O	CP[5]	A	
AXR0 / ECAP0_APWM0 / GP8[7] / **MII_TXD[0]** / CLKS0	F3	O	CP[6]	A	
EPWMSYNCI / GP8[6] / **MII_RXER**	C16	I	CP[7]	A	EMAC MII receive error input
SPI0_SIMO /EPWMSYNCO / GP8[5] / **MII_CRS**	C18	I	CP[7]	A	EMAC MII carrier sense input
SPI0_CLK / EPWM0A / GP1[8] / **MII_RXCLK**	D19	I	CP[7]	A	EMAC MII receive clock input
SPI0_ENA / EPWM0B / **MII_RXDV**	C17	I	CP[7]	A	EMAC MII receive data valid input
$\overline{\text{SPI0\_SCS[5]}}$ /UART0_RXD / GP8[4] / **MII_RXD[3]**	C19	I	CP[8]	A	EMAC MII receive data
$\overline{\text{SPI0\_SCS[4]}}$ /UART0_TXD / GP8[3] / **MII_RXD[2]**	D18	I	CP[8]	A	
$\overline{\text{SPI0\_SCS[3]}}$ /$\overline{\text{UART0\_CTS}}$ / GP8[2] / **MII_RXD[1]** / SATA_MP_SWITCH	E17	I	CP[9]	A	
$\overline{\text{SPI0\_SCS[2]}}$ /$\overline{\text{UART0\_RTS}}$ / GP8[1] / **MII_RXD[0]** / SATA_CP_DET	D16	I	CP[9]	A	
RMII					
VP_DIN[1] / UHPI_HD[9] / UPP_CH1_D[9] / **RMII_MHZ_50_CLK**	W18	I/O	CP[26]	C	EMAC 50-MHz clock input or output
VP_DIN[2] / UHPI_HD[10] / UPP_CH1_D[10] / **RMII_RXER**	W17	I	CP[26]	C	EMAC RMII receiver error
VP_DIN[3] / UHPI_HD[11] / UPP_CH1_D[11] / **RMII_RXD[0]**	V17	I	CP[26]	C	EMAC RMII receive data
VP_DIN[4] / UHPI_HD[12] / UPP_CH1_D[12] / **RMII_RXD[1]**	W16	I	CP[26]	C	
VP_DIN[0] / UHPI_HD[8] / UPP_CH1_D[8] / **RMII_CRS_DV**	W19	I	CP[26]	C	EMAC RMII carrier sense data valid
VP_DIN[5] / UHPI_HD[13] / UPP_CH1_D[13] / **RMII_TXEN**	R14	O	CP[26]	C	EMAC RMII transmit enable
VP_DIN[6] / UHPI_HD[14] / UPP_CH1_D[14] / **RMII_TXD[0]**	V16	O	CP[26]	C	EMAC RMII transmit data
VP_DIN[7] / UHPI_HD[15] / UPP_CH1_D[15] / **RMII_TXD[1]**	U18	O	CP[26]	C	
MDIO					
$\overline{\text{SPI0\_SCS[0]}}$ /TM64P1_OUT12 / GP1[6] / **MDIO_D** / TM64P1_IN12	D17	I/O	CP[10]	A	MDIO serial data

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

Table 3-20. Ethernet Media Access Controller (EMAC) Terminal Functions (continued)

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
$\overline{\text{SPI0\_SCS[1]}}$ /TM64P0_OUT12 / GP1[7] / **MDIO_CLK** / TM64P0_IN12	E16	O	CP[10]	A	MDIO clock

3.8.18 Multimedia Card/Secure Digital (MMC/SD)

Table 3-21. Multimedia Card/Secure Digital (MMC/SD) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
MMCSD0					
EMA_A[23] / **MMCSD0_CLK** / GP4[7]	E9	O	CP[18]	B	MMCSD0 Clock
EMA_A[22] / **MMCSD0_CMD** / GP4[6]	A10	I/O	CP[18]	B	MMCSD0 Command
EMA_A[21] / **MMCSD0_DAT[0]** / GP4[5]	B10	I/O	CP[18]	B	MMC/SD0 data
EMA_A[20] / **MMCSD0_DAT[1]** / GP4[4]	A11	I/O	CP[18]	B	
EMA_A[19] / **MMCSD0_DAT[2]** / GP4[3]	C10	I/O	CP[18]	B	
EMA_A[18] / **MMCSD0_DAT[3]** / GP4[2]	E11	I/O	CP[18]	B	
EMA_A[17] / **MMCSD0_DAT[4]** / GP4[1]	B11	I/O	CP[18]	B	
EMA_A[16] / **MMCSD0_DAT[5]** / GP4[0]	E12	I/O	CP[18]	B	
EMA_A[15] / **MMCSD0_DAT[6]** / GP5[15]	C11	I/O	CP[19]	B	
EMA_A[14] / **MMCSD0_DAT[7]** / GP5[14]	A12	I/O	CP[19]	B	
MMCSD1					
MMCSD1_CLK / UPP_CH0_START / GP8[14]	G2	O	CP[30]	C	MMCSD1 Clock
MMCSD1_CMD / UPP_CH0_ENABLE / GP8[13]	J4	I/O	CP[30]	C	MMCSD1 Command
MMCSD1_DAT[7] / LCD_PCLK /GP8[11]	F1	I/O	CP[31]	C	MMC/SD1 data
MMCSD1_DAT[5] / LCD_HSYNC /GP8[9]	H4	I/O	CP[31]	C	
MMCSD1_DAT[4] / LCD_VSYNC /GP8[8]	G4	I/O	CP[31]	C	
MMCSD1_DAT[6] / LCD_MCLK /GP8[10]	F2	I/O	CP[31]	C	
VP_CLKIN2 / **MMCSD1_DAT[3]** / GP6[4]	H3	I/O	CP[30]	C	
VP_CLKIN3 / **MMCSD1_DAT[1]** / GP6[2]	J3	I/O	CP[30]	C	
VP_CLKOUT2 / **MMCSD1_DAT[2]** / GP6[3]	K3	I/O	CP[30]	C	
MMCSD1_DAT[0] / UPP_CH0_CLK / GP8[15]	G1	I/O	CP[30]	C	

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.19 Liquid Crystal Display Controller(LCD)

Table 3-22. Liquid Crystal Display Controller (LCD) Terminal Functions

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
VP_DOUT[15] / **LCD_D[15]** / UPP_XD[7] / GP7[7] / BOOT[7]	P4	I/O	CP[29]	C	LCD data bus
VP_DOUT[14] / **LCD_D[14]** / UPP_XD[6] / GP7[6] / BOOT[6]	R3	I/O	CP[29]	C	
VP_DOUT[13] / **LCD_D[13]** / UPP_XD[5] / GP7[5] / BOOT[5]	R2	I/O	CP[29]	C	
VP_DOUT[12] / **LCD_D[12]** / UPP_XD[4] / GP7[4] / BOOT[4]	R1	I/O	CP[29]	C	
VP_DOUT[11] / **LCD_D[11]** / UPP_XD[3] / GP7[3] / BOOT[3]	T3	I/O	CP[29]	C	
VP_DOUT[10] / **LCD_D[10]** / UPP_XD[2] / GP7[2] / BOOT[2]	T2	I/O	CP[29]	C	
VP_DOUT[9] / **LCD_D[9]** / UPP_XD[1] / GP7[1] / BOOT[1]	T1	I/O	CP[29]	C	
VP_DOUT[8] / **LCD_D[8]** / UPP_XD[0] / GP7[0] / BOOT[0]	U3	I/O	CP[29]	C	
VP_DOUT[7] / **LCD_D[7]** / UPP_XD[15] / GP7[15]	U2	I/O	CP[28]	C	
VP_DOUT[6] / **LCD_D[6]** / UPP_XD[14] / GP7[14]	U1	I/O	CP[28]	C	
VP_DOUT[5] / **LCD_D[5]** / UPP_XD[13] / GP7[13]	V3	I/O	CP[28]	C	
VP_DOUT[4] / **LCD_D[4]** / UPP_XD[12] / GP7[12]	V2	I/O	CP[28]	C	
VP_DOUT[3] / **LCD_D[3]** / UPP_XD[11] / GP7[11]	V1	I/O	CP[28]	C	
VP_DOUT[2] / **LCD_D[2]** / UPP_XD[10] / GP7[10]	W3	I/O	CP[28]	C	
VP_DOUT[1] / **LCD_D[1]** / UPP_XD[9] / GP7[9]	W2	I/O	CP[28]	C	
VP_DOUT[0] / **LCD_D[0]** / UPP_XD[8] / GP7[8]	W1	I/O	CP[28]	C	
MMCSD1_DAT[7] / **LCD_PCLK** / GP8[11]	F1	O	CP[31]	C	LCD pixel clock
MMCSD1_DAT[5] / **LCD_HSYNC** / GP8[9]	H4	O	CP[31]	C	LCD horizontal sync
MMCSD1_DAT[4] / **LCD_VSYNC** / GP8[8]	G4	O	CP[31]	C	LCD vertical sync
$\overline{\text{LCD\_AC\_ENB\_CS}}$ / GP6[0]	R5	O	CP[31]	C	LCD AC bias enable chip select
MMCSD1_DAT[6] / **LCD_MCLK** / GP8[10]	F2	O	CP[31]	C	LCD memory clock

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.20 Serial ATA Controller (SATA)

Table 3-23. Serial ATA Controller (SATA) Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
SATA_RXP	L1	I	—	—	SATA receive data (positive)
$\overline{\text{SATA\_RXN}}$	L2	I	—	—	SATA receive data (negative)
SATA_TXP	J1	O	—	—	SATA transmit data (positive)
$\overline{\text{SATA\_TXN}}$	J2	O	—	—	SATA transmit data (negative)
SATA_REFCLKP	N2	I	—	—	SATA PHY reference clock (positive)
$\overline{\text{SATA\_REFCLKN}}$	N1	I	—	—	SATA PHY reference clock (negative)
$\overline{\text{SPI0\_SCS[3]}}$ / $\overline{\text{UART0\_CTS}}$ / GP8[2] / MII_RXD[1] / **SATA_MP_SWITCH**	E17	I	CP[9]	A	SATA mechanical presence switch input
$\overline{\text{SPI0\_SCS[2]}}$ / $\overline{\text{UART0\_RTS}}$ / GP8[1] / MII_RXD[0] / **SATA_CP_DET**	D16	I	CP[9]	A	SATA cold presence detect input
$\overline{\text{SPI1\_SCS[2]}}$ / UART1_TXD / **SATA_CP_POD** / GP1[0]	F19	O	CP[13]	A	SATA cold presence power-on output
$\overline{\text{SPI1\_SCS[3]}}$ / UART1_RXD / **SATA_LED** / GP1[1]	E18	O	CP[13]	A	SATA LED control output
SATA_REG	N3	A	—	—	SATA PHY PLL regulator output. Requires an external 0.1uF filter capacitor.
SATA_VDDR	P3	PWR	—	—	SATA PHY 1.8V internal regulator supply
SATA_VDD	M2, P1, P2, N4	PWR	—	—	SATA PHY 1.2V logic supply
SATA_VSS	H1, H2, K1, K2, L3, M1	GND	—	—	SATA PHY ground reference

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.21 Universal Host-Port Interface (UHPI)

Table 3-24. Universal Host-Port Interface (UHPI) Terminal Functions

SIGNAL		TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
NAME	NO.				
VP_DIN[7] / **UHPI_HD[15]** / UPP_CH1_D[15] / RMII_TXD[1]	U18	I/O	CP[26]	C	UHPI data bus
VP_DIN[6] / **UHPI_HD[14]** / UPP_CH1_D[14] / RMII_TXD[0]	V16	I/O	CP[26]	C	
VP_DIN[5] / **UHPI_HD[13]** / UPP_CH1_D[13] / RMII_TXEN	R14	I/O	CP[26]	C	
VP_DIN[4] / **UHPI_HD[12]** / UPP_CH1_D[12] / RMII_RXD[1]	W16	I/O	CP[26]	C	
VP_DIN[3] / **UHPI_HD[11]** / UPP_CH1_D[11] / RMII_RXD[0]	V17	I/O	CP[26]	C	
VP_DIN[2] / **UHPI_HD[10]** / UPP_CH1_D[10] / RMII_RXER	W17	I/O	CP[26]	C	
VP_DIN[1] / **UHPI_HD[9]** / UPP_CH1_D[9] / RMII_MHZ_50_CLK	W18	I/O	CP[26]	C	
VP_DIN[0] / **UHPI_HD[8]** / UPP_CH1_D[8] / RMII_CRS_DV	W19	I/O	CP[26]	C	
VP_DIN[15]_VSYNC / **UHPI_HD[7]** / UPP_CH1_D[7]	V18	I/O	CP[27]	C	
VP_DIN[14]_HSYNC / **UHPI_HD[6]** / UPP_CH1_D[6]	V19	I/O	CP[27]	C	
VP_DIN[13]_FIELD / **UHPI_HD[5]** / UPP_CH1_D[5]	U19	I/O	CP[27]	C	
VP_DIN[12] / **UHPI_HD[4]** / UPP_CH1_D[4]	T16	I/O	CP[27]	C	
VP_DIN[11] / **UHPI_HD[3]** / UPP_CH1_D[3]	R18	I/O	CP[27]	C	
VP_DIN[10] / **UHPI_HD[2]** / UPP_CH1_D[2]	R19	I/O	CP[27]	C	
VP_DIN[9] / **UHPI_HD[1]** / UPP_CH1_D[1]	R15	I/O	CP[27]	C	
VP_DIN[8] / **UHPI_HD[0]** / UPP_CH1_D[0] / GP6[5]	P17	I/O	CP[27]	C	
UHPI_HCNTL0 / UPP_CH1_CLK / GP6[11]	U17	I	CP[24]	C	UHPI access control
UHPI_HCNTL1 / UPP_CH1_START / GP6[10]	W15	I	CP[24]	C	
UHPI_HHWIL / UPP_CH1_ENABLE / GP6[9]	U16	I	CP[24]	C	UHPI half-word identification control
UHPI_HR$\overline{W}$ / UPP_CH1_WAIT / GP6[8]	T15	I	CP[24]	C	UHPI read/write
VP_CLKIN0 / **$\overline{UHPI\_HCS}$** / GP6[7] / UPP_2xTXCLK	W14	I	CP[25]	C	UHPI chip select
VP_CLKIN1 / **$\overline{UHPI\_HDS1}$** / GP6[6]	V15	I	CP[25]	C	UHPI data strobe
CLKOUT / **$\overline{UHPI\_HDS2}$** / GP6[14]	T18	I	CP[22]	C	
$\overline{UHPI\_HINT}$ / GP6[12]	R16	I	CP[23]	C	UHPI host interrupt
UHPI_HRDY / GP6[13]	R17	O	CP[23]	C	UHPI ready
$\overline{RESETOUT}$ / **$\overline{UHPI\_HAS}$** / GP6[15]	T17	I	CP[21]	C	UHPI address strobe

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

3.8.22 Universal Parallel Port (uPP)

Table 3-25. Universal Parallel Port (uPP) Terminal Functions

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
VP_CLKIN0 / $\overline{\text{UHPI\_HCS1}}$ / GP6[7] / **UPP_2xTXCLK**	W14	I	CP[25]	C	uPP 2x transmit clock input
MMCSD1_DAT[0] / **UPP_CH0_CLK** / GP8[15]	G1	I/O	CP[30]	C	uPP channel 0 clock
MMCSD1_CLK / **UPP_CH0_START** / GP8[14]	G2	I/O	CP[30]	C	uPP channel 0 start
MMCSD1_CMD / **UPP_CH0_ENABLE** / GP8[13]	J4	I/O	CP[30]	C	uPP channel 0 enable
UPP_CH0_WAIT / GP8[12]	G3	I/O	CP[30]	C	uPP channel 0 wait
UHPI_CNTL0 / **UPP_CH1_CLK** / GP6[11]	U17	I/O	CP[24]	C	uPP channel 1 clock
UHPI_HCNTL1 / **UPP_CH1_START** / GP6[10]	W15	I/O	CP[24]	C	uPP channel 1 start
UHPI_HHWIL / **UPP_CH1_ENABLE** / GP6[9]	U16	I/O	CP[24]	C	uPP channel 1 enable
UHPI_H$\overline{\text{RW}}$ / **UPP_CH1_WAIT** / GP6[8]	T15	I/O	CP[24]	C	uPP channel 1 wait

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

Table 3-25. Universal Parallel Port (uPP) Terminal Functions (continued)

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
VP_DOUT[7] / LCD_D[7] /**UPP_XD[15]** / GP7[15]	U2	I/O	CP[28]	C	uPP data bus
VP_DOUT[6] / LCD_D[6] /**UPP_XD[14]** / GP7[14]	U1	I/O	CP[28]	C	
VP_DOUT[5] / LCD_D[5] /**UPP_XD[13]** / GP7[13]	V3	I/O	CP[28]	C	
VP_DOUT[4] / LCD_D[4] /**UPP_XD[12]** / GP7[12]	V2	I/O	CP[28]	C	
VP_DOUT[3] / LCD_D[3] /**UPP_XD[11]** / GP7[11]	V1	I/O	CP[28]	C	
VP_DOUT[2] / LCD_D[2] /**UPP_XD[10]** / GP7[10]	W3	I/O	CP[28]	C	
VP_DOUT[1] / LCD_D[1] /**UPP_XD[9]** / GP7[9]	W2	I/O	CP[28]	C	
VP_DOUT[0] / LCD_D[0] /**UPP_XD[8]** / GP7[8]	W1	I/O	CP[28]	C	
VP_DOUT[15] / LCD_D[15] /**UPP_XD[7]** / GP7[7] / BOOT[7]	P4	I/O	CP[29]	C	
VP_DOUT[14] / LCD_D[14] /**UPP_XD[6]** / GP7[6] / BOOT[6]	R3	I/O	CP[29]	C	
VP_DOUT[13] / LCD_D[13] /**UPP_XD[5]** / GP7[5] / BOOT[5]	R2	I/O	CP[29]	C	
VP_DOUT[12] / LCD_D[12] /**UPP_XD[4]** / GP7[4] / BOOT[4]	R1	I/O	CP[29]	C	
VP_DOUT[11] / LCD_D[11] /**UPP_XD[3]** / GP7[3] / BOOT[3]	T3	I/O	CP[29]	C	
VP_DOUT[10] / LCD_D[10] /**UPP_XD[2]** / GP7[2] / BOOT[2]	T2	I/O	CP[29]	C	
VP_DOUT[9] / LCD_D[9] /**UPP_XD[1]** / GP7[1] / BOOT[1]	T1	I/O	CP[29]	C	
VP_DOUT[8] / LCD_D[8] /**UPP_XD[0]** / GP7[0] / BOOT[0]	U3	I/O	CP[29]	C	
VP_DIN[7] / UHPI_HD[15] / **UPP_D[15]** / RMII_TXD[1]	U18	I/O	CP[26]	C	
VP_DIN[6] / UHPI_HD[14] / **UPP_D[14]** / RMII_TXD[0]	V16	I/O	CP[26]	C	
VP_DIN[5] / UHPI_HD[13] / **UPP_D[13]** / RMII_TXEN	R14	I/O	CP[26]	C	
VP_DIN[4] / UHPI_HD[12] / **UPP_D[12]** / RMII_RXD[1]	W16	I/O	CP[26]	C	
VP_DIN[3] / UHPI_HD[11] / **UPP_D[11]** / RMII_RXD[0]	V17	I/O	CP[26]	C	
VP_DIN[2] / UHPI_HD[10] / **UPP_D[10]** / RMII_RXER	W17	I/O	CP[26]	C	
VP_DIN[1] / UHPI_HD[9] / **UPP_D[9]** / RMII_MHZ_50_CLK	W18	I/O	CP[26]	C	
VP_DIN[0] / UHPI_HD[8] / **UPP_D[8]** / RMII_CRS_DV	W19	I/O	CP[26]	C	
VP_DIN[15]_VSYNC / UHPI_HD[7] / **UPP_D[7]**	V18	I/O	CP[27]	C	
VP_DIN[14]_HSYNC / UHPI_HD[6] / **UPP_D[6]**	V19	I/O	CP[27]	C	
VP_DIN[13]_FIELD / UHPI_HD[5] / **UPP_D[5]**	U19	I/O	CP[27]	C	
VP_DIN[12] / UHPI_HD[4] / **UPP_D[4]**	T16	I/O	CP[27]	C	
VP_DIN[11] / UHPI_HD[3] / **UPP_D[3]**	R18	I/O	CP[27]	C	
VP_DIN[10] / UHPI_HD[2] / **UPP_D[2]**	R19	I/O	CP[27]	C	
VP_DIN[9] / UHPI_HD[1] / **UPP_D[1]**	R15	I/O	CP[27]	C	
VP_DIN[8] / UHPI_HD[0] / **UPP_D[0]** / GP6[5]	P17	I/O	CP[27]	C	

3.8.23 Video Port Interface (VPIF)

Table 3-26. Video Port Interface (VPIF) Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	PULL(2)	POWER GROUP(3)	DESCRIPTION
VIDEO INPUT					
VP_CLKIN0 / $\overline{\text{UHPI\_HCS1}}$ / GP6[7] / UPP_2xTXCLK	W14	I	CP[25]	C	VPIF capture channel 0 input clock
VP_CLKIN1 / $\overline{\text{UHPI\_HDS1}}$ / GP6[6]	V15	I	CP[25]	C	VPIF capture channel 1 input clock
VP_DIN[15]_VSYNC / UHPI_HD[7] / UPP_CH1_D[7]	V18	I	CP[27]	C	VPIF capture data bus
VP_DIN[14]_HSYNC / UHPI_HD[6] / UPP_CH1_D[6]	V19	I	CP[27]	C	
VP_DIN[13]_FIELD / UHPI_HD[5] / UPP_CH1_D[5]	U19	I	CP[27]	C	
VP_DIN[12] / UHPI_HD[4] / UPP_CH1_D[4]	T16	I	CP[27]	C	
VP_DIN[11] / UHPI_HD[3] / UPP_CH1_D[3]	R18	I	CP[27]	C	
VP_DIN[10] / UHPI_HD[2] / UPP_CH1_D[2]	R19	I	CP[27]	C	
VP_DIN[9] / UHPI_HD[1] / UPP_CH1_D[1]	R15	I	CP[27]	C	
VP_DIN[8] / UHPI_HD[0] / UPP_CH1_D[0] / GP6[5]	P17	I	CP[27]	C	
VP_DIN[7] / UHPI_HD[15] / UPP_CH1_D[15] / RMII_TXD[1]	U18	I	CP[26]	C	
VP_DIN[6] / UHPI_HD[14] / UPP_CH1_D[14] / RMII_TXD[0]	V16	I	CP[26]	C	
VP_DIN[5] / UHPI_HD[13] / UPP_CH1_D[13] / RMII_TXEN	R14	I	CP[26]	C	
VP_DIN[4] / UHPI_HD[12] / UPP_CH1_D[12] / RMII_RXD[1]	W16	I	CP[26]	C	
VP_DIN[3] / UHPI_HD[11] / UPP_CH1_D[11] / RMII_RXD[0]	V17	I	CP[26]	C	
VP_DIN[2] / UHPI_HD[10] / UPP_CH1_D[10] / RMII_RXER	W17	I	CP[26]	C	
VP_DIN[1] / UHPI_HD[9] / UPP_CH1_D[9] / RMII_MHZ_50_CLK	W18	I	CP[26]	C	
VP_DIN[0] / UHPI_HD[8] / UPP_CH1_D[8] / RMII_CRS_DV	W19	I	CP[26]	C	
VIDEO OUTPUT					
VP_CLKIN2 / MMCSD1_DAT[3] / GP6[4]	H3	I	CP[30]	C	VPIF display channel 2 input clock
VP_CLKOUT2 / MMCSD1_D2 / GP6[3]	K3	O	CP[30]	C	VPIF display channel 2 output clock
VP_CLKIN3 / MMCSD1_DAT[1] / GP6[2]	J3	I	CP[30]	C	VPIF display channel 3 input clock
VP_CLKOUT3 / GP6[1]	K4	O	CP[30]	C	VPIF display channel 3 output clock

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are weakly pulled down. If the application requires a pull-up, an external pull-up can be used.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

Table 3-26. Video Port Interface (VPIF) Terminal Functions (continued)

SIGNAL		TYPE[1]	PULL[2]	POWER GROUP[3]	DESCRIPTION
NAME	NO.				
VP_DOUT[15] / LCD_D[15] /UPP_XD[7] / GP7[7] / BOOT[7]	P4	O	CP[29]	C	VPIF display data bus
VP_DOUT[14] / LCD_D[14] / UPP_XD[6] / GP7[6] / BOOT[6]	R3	O	CP[29]	C	
VP_DOUT[13] / LCD_D[13] /UPP_XD[5] / GP7[5] / BOOT[5]	R2	O	CP[29]	C	
VP_DOUT[12] / LCD_D[12] /UPP_XD[4] / GP7[4] / BOOT[4]	R1	O	CP[29]	C	
VP_DOUT[11] / LCD_D[11] /UPP_XD[3] / GP7[3] / BOOT[3]	T3	O	CP[29]	C	
VP_DOUT[10] / LCD_D[10] /UPP_XD[2] / GP7[2] / BOOT[2]	T2	O	CP[29]	C	
VP_DOUT[9] / LCD_D[9] /UPP_XD[1] / GP7[1] / BOOT[1]	T1	O	CP[29]	C	
VP_DOUT[8] / LCD_D[8] /UPP_XD[0] / GP7[0] / BOOT[0]	U3	O	CP[29]	C	
VP_DOUT[7] / LCD_D[7] /UPP_XD[15] / GP7[15]	U2	O	CP[28]	C	
VP_DOUT[6] / LCD_D[6] /UPP_XD[14] / GP7[14]	U1	O	CP[28]	C	
VP_DOUT[5] / LCD_D[5] /UPP_XD[13] / GP7[13]	V3	O	CP[28]	C	
VP_DOUT[4] / LCD_D[4] /UPP_XD[12] / GP7[12]	V2	O	CP[28]	C	
VP_DOUT[3] / LCD_D[3] /UPP_XD[11] / GP7[11]	V1	O	CP[28]	C	
VP_DOUT[2] / LCD_D[2] /UPP_XD[10] / GP7[10]	W3	O	CP[28]	C	
VP_DOUT[1] / LCD_D[1] /UPP_XD[9] / GP7[9]	W2	O	CP[28]	C	
VP_DOUT[0] /LCD_D[0] /UPP_XD[8] / GP7[8]	W1	O	CP[28]	C	

3.8.24 Reserved and No Connect

Table 3-27. Reserved and No Connect Terminal Functions

SIGNAL		TYPE[1]	DESCRIPTION
NAME	NO.		
RSV2	T19	PWR	Reserved. For proper device operation, this pin **must** be tied directly to CV_{DD}.
NC	M3, M14, N16	—	No connect (Leave unconnected, ***do not*** connect to power or ground.)

(1) PWR = Supply voltage.

3.8.25 Supply and Ground

Table 3-28. Supply and Ground Terminal Functions

SIGNAL		TYPE(1)	DESCRIPTION
NAME	NO.		
CVDD (Core supply)	E15, G7, G8, G13, H6, H7, H10, H11, H12, H13, J6, J12, K6, K12, L12, M8, M9, N8	PWR	1.2-V core supply voltage pins
RVDD (Internal RAM supply)	E5, H14, N7	PWR	1.2V internal ram supply voltage pins
DVDD18 (I/O supply)	F14, G6, G10, G11, G12, J13, K5, L6, N6, N9, N10, P7, P8, P9, P10, P13, R7, R8, R9, R13	PWR	1.8V I/O supply voltage pins
DVDD3318_A (I/O supply)	F5, F15, G5, G14, G15, H5	PWR	1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group A
DVDD3318_B (I/O supply)	E14, F6, F7, F8, F10, F11, F12, F13, G9, J14, K15	PWR	1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group B
DVDD3318_C (I/O supply)	J5, K13, L4, L13, M13, N13, P5, P6, P12, R4	PWR	1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group C
VSS (Ground)	A19, H8, H9, H15, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L5, L7, L8, L9, L10, L11, M4, M5, M6, M7, M10, M11, N5, N11, N12, P11	GND	Ground pins.

(1) PWR = Supply voltage, GND - Ground.

4 Device Configuration

4.1 Boot Modes

This device supports a variety of boot modes through an internal DSP ROM bootloader. This device does not support dedicated hardware boot modes; therefore, all boot modes utilize the internal DSP ROM. The input states of the BOOT pins are sampled and latched into the BOOTCFG register, which is part of the system configuration (SYSCFG) module, when device reset is deasserted. Boot mode selection is determined by the values of the BOOT pins.

See *Using the D800K001 Bootloader Application Report* (SPRAB04) for more details on the ROM Boot Loader.

The following boot modes are supported:

- NAND Flash boot
  - 8-bit NAND
- NOR Flash boot
  - NOR Direct boot (8-bit or 16-bit)
  - NOR Legacy boot (8-bit or 16-bit)
  - NOR AIS boot (8-bit or 16-bit)
- HPI Boot
- I2C0/I2C1 Boot
  - EEPROM (Master Mode)
  - External Host (Slave Mode)
- SPI0/SPI1 Boot
  - Serial Flash (Master Mode)
  - SERIAL EEPROM (Master Mode)
  - External Host (Slave Mode)
- UART0/UART1/UART2 Boot
  - External Host

4.2 SYSCFG Module

The following system level features of the chip are controlled by the SYSCFG peripheral:

- Readable Device, Die, and Chip Revision ID
- Control of Pin Multiplexing
- Priority of bus accesses different bus masters in the system
- Capture at power on reset the chip BOOT pin values and make them available to software
- Control of the DeepSleep power management function
- Enable and selection of the programmable pin pullups and pulldowns
- Special case settings for peripherals:
  - Locking of PLL controller settings
  - Default burst sizes for EDMA3 transfer controllers
  - Selection of the source for the eCAP module input capture (including on chip sources)
  - McASP AMUTEIN selection and clearing of AMUTE status for the McASP
  - Control of the reference clock source and other side-band signals for both of the integrated USB PHYs
  - Clock source selection for EMIFA
  - DDR2 Controller PHY settings
  - SATA PHY power management controls
- Selects the source of emulation suspend signal (from DSP) of peripherals supporting this function.

Since the SYSCFG peripheral controls global operation of the device, its registers are protected against erroneous accesses by several mechanisms:

- A special key sequence must be written to KICK0, KICK1 registers before any other registers are writeable.
- Additionally, many registers are accessible only by a host (DSP) when it is operating in its privileged mode. (ex. from the kernel, but not from user space code).

Table 4-1. System Configuration (SYSCFG) Module Register Access

Register Address	Register Name	Register Description	Register Access
0x01C1 4000	REVID	Revision Identification Register	—
0x01C14008	DIEIDR0	Device Identification Register 0	—
0x01C1400C	DIEIDR1	Device Identification Register 1	—
0x01C14010	DIEIDR2	Device Identification Register 2	—
0x01C14014	DIEIDR3	Device Identification Register 3	—
0x01C1 4020	BOOTCFG	Boot Configuration Register	Privileged mode
0x01C1 4038	KICK0R	Kick 0 Register	Privileged mode
0x01C1 403C	KICK1R	Kick 1 Register	Privileged mode
0x01C1 4044	HOST1CFG	Host 1 Configuration Register	—
0x01C1 40E0	IRAWSTAT	Interrupt Raw Status/Set Register	Privileged mode
0x01C1 40E4	IENSTAT	Interrupt Enable Status/Clear Register	Privileged mode
0x01C1 40E8	IENSET	Interrupt Enable Register	Privileged mode
0x01C1 40EC	IENCLR	Interrupt Enable Clear Register	Privileged mode
0x01C1 40F0	EOI	End of Interrupt Register	Privileged mode
0x01C1 40F4	FLTADDRR	Fault Address Register	Privileged mode
0x01C1 40F8	FLTSTAT	Fault Status Register	—
0x01C1 4110	MSTPRI0	Master Priority 0 Registers	Privileged mode
0x01C1 4114	MSTPRI1	Master Priority 1 Registers	Privileged mode
0x01C1 4118	MSTPRI2	Master Priority 2 Registers	Privileged mode
0x01C1 4120	PINMUX0	Pin Multiplexing Control 0 Register	Privileged mode
0x01C1 4124	PINMUX1	Pin Multiplexing Control 1 Register	Privileged mode
0x01C1 4128	PINMUX2	Pin Multiplexing Control 2 Register	Privileged mode
0x01C1 412C	PINMUX3	Pin Multiplexing Control 3 Register	Privileged mode
0x01C1 4130	PINMUX4	Pin Multiplexing Control 4 Register	Privileged mode
0x01C1 4134	PINMUX5	Pin Multiplexing Control 5 Register	Privileged mode
0x01C1 4138	PINMUX6	Pin Multiplexing Control 6 Register	Privileged mode
0x01C1 413C	PINMUX7	Pin Multiplexing Control 7 Register	Privileged mode
0x01C1 4140	PINMUX8	Pin Multiplexing Control 8 Register	Privileged mode
0x01C1 4144	PINMUX9	Pin Multiplexing Control 9 Register	Privileged mode
0x01C1 4148	PINMUX10	Pin Multiplexing Control 10 Register	Privileged mode
0x01C1 414C	PINMUX11	Pin Multiplexing Control 11 Register	Privileged mode
0x01C1 4150	PINMUX12	Pin Multiplexing Control 12 Register	Privileged mode
0x01C1 4154	PINMUX13	Pin Multiplexing Control 13 Register	Privileged mode
0x01C1 4158	PINMUX14	Pin Multiplexing Control 14 Register	Privileged mode
0x01C1 415C	PINMUX15	Pin Multiplexing Control 15 Register	Privileged mode
0x01C1 4160	PINMUX16	Pin Multiplexing Control 16 Register	Privileged mode
0x01C1 4164	PINMUX17	Pin Multiplexing Control 17 Register	Privileged mode
0x01C1 4168	PINMUX18	Pin Multiplexing Control 18 Register	Privileged mode
0x01C1 416C	PINMUX19	Pin Multiplexing Control 19 Register	Privileged mode
0x01C1 4170	SUSPSRC	Suspend Source Register	Privileged mode

Table 4-1. System Configuration (SYSCFG) Module Register Access (continued)

Register Address	Register Name	Register Description	Register Access
0x01C1 4174	CHIPSIG	Chip Signal Register	—
0x01C1 4178	CHIPSIG_CLR	Chip Signal Clear Register	—
0x01C1 417C	CFGCHIP0	Chip Configuration 0 Register	Privileged mode
0x01C1 4180	CFGCHIP1	Chip Configuration 1 Register	Privileged mode
0x01C1 4184	CFGCHIP2	Chip Configuration 2 Register	Privileged mode
0x01C1 4188	CFGCHIP3	Chip Configuration 3 Register	Privileged mode
0x01C1 418C	CFGCHIP4	Chip Configuration 4 Register	Privileged mode
0x01E2 C000	VTPIO_CTL	VTPIO COntrol Register	Privileged mode
0x01E2 C004	DDR_SLEW	DDR Slew Register	Privileged mode
0x01E2 C008	DeepSleep	DeepSleep Register	Privileged mode
0x01E2 C00C	PUPD_ENA	Pullup / Pulldown Enable Register	Privileged mode
0x01E2 C010	PUPD_SEL	Pullup / Pulldown Selection Register	Privileged mode
0x01E2 C014	RXACTIVE	RXACTIVE Control Register	Privileged mode
0x01E2 C018	PWRDN	PWRDN Control Register	Privileged mode

5 Device Operating Conditions

5.1 Absolute Maximum Ratings Over Operating Junction Temperature Range (Unless Otherwise Noted) (1)

Supply voltage ranges	Core Logic, Variable and Fixed (CVDD, RVDD, RTC_CVDD, PLL0_VDDA , PLL1_VDDA , SATA_VDD, USB_CVDD(2),) (3)	-0.5 V to 1.4 V
	I/O, 1.8V (USB0_VDDA18, USB1_VDDA18, SATA_VDDR, DDR_DVDD18) (3)	-0.5 V to 2 V
	I/O, 3.3V (DVDD3318_A, DVDD3318_B, DVDD3318_C, USB0_VDDA33, USB1_VDDA33) (3)	-0.5 V to 3.8V
Input voltage (V_I) ranges	Oscillator inputs (OSCIN, RTC_XI), 1.2V	-0.3 V to CVDD + 0.3V
	Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State)	-0.3V to DVDD + 0.3V
	Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Transient)	DVDD + 20% up to 20% of Signal Period
	USB 5V Tolerant IOs: (USB0_DM, USB0_DP, USB0_ID, USB1_DM, USB1_DP)	5.25V(4)
	USB0 VBUS Pin	5.50V(4)
Output voltage (V_O) ranges	Dual-voltage LVCMOS outputs, 3.3V or 1.8V (Steady State)	-0.5 V to DVDD + 0.3V
	Dual-voltage LVCMOS outputs, 3.3V or 1.8V (Transient)	DVDD + 20% up to 20% of Signal Period
Clamp Current	Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the I/O's internal diode protection cells.	±20mA
Operating Junction Temperature ranges, T_J	Commercial (default)	0°C to 90°C
	Extended (A version)	-40°C to 105°C
Storage temperature range, T_{stg}	(default)	-55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is an internal LDO output and connected via 0.22 F capacitor to VSS
(3) All voltage values are with respect to VSS, USB0_VSSA33, USB0_VSSA, PLL0_VSSA, OSCVSS, RTC_VSS
(4) Up to a maximum of 24 hours.

PRODUCT PREVIEW

5.2 Recommended Operating Conditions

	NAME	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Supply Voltage	CVDD	Core Logic Supply Voltage (variable)	1.2V operating point	1.14	1.2 or 1.26	1.32	V
			1.1V operating point	1.05	1.1	1.16	V
			1.0V operating point	0.95	1.0	1.05	V
	RVDD	Internal RAM Supply Voltage		1.14	1.2 or 1.26	1.32	V
	RTC_CVDD	RTC Core Logic Supply Voltage		1.14	1.2 or 1.26	1.32	V
	PLL0_VDDA	PLL0 Supply Voltage		1.14	1.2 or 1.26	1.32	V
	PLL1_VDDA	PLL1 Supply Voltage		1.14	1.2 or 1.26	1.32	V
	SATA_VDD	SATA Core Logic Supply Voltage		1.14	1.2 or 1.26	1.32	V
	USB_CVDD(1)	USB0, USB1 Core Logic Supply Voltage		1.14	1.2 or 1.26	1.32	V
	USB0_VDDA18	USB0 PHY Supply Voltage		1.71	1.8	1.89	V
	USB0_VDDA33	USB0 PHY Supply Voltage		3.15	3.3	3.45	V
	USB1_VDDA18	USB1 IO Supply Voltage		1.71	1.8	1.89	V
	USB1_VDDA33	USB1 IO Supply Voltage		3.15	3.3	3.45	V
	SATA_VDDR	SATA PHY Internal Regulator Supply Voltage		1.71	1.8	1.89	V
	DDR_DVDD18	DDR2 PHY Supply Voltage		1.71	1.8	1.89	V
	DDR_VREF	DDR2/mDDR reference voltage		0.49* DDR_DVDD18	0.5* DDR_DVDD18	0.51* DDR_DVDD18	V
	DDR_ZP	DDR2/mDDR impedance control, connected via 200Ω resistor to Vss			Vss		V
	DVDD3318_A	Power Group A Dual-voltage IO Supply Voltage	1.8V operating point	1.71	1.8	1.89	V
			3.3V operating point	3.15	3.3	3.45	V
	DVDD3318_B	Power Group B Dual-voltage IO Supply Voltage	1.8V operating point	1.71	1.8	1.89	V
			3.3V operating point	3.15	3.3	3.45	V
	DVDD3318_C	Power Group C Dual-voltage IO Supply Voltage	1.8V operating point	1.71	1.8	1.89	V
			3.3V operating point	3.15	3.3	3.45	V
Supply Ground	VSS	Core Logic Digital Ground		0	0	0	V
	PLL0_VSSA	PLL0 Ground					V
	PLL1_VSSA	PLL1 Ground					V
	SATA_VSS	SATA PHY Ground					V
	OSCVSS(2)	Oscillator Ground					V
	RTC_VSS(2)	RTC Oscillator Ground					V
	USB0_VSSA	USB0 PHY Ground					V
	USB0_VSSA33	USB0 PHY Ground					V
Voltage Input High	V_{IH}	High-level input voltage, Dual-voltage I/O, 3.3V(3)		2			V
		High-level input voltage, Dual-voltage I/O, 1.8V (3)		0.65*DVDD			V
		High-level input voltage, RTC_XI		0.8*RTC_CVDD			V
		High-level input voltage, OSCIN		0.8*CVDD			V
		High-level input voltage, SATA_REFCLKP and SATA_REFCLKN		TBD			V
Voltage Input Low	V_{IL}	Low-level input voltage, Dual-voltage I/O, 3.3V(3)				0.8	V
		High-level input voltage, Dual-voltage I/O, 1.8V (3)				0.35*DVDD	V
		Low-level input voltage, RTC_XI				0.2*RTC_CVDD	V
		Low-level input voltage, OSCIN				0.2*CVDD	V
		Low-level input voltage, SATA_REFCLKP and SATA_REFCLKN				TBD	V
Transition Time	t_t	10%-90%, All Inputs (except SATA, USB0 and DDR2)				5	ns

(1) This pin is an internal LDO output and connected via 0.22 F capacitor to VSS
(2) When an external crystal is used oscillator (OSC_VSS, RTC_VSS) ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground. These pins are shorted to VSS on the device itself and should not be connected to VSS on the circuit board. If a crystal is not used and the clock input is driven directly, then the oscillator VSS may be connected to board ground.
(3) These IO specifications apply to the dual-voltage IOs only and do not apply to DDR2/mDDR or SATA interfaces. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.

Recommended Operating Conditions *(continued)*

	NAME	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Operating Frequency	$F_{SYSCLK1,6}$	Commercial temperature grade (default)	CVDD = 1.2V operating point	0		300	MHz
			CVDD = 1.1V operating point	0		200	
			CVDD = 1.0V operating point	0		100	
		Extended temperature grade (A suffix)	CVDD = 1.2V operating point	0		300	MHz
			CVDD = 1.1V operating point	0		200	
			CVDD = 1.0V operating point	0		100	

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5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Junction Temperature (Unless Otherwise Noted)

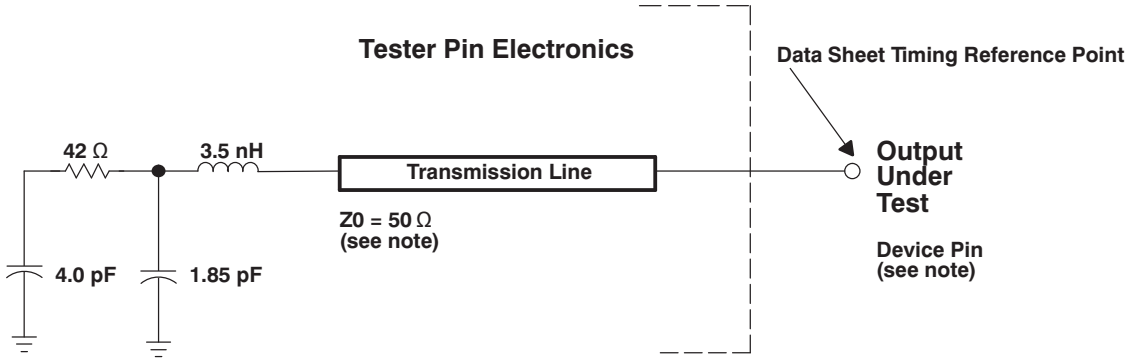
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Low/full speed: USB0_DM and USB0_DP		2.8		USB0_VDDA33	V
	High speed: USB_DM and USB_DP		360		440	mV
	Low/full speed: USB1_DM and USB1_DP		2.8		USB1_VDDA33	V
	High-level output voltage (dual-voltage LVCMOS IOs at 3.3V)(1)	DVDD = 3.15V, I_{OH} = -4 mA	2.4			V
		DVDD = 3.15V, I_{OH} = -100 µA	2.95			V
	High-level output voltage (dual-voltage LVCMOS IOs at 1.8V)(1)	DVDD = 1.65V, I_{OH} = -2 mA	DVDD-0.45			V
V_{OL}	Low/full speed: USB_DM and USB_DP		0.0		0.3	V
	High speed: USB_DM and USB_DP		-10		10	mV
	Low-level output voltage (dual-voltage LVCMOS I/Os at 3.3V)	DVDD = 3.15V, I_{OL} = 4mA			0.4	V
		DVDD = 3.15V, I_{OL} = -100 µA			0.2	V
	Low-level output voltage (dual-voltage LVCMOS I/Os at 1.8V)	DVDD = 1.65V, I_{OL} = 2mA			0.45	V
I_I (2)	Input current(1) (dual-voltage LVCMOS I/Os)	V_I = VSS to DVDD without opposing internal resistor			±9	µA
		V_I = VSS to DVDD with opposing internal pullup resistor (3)	70		310	µA
		V_I = VSS to DVDD with opposing internal pulldown resistor (3)	-75		-270	µA
I_{OH}	High-level output current(1) (dual-voltage LVCMOS I/Os)	All peripherals			-6	mA
I_{OL}	Low-level output current(1) (dual-voltage LVCMOS I/Os)	All peripherals			6	mA
Capacitance	Input capacitance (dual-voltage LVCMOS)			3		pF
	Output capacitance (dual-voltage LVCMOS)			3		pF

(1) These IO specifications apply to the dual-voltage IOs only and do not apply to DDR2/mDDR or SATA interfaces. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.
(2) I_I applies to input-only pins and bi-directional pins. For input-only pins, I_I indicates the input leakage current. For bi-directional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.
(3) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

6 Peripheral Information and Electrical Specifications

6.1 Parameter Information

6.1.1 Parameter Information Device-Specific Information



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 6-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.1.1.1 Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. For 3.3 V I/O, V_{ref} = 1.65 V. For 1.8 V I/O, V_{ref} = 0.9 V.

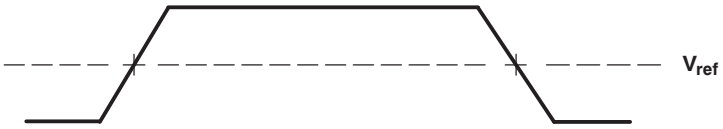


Figure 6-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL}MAX and V_{OH} MIN for output clocks

Figure 6-3. Rise and Fall Transition Time Voltage Reference Levels

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6.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

6.3 Power Supplies

6.3.1 Power-on Sequence

The device should be powered-on in the following order:

- 1) RTC (RTC_CVDD) may be powered from an external device (such as a battery) prior to all other supplies being applied. If the RTC is not used, RTC_CVDD should be connected to CVDD.
- 2a) All variable 1.2V - 1.0V core logic supplies (CVDD)
- 2b) All static 1.2V logic supplies (RVDD, VDDA_12_PLL0, VDDA_12_PLL1, USB_CVDD, SATA_VDD). If voltage scaling is not used on the device, groups 2a) and 2b) can be controlled from the same power supply and powered up together.
- 3) All static 1.8V IO supplies (DVDD18, DDR_DVDD18, USB0_VDDA18, USB1_VDDA18 and SATA_VDDR) and any of the LVCMOS IO supply groups used at 1.8V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).
- 4) All analog 3.3V PHY supplies (USB0_VDDA33 and USB1_VDDA33; these are not required if both USB0 and USB1 are not used) and any of the LVCMOS IO supply groups used at 3.3V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).

There is no specific required voltage ramp rate for any of the supplies as long as the LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed the STATIC 1.8V supplies by more than 2 volts.

6.3.2 Power-off Sequence

The power supplies can be powered-off in any order as long as LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed static 1.8V supplies by more than 2 volts. There is no specific required voltage ramp down rate for any of the supplies (except as required to meet the above mentioned voltage condition).

6.4 Reset

6.4.1 Power-On Reset (POR)

A power-on reset (POR) is required to place the device in a known good state after power-up. Power-On Reset is initiated by bringing RESET and TRST low at the same time. POR sets all of the device internal logic to its default state. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence. RESETOUT is an output for use by other controllers in the system that indicates the device is currently in reset.

A summary of the effects of Power-On Reset is given below:

- All internal logic (including emulation logic and the PLL logic) is reset to its default state
- Internal memory is not maintained through a POR
- RESETOUT goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a POR. A software sequence is required to reset the RTC

A watchdog reset triggers a POR.

6.4.2 Warm Reset

A warm reset provides a limited reset to the device. Warm Reset is initiated by bringing only RESET low (TRST is maintained high through a warm reset). Warm reset sets certain portions of the device to their default state while leaving others unaltered. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence. RESETOUT is an output for use by other controllers in the system that indicates the device is currently in reset.

A summary of the effects of Warm Reset is given below:

- All internal logic (except for the emulation logic and the PLL logic) is reset to its default state
- Internal memory is maintained through a warm reset
- RESETOUT goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a warm reset. A software sequence is required to reset the RTC

6.4.3 Reset Electrical Data Timings

Table 6-1 assumes testing over the recommended operating conditions.

Table 6-1. Reset Timing Requirements ((1), (2))

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{w(RSTL)}$	Pulse width, $\overline{RESET}$/$\overline{TRST}$ low	100		100		100		ns
2	$t_{su(BPV-RSTH)}$	Setup time, boot pins valid before $\overline{RESET}$/$\overline{TRST}$ high	20		20		20		ns
3	$t_{h(RSTH-BPV)}$	Hold time, boot pins valid after $\overline{RESET}$/$\overline{TRST}$ high	20		20		20		ns
4	$t_{d(RSTH-RESETOUTH)}$	$\overline{RESET}$ high to $\overline{RESETOUT}$ high; Warm reset		14		16		20	cycles(3)
		$\overline{RESET}$ high to $\overline{RESETOUT}$ high; Power-on Reset		14		16		20	
5	$t_{d(RSTL-RESETOUTL)}$	Delay time, $\overline{RESET}$/$\overline{TRST}$ low to $\overline{RESETOUT}$ low		14		16		20	ns

(1) $\overline{RESETOUT}$ is multiplexed with other pin functions. See the Terminal Functions table, Table 3-4 for details.
(2) For power-on reset (POR), the reset timings in this table refer to $\overline{RESET}$ and $\overline{TRST}$ together. For warm reset, the reset timings in this table refer to $\overline{RESET}$ only ($\overline{TRST}$ is held high).
(3) OSCIN cycles.

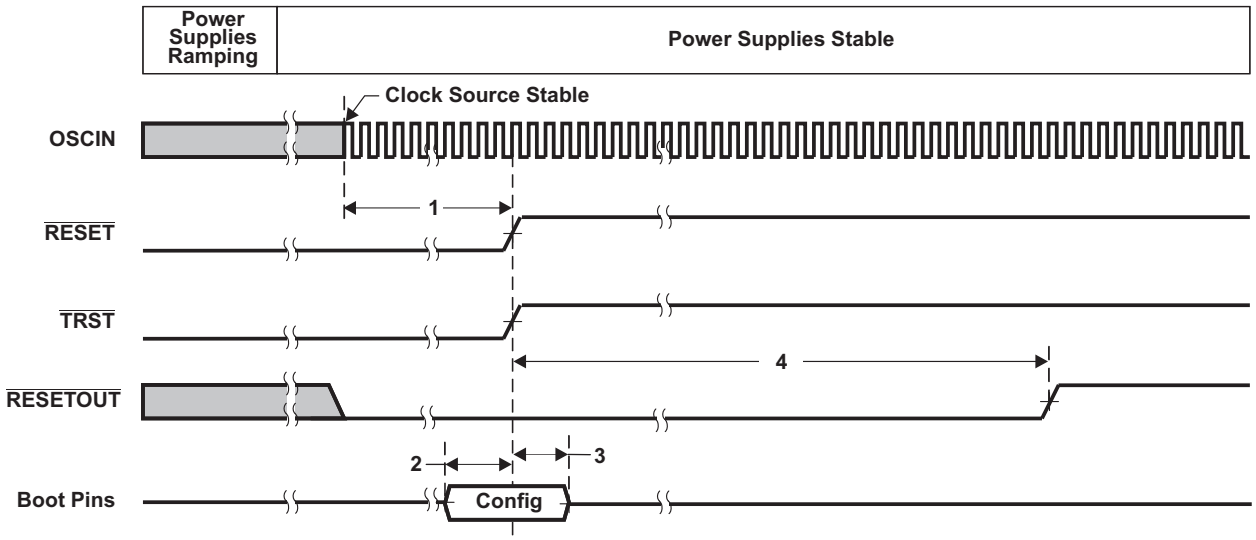

Figure 6-4. Power-On Reset (RESET and TRST active) Timing

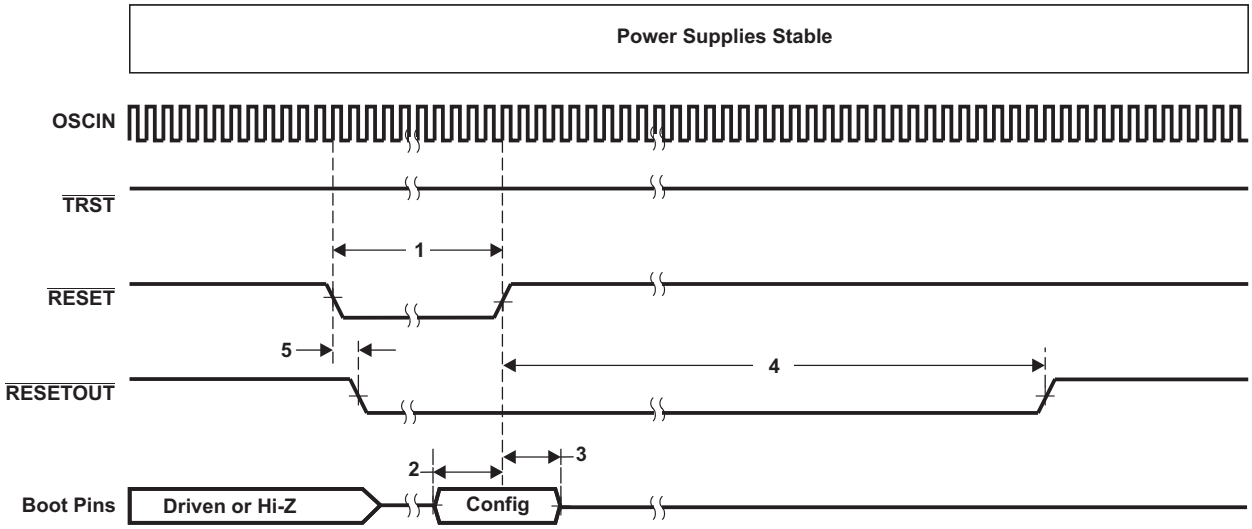

Figure 6-5. Warm Reset (RESET active, TRST high) Timing

6.5 Crystal Oscillator or External Clock Input

The device includes two choices to provide an external clock input, which is fed to the on-chip PLLs to generate high-frequency system clocks. These options are illustrated in Figure 6-6 and Figure 6-7. For input clock frequencies between 12 and 20 MHz, a crystal with 80 ohm max ESR is recommended. For input clock frequencies between 20 and 30 MHz, a crystal with 60 ohm max ESR is recommended. Typical C1, C2 values are 10-20 pF.

Figure 6-6 illustrates the option that uses on-chip 1.2V oscillator with external crystal circuit. Figure 6-7 illustrates the option that uses an external 1.2V clock input.

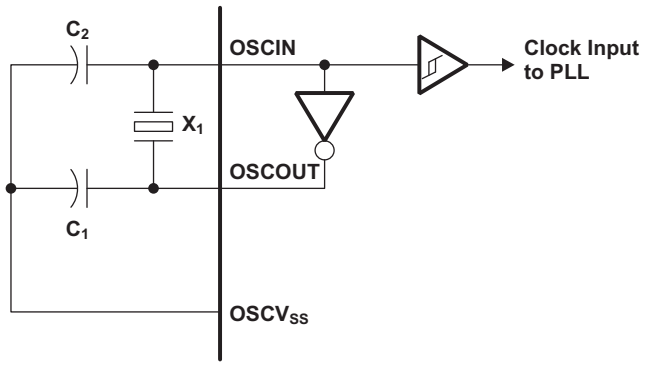

Figure 6-6. On-Chip Oscillator

Table 6-2. Oscillator Timing Requirements

PARAMETER		MIN	MAX	UNIT
f_{osc}	Oscillator frequency range (OSCIN/OSCOUT)	12	30	MHz

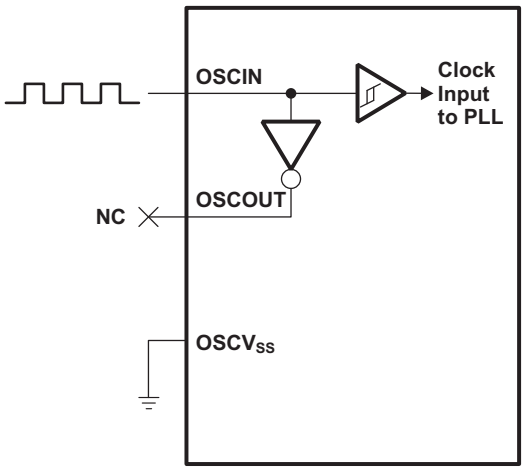

Figure 6-7. External 1.2V Clock Source

Table 6-3. OSCIN Timing Requirements for an Externally Driven Clock

PARAMETER		MIN	MAX	UNIT
f_{CLKIN}	OSCIN frequency range	12	50	MHz
$t_{c(CLKIN)}$	Cycle time, external clock driven on OSCIN	20		ns
$t_{w(CLKINH)}$	Pulse width high, external clock on OSCIN	0.4 $t_{c(CLKIN)}$		ns
$t_{w(CLKINL)}$	Pulse width low, external clock on OSCIN	0.4 $t_{c(CLKIN)}$		ns
$t_{t(CLKIN)}$	Transition time, OSCIN		5	ns

6.6 Clock PLLs

The device has two PLL controllers that provide clocks to different parts of the system. PLL0 provides clocks (though various dividers) to most of the components of the device. PLL1 provides clocks to the mDDR/DDR2 Controller and provides an alternate clock source for the ASYNC3 clock domain. This allows the peripherals on the ASYNC3 clock domain to be immune to frequency scaling operation on PLL0.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK [1:n]
- Auxiliary Clock from reference clock source: AUXCLK

Various dividers that can be used are as follows:

- Post-PLL Divider: POSTDIV
- SYSCLK Divider: D1, , Dn

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software programmable PLL Bypass: PLLEN

6.6.1 PLL Device-Specific Information

The device DSP generates the high-frequency internal clocks it requires through an on-chip PLL.

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The PLL requires some external filtering components to reduce power supply noise as shown in Figure 6-8.

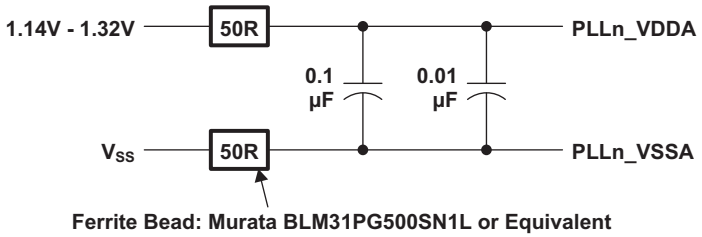

Figure 6-8. PLL External Filtering Components

The input to the PLL is either from the on-chip oscillator or from an external clock on the OSCIN pin. PLL0 outputs seven clocks that have programmable divider options. PLL1 outputs three clocks that have programmable divider options. Figure 6-9 illustrates the high-level view of the PLL Topology.

The PLLs are disabled by default after a device reset. They must be configured by software according to the allowable operating conditions listed in Table 6-4 before enabling the device to run from the PLL by setting PLLEN = 1.

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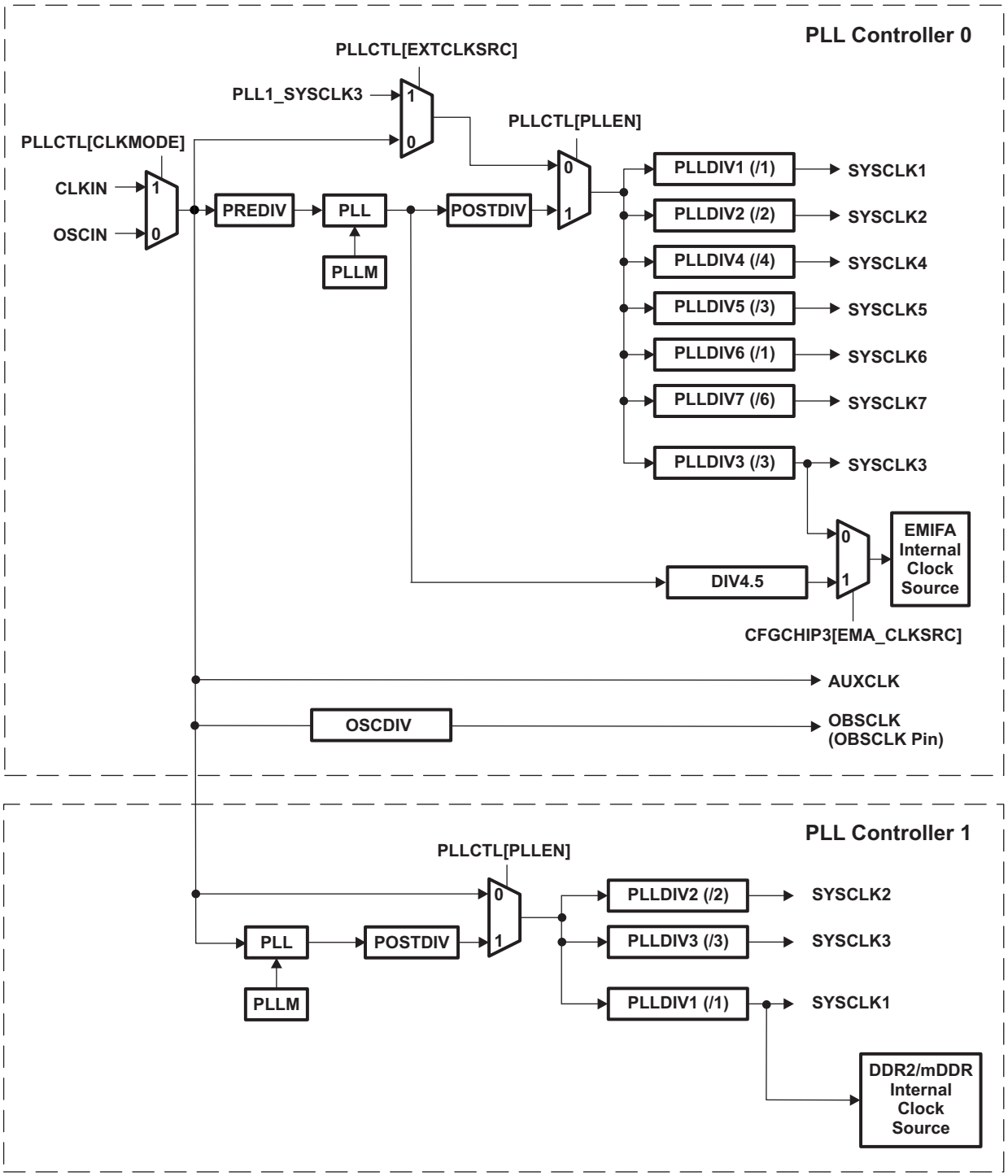

Figure 6-9. PLL Topology

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Table 6-4. Allowed PLL Operating Conditions (PLL0 and PLL1)

NO.	PARAMETER	Default Value	MIN	MAX	UNIT
1	**PLLRST**: Assertion time during initialization	N/A	125	N/A	ns
2	**Lock time**: The time that the application has to wait for the PLL to acquire lock before setting PLLEN, after changing PREDIV, PLLM, or OSCIN	N/A	N/A	Max PLL Lock Time = $\frac{2000\ N}{\sqrt{m}}$ where N = Pre-Divider Ratio M = PLL Multiplier	OSCIN cycles
3	**PREDIV**: Pre-divider value	/1	/1	/32	ns
4	**PLLREF**: PLL input frequency		12	50	MHz
5	**PLLM**: PLL multiplier values	x20	x4	x32	
6	**PLLOUT**: PLL output frequency	N/A	400	600(1)	MHz
7	**POSTDIV**: Post-divider value	/1	/2(1)	/32	ns

(1) PLL post divider / 2 must be used. The /4.5 clock path can be used to generate an EMIF clock from the undivided (i.e. 600 MHz) PLL output clock.

6.6.2 Device Clock Generation

PLL0 is controlled by PLL Controller 0 and PLL1 is controlled by PLL Controller 1. PLLC0 and PLLC1 manage the clock ratios, alignment, and gating for the system clocks to the chip. The PLLCs are responsible for controlling all modes of the PLL through software, in terms of pre-division of the clock inputs (PLLC0 only), multiply factors within the PLLs, and post-division for each of the chip-level clocks from the PLLs outputs. PLLC0 also controls reset propagation through the chip, clock alignment, and test points.

PLLC0 provides clocks for the majority of the system but PLLC1 provides clocks to the mDDR/DDR2 Controller and the ASYNC3 clock domain to provide frequency scaling immunity to a defined set or peripherals. The ASYNC3 clock domain can either derive its clock from PLL1_SYSCLK2 (for frequency scaling immunity from PLL0) or from PLL0_SYSCLK2 (for synchronous timing with PLL0) depending on the application requirements. In addition, some peripherals have specific clock options independent of the ASYNC clock domain.

6.7 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems.

6.7.1 DSP Interrupts

The C674x DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user programmable and is listed in Table 6-5. Also, the interrupt controller controls the generation of the CPU exceptions, NMI, and emulation interrupts. Table 6-6 summarizes the C674x interrupt controller registers and memory locations.

Table 6-5. C6748 DSP Interrupts

EVT#	Interrupt Name	Source
0	EVT0	C674x Int Ctl 0
1	EVT1	C674x Int Ctl 1
2	EVT2	C674x Int Ctl 2
3	EVT3	C674x Int Ctl 3
4	T64P0_TINT12	Timer64P0 - TINT12
5	SYSCFG_CHIPINT2	SYSCFG CHIPSIG Register
6	-	Reserved
7	EHRPWM0	HiResTimer/PWM0 Interrupt
8	EDMA3_0_CC0_INT1	EDMA3_0 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt
9	EMU_DTDMA	C674x-ECM
10	EHRPWM0TZ	HiResTimer/PWM0 Trip Zone Interrupt
11	EMU_RTDXRX	C674x-RTDX
12	EMU_RTDXTX	C674x-RTDX
13	IDMAINT0	C674x-EMC
14	IDMAINT1	C674x-EMC
15	MMCSD0_INT0	MMCSD0 MMC/SD Interrupt
16	MMCSD0_INT1	MMCSD0 SDIO Interrupt
17	-	Reserved
18	EHRPWM1	HiResTimer/PWM1 Interrupt
19	USB0_INT	USB0 Interrupt
20	USB1_HCINT	USB1 OHCI Host Controller Interrupt
21	USB1_RWAKEUP	USB1 Remote Wakeup Interrupt
22	-	Reserved
23	EHRPWM1TZ	HiResTimer/PWM1 Trip Zone Interrupt
24	SATA_INT	SATA Controller
25	T64P2_TINTALL	Timer64P2 Combined TINT12 and TINT 34 Interrupt
26	EMAC_C0RXTHRESH	EMAC - Core 0 Receive Threshold Interrupt
27	EMAC_C0RX	EMAC - Core 0 Receive Interrupt
28	EMAC_C0TX	EMAC - Core 0 Transmit Interrupt
29	EMAC_C0MISC	EMAC - Core 0 Miscellaneous Interrupt
30	EMAC_C1RXTHRESH	EMAC - Core 1 Receive Threshold Interrupt
31	EMAC_C1RX	EMAC - Core 1 Receive Interrupt
32	EMAC_C1TX	EMAC - Core 1 Transmit Interrupt
33	EMAC_C1MISC	EMAC - Core 1 Miscellaneous Interrupt
34	UHPI_DSPINT	UHPI DSP Interrupt
35	-	Reserved
36	IIC0_INT	I2C0
37	SP0_INT	SPI0
38	UART0_INT	UART0
39	-	Reserved
40	T64P1_TINT12	Timer64P1 Interrupt 12
41	GPIO_B1INT	GPIO Bank 1 Interrupt
42	IIC1_INT	I2C1
43	SPI1_INT	SPI1
44	-	Reserved
45	ECAP0	ECAP0

Table 6-5. C6748 DSP Interrupts (continued)

EVT#	Interrupt Name	Source
46	UART_INT1	UART1
47	ECAP1	ECAP1
48	T64P1_TINT34	Timer64P1 Interrupt 34
49	GPIO_B2INT	GPIO Bank 2 Interrupt
50	-	Reserved
51	ECAP2	ECAP2
52	GPIO_B3INT	GPIO Bank 3 Interrupt
53	MMCSD1_INT1	MMCSD1 SDIO Interrupt
54	GPIO_B4INT	GPIO Bank 4 Interrupt
55	EMIFA_INT	EMIFA
56	EDMA3_0_CC0_ERRINT	EDMA3_0 Channel Controller 0 Error Interrupt
57	EDMA3_0_TC0_ERRINT	EDMA3_0 Transfer Controller 0 Error Interrupt
58	EDMA3_0_TC1_ERRINT	EDMA3_0 Transfer Controller 1 Error Interrupt
59	GPIO_B5INT	GPIO Bank 5 Interrupt
60	DDR2_MEMERR	DDR2 Memory Error Interrupt
61	MCASP0_INT	McASP0 Combined RX/TX Interrupts
62	GPIO_B6INT	GPIO Bank 6 Interrupt
63	RTC_IRQS	RTC Combined
64	T64P0_TINT34	Timer64P0 Interrupt 34
65	GPIO_B0INT	GPIO Bank 0 Interrupt
66	-	Reserved
67	SYSCFG_CHIPINT3	SYSCFG_CHIPSIG Register
68	MMCSD1_INT0	MMCSD1 MMC/SD Interrupt
69	UART2_INT	UART2
70	PSC0_ALLINT	PSC0
71	PSC1_ALLINT	PSC1
72	GPIO_B7INT	GPIO Bank 7 Interrupt
73	LCDC_INT	LDC Controller
74	PROTERR	SYSCFG Protection Shared Interrupt
75	GPIO_B8INT	GPIO Bank 8 Interrupt
76	-	Reserved
77	-	Reserved
78	T64P2_CMPINT0	Timer64P2 - Compare Interrupt 0
79	T64P2_CMPINT1	Timer64P2 - Compare Interrupt 1
80	T64P2_CMPINT2	Timer64P2 - Compare Interrupt 2
81	T64P2_CMPINT3	Timer64P2 - Compare Interrupt 3
82	T64P2_CMPINT4	Timer64P2 - Compare Interrupt 4
83	T64P2_CMPINT5	Timer64P2 - Compare Interrupt 5
84	T64P2_CMPINT6	Timer64P2 - Compare Interrupt 6
85	T64P2_CMPINT7	Timer64P2 - Compare Interrupt 7
86	T64P3_TINTALL	Timer64P3 Combined TINT12 and TINT 34 Interrupt
87	MCBSP0_RINT	McBSP0 Receive Interrupt
88	MCBSP0_XINT	McBSP0 Transmit Interrupt
89	MCBSP1_RINT	McBSP1 Receive Interrupt
90	MCBSP1_XINT	McBSP1 Transmit Interrupt
91	EDMA3_1_CC0_INT1	EDMA3_1 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt

Table 6-5. C6748 DSP Interrupts (continued)

EVT#	Interrupt Name	Source
92	EDMA3_1_CC0_ERRINT	EDMA3_1 Channel Controller 0 Error Interrupt
93	EDMA3_1_TC0_ERRINT	EDMA3_1 Transfer Controller 0 Error Interrupt
94	UPP_INT	uPP Combined Interrupt
95	VPIF_INT	VPIF Combined Interrupt
96	INTERR	C674x-Int Ctl
97	EMC_IDMAERR	C674x-EMC
98	-	Reserved
99	-	Reserved
100	-	Reserved
101	-	Reserved
102	-	Reserved
103	-	Reserved
104	-	Reserved
105	-	Reserved
106	-	Reserved
107	-	Reserved
108	-	Reserved
109	-	Reserved
110	-	Reserved
111	-	Reserved
112	-	Reserved
113	PMC_ED	C674x-PMC
114	-	Reserved
115	-	Reserved
116	UMC_ED1	C674x-UMC
117	UMC_ED2	C674x-UMC
118	PDC_INT	C674x-PDC
119	SYS_CMPA	C674x-SYS
120	PMC_CMPA	C674x-PMC
121	PMC_CMPA	C674x-PMC
122	DMC_CMPA	C674x-DMC
123	DMC_CMPA	C674x-DMC
124	UMC_CMPA	C674x-UMC
125	UMC_CMPA	C674x-UMC
126	EMC_CMPA	C674x-EMC
127	EMC_BUSERR	C674x-EMC

Table 6-6. C674x DSP Interrupt Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x0180 0000	EVTFLAG0	Event flag register 0
0x0180 0004	EVTFLAG1	Event flag register 1
0x0180 0008	EVTFLAG2	Event flag register 2
0x0180 000C	EVTFLAG3	Event flag register 3
0x0180 0020	EVTSET0	Event set register 0
0x0180 0024	EVTSET1	Event set register 1
0x0180 0028	EVTSET2	Event set register 2
0x0180 002C	EVTSET3	Event set register 3
0x0180 0040	EVTCLR0	Event clear register 0
0x0180 0044	EVTCLR1	Event clear register 1
0x0180 0048	EVTCLR2	Event clear register 2
0x0180 004C	EVTCLR3	Event clear register 3
0x0180 0080	EVTMASK0	Event mask register 0
0x0180 0084	EVTMASK1	Event mask register 1
0x0180 0088	EVTMASK2	Event mask register 2
0x0180 008C	EVTMASK3	Event mask register 3
0x0180 00A0	MEVTFLAG0	Masked event flag register 0
0x0180 00A4	MEVTFLAG1	Masked event flag register 1
0x0180 00A8	MEVTFLAG2	Masked event flag register 2
0x0180 00AC	MEVTFLAG3	Masked event flag register 3
0x0180 00C0	EXPMASK0	Exception mask register 0
0x0180 00C4	EXPMASK1	Exception mask register 1
0x0180 00C8	EXPMASK2	Exception mask register 2
0x0180 00CC	EXPMASK3	Exception mask register 3
0x0180 00E0	MEXPFLAG0	Masked exception flag register 0
0x0180 00E4	MEXPFLAG1	Masked exception flag register 1
0x0180 00E8	MEXPFLAG2	Masked exception flag register 2
0x0180 00EC	MEXPFLAG3	Masked exception flag register 3
0x0180 0104	INTMUX1	Interrupt mux register 1
0x0180 0108	INTMUX2	Interrupt mux register 2
0x0180 010C	INTMUX3	Interrupt mux register 3
0x0180 0140 - 0x0180 0144	-	Reserved
0x0180 0180	INTXSTAT	Interrupt exception status
0x0180 0184	INTXCLR	Interrupt exception clear
0x0180 0188	INTDMASK	Dropped interrupt mask register
0x0180 01C0	EVTASRT	Event assert register

6.8 Power and Sleep Controller (PSC)

The Power and Sleep Controllers (PSC) are responsible for managing transitions of system power on/off, clock on/off, resets (device level and module level). It is used primarily to provide granular power control for on chip modules (peripherals and CPU). A PSC module consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, PSC interrupts, a state machine for each peripheral/module it controls. An LPSC is associated with every module that is controlled by the PSC and provides clock and reset control.

The PSC includes the following features:

- Provides a software interface to:
  - Control module clock enable/disable
  - Control module reset
  - Control CPU local reset
- Supports IcePick emulation features: power, clock and reset

  PSC0 controls 16 local PSCs.

  PSC1 controls 32 local PSCs.

Table 6-7. Power and Sleep Controller (PSC) Registers

PSC0 BYTE ADDRESS	PSC1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C1 0000	0x01E2 7000	REVID	Peripheral Revision and Class Information Register
0x01C1 0018	0x01E2 7018	INTEVAL	Interrupt Evaluation Register
0x01C1 0040	0x01E2 7040	MERRPR0	Module Error Pending Register 0 (module 0-15) (PSC0) Module Error Pending Register 0 (module 0-31) (PSC1)
0x01C1 0050	0x01E2 7050	MERRCR0	Module Error Clear Register 0 (module 0-15) (PSC0) Module Error Clear Register 0 (module 0-31) (PSC1)
0x01C1 0060	0x01E2 7060	PERRPR	Power Error Pending Register
0x01C1 0068	0x01E2 7068	PERRCR	Power Error Clear Register
0x01C1 0120	0x01E2 7120	PTCMD	Power Domain Transition Command Register
0x01C1 0128	0x01E2 7128	PTSTAT	Power Domain Transition Status Register
0x01C1 0200	0x01E2 7200	PDSTAT0	Power Domain 0 Status Register
0x01C1 0204	0x01E2 7204	PDSTAT1	Power Domain 1 Status Register
0x01C1 0300	0x01E2 7300	PDCTL0	Power Domain 0 Control Register
0x01C1 0304	0x01E2 7304	PDCTL1	Power Domain 1 Control Register
0x01C1 0400	0x01E2 7400	PDCFG0	Power Domain 0 Configuration Register
0x01C1 0404	0x01E2 7404	PDCFG1	Power Domain 1 Configuration Register
0x01C1 0800	0x01E2 7800	MDSTAT0	Module 0 Status Register
0x01C1 0804	0x01E2 7804	MDSTAT1	Module 1 Status Register
0x01C1 0808	0x01E2 7808	MDSTAT2	Module 2 Status Register
0x01C1 080C	0x01E2 780C	MDSTAT3	Module 3 Status Register
0x01C1 0810	0x01E2 7810	MDSTAT4	Module 4 Status Register
0x01C1 0814	0x01E2 7814	MDSTAT5	Module 5 Status Register
0x01C1 0818	0x01E2 7818	MDSTAT6	Module 6 Status Register
0x01C1 081C	0x01E2 781C	MDSTAT7	Module 7 Status Register
0x01C1 0820	0x01E2 7820	MDSTAT8	Module 8 Status Register
0x01C1 0824	0x01E2 7824	MDSTAT9	Module 9 Status Register
0x01C1 0828	0x01E2 7828	MDSTAT10	Module 10 Status Register
0x01C1 082C	0x01E2 782C	MDSTAT11	Module 11 Status Register
0x01C1 0830	0x01E2 7830	MDSTAT12	Module 12 Status Register
0x01C1 0834	0x01E2 7834	MDSTAT13	Module 13 Status Register

Table 6-7. Power and Sleep Controller (PSC) Registers (continued)

PSC0 BYTE ADDRESS	PSC1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C1 0838	0x01E2 7838	MDSTAT14	Module 14 Status Register
0x01C1 083C	0x01E2 783C	MDSTAT15	Module 15 Status Register
-	0x01E2 7840	MDSTAT16	Module 16 Status Register
-	0x01E2 7844	MDSTAT17	Module 17 Status Register
-	0x01E2 7848	MDSTAT18	Module 18 Status Register
-	0x01E2 784C	MDSTAT19	Module 19 Status Register
-	0x01E2 7850	MDSTAT20	Module 20 Status Register
-	0x01E2 7854	MDSTAT21	Module 21 Status Register
-	0x01E2 7858	MDSTAT22	Module 22 Status Register
-	0x01E2 785C	MDSTAT23	Module 23 Status Register
-	0x01E2 7860	MDSTAT24	Module 24 Status Register
-	0x01E2 7864	MDSTAT25	Module 25 Status Register
-	0x01E2 7868	MDSTAT26	Module 26 Status Register
-	0x01E2 786C	MDSTAT27	Module 27 Status Register
-	0x01E2 7870	MDSTAT28	Module 28 Status Register
-	0x01E2 7874	MDSTAT29	Module 29 Status Register
-	0x01E2 7878	MDSTAT30	Module 30 Status Register
-	0x01E2 787C	MDSTAT31	Module 31 Status Register
0x01C1 0A00	0x01E2 7A00	MDCTL0	Module 0 Control Register
0x01C1 0A04	0x01E2 7A04	MDCTL1	Module 1 Control Register
0x01C1 0A08	0x01E2 7A08	MDCTL2	Module 2 Control Register
0x01C1 0A0C	0x01E2 7A0C	MDCTL3	Module 3 Control Register
0x01C1 0A10	0x01E2 7A10	MDCTL4	Module 4 Control Register
0x01C1 0A14	0x01E2 7A14	MDCTL5	Module 5 Control Register
0x01C1 0A18	0x01E2 7A18	MDCTL6	Module 6 Control Register
0x01C1 0A1C	0x01E2 7A1C	MDCTL7	Module 7 Control Register
0x01C1 0A20	0x01E2 7A20	MDCTL8	Module 8 Control Register
0x01C1 0A24	0x01E2 7A24	MDCTL9	Module 9 Control Register
0x01C1 0A28	0x01E2 7A28	MDCTL10	Module 10 Control Register
0x01C1 0A2C	0x01E2 7A2C	MDCTL11	Module 11 Control Register
0x01C1 0A30	0x01E2 7A30	MDCTL12	Module 12 Control Register
0x01C1 0A34	0x01E2 7A34	MDCTL13	Module 13 Control Register
0x01C1 0A38	0x01E2 7A38	MDCTL14	Module 14 Control Register
0x01C1 0A3C	0x01E2 7A3C	MDCTL15	Module 15 Control Register
-	0x01E2 7A40	MDCTL16	Module 16 Control Register
-	0x01E2 7A44	MDCTL17	Module 17 Control Register
-	0x01E2 7A48	MDCTL18	Module 18 Control Register
-	0x01E2 7A4C	MDCTL19	Module 19 Control Register
-	0x01E2 7A50	MDCTL20	Module 20 Control Register
-	0x01E2 7A54	MDCTL21	Module 21 Control Register
-	0x01E2 7A58	MDCTL22	Module 22 Control Register
-	0x01E2 7A5C	MDCTL23	Module 23 Control Register
-	0x01E2 7A60	MDCTL24	Module 24 Control Register
-	0x01E2 7A64	MDCTL25	Module 25 Control Register
-	0x01E2 7A68	MDCTL26	Module 26 Control Register
-	0x01E2 7A6C	MDCTL27	Module 27 Control Register

Table 6-7. Power and Sleep Controller (PSC) Registers (continued)

PSC0 BYTE ADDRESS	PSC1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
-	0x01E2 7A70	MDCTL28	Module 28 Control Register
-	0x01E2 7A74	MDCTL29	Module 29 Control Register
-	0x01E2 7A78	MDCTL30	Module 30 Control Register
-	0x01E2 7A7C	MDCTL31	Module 31 Control Register

6.8.1 Power Domain and Module Topology

The device includes two PSC modules.

Each PSC module controls clock states for several of the on chip modules, controllers and interconnect components. Table 6-8 and Table 6-9 lists the set of peripherals/modules that are controlled by the PSC, the power domain they are associated with, the LPSC assignment and the default (power-on reset) module states. See the device-specific data manual for the peripherals available on a given device. The module states and terminology are defined in Section 6.8.1.2.

Table 6-8. PSC0 Default Module Configuration

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/Wake Only
0	EDMA3 Channel Controller 0	AlwaysON (PD0)	SwRstDisable	—
1	EDMA3 Transfer Controller 0	AlwaysON (PD0)	SwRstDisable	—
2	EDMA3 Transfer Controller 1	AlwaysON (PD0)	SwRstDisable	—
3	EMIFA (Br7)	AlwaysON (PD0)	SwRstDisable	—
4	SPI 0	AlwaysON (PD0)	SwRstDisable	—
5	MMC/SD 0	AlwaysON (PD0)	SwRstDisable	—
6	—	—	—	—
7	—	—	—	—
8	—	—	—	—
9	UART 0	AlwaysON (PD0)	SwRstDisable	—
10	SCR0 (Br 0, Br 1, Br 2, Br 8)	AlwaysON (PD0)	Enable	Yes
11	SCR1 (Br 4)	AlwaysON (PD0)	Enable	Yes
12	SCR2 (Br 3, Br 5, Br 6)	AlwaysON (PD0)	Enable	Yes
13	—	—	—	—
14	—	—	—	—
15	DSP	PD_DSP (PD1)	Enable	—

Table 6-9. PSC1 Default Module Configuration

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/Wake Only
0	EDMA3 Channel Controller 1	AlwaysON (PD0)	SwRstDisable	—
1	USB0 (USB2.0)	AlwaysON (PD0)	SwRstDisable	—
2	USB1 (USB1.1)	AlwaysON (PD0)	SwRstDisable	—
3	GPIO	AlwaysON (PD0)	SwRstDisable	—
4	UHPI	AlwaysON (PD0)	SwRstDisable	—
5	EMAC	AlwaysON (PD0)	SwRstDisable	—
6	DDR2 (and SCR_F3)	AlwaysON (PD0)	SwRstDisable	—
7	McASP0 (+ McASP0 FIFO)	AlwaysON (PD0)	SwRstDisable	—
8	SATA	AlwaysON (PD0)	SwRstDisable	—
9	VPIF	AlwaysON (PD0)	SwRstDisable	—
10	SPI 1	AlwaysON (PD0)	SwRstDisable	—
11	I2C 1	AlwaysON (PD0)	SwRstDisable	—
12	UART 1	AlwaysON (PD0)	SwRstDisable	—
13	UART 2	AlwaysON (PD0)	SwRstDisable	—
14	McBSP0 (+ McBSP0 FIFO)	AlwaysON (PD0)	SwRstDisable	—
15	McBSP1 (+ McBSP1 FIFO)	AlwaysON (PD0)	SwRstDisable	—
16	LCDC	AlwaysON (PD0)	SwRstDisable	—
17	eHRPWM0/1	AlwaysON (PD0)	SwRstDisable	—
18	MMCSD1	AlwaysON (PD0)	SwRstDisable	—
19	uPP	AlwaysON (PD0)	SwRstDisable	—
20	ECAP0/1/2	AlwaysON (PD0)	SwRstDisable	—
21	EDMA3 Transfer Controller 2	AlwaysON (PD0)	SwRstDisable	—
22	—	—	—	—
23	—	—	—	—
24	SCR_F0 (and bridge F0)	AlwaysON (PD0)	Enable	Yes
25	SCR_F1 (and bridge F1)	AlwaysON (PD0)	Enable	Yes
26	SCR_F2 (and bridge F2)	AlwaysON (PD0)	Enable	Yes
27	SCR_F6 (and bridge F3)	AlwaysON (PD0)	Enable	Yes
28	SCR_F7 (and bridge F4)	AlwaysON (PD0)	Enable	Yes
29	SCR_F8 (and bridge F5)	AlwaysON (PD0)	Enable	Yes
30	Bridge F7 (DDR Controller path)	AlwaysON (PD0)	Enable	Yes
31	Shared RAM (including SCR_F4 and bridge F6)	PD_SHRAM	Enable	—

6.8.1.1 Power Domain States

A power domain can only be in one of the two states: ON or OFF, defined as follows:

- ON: power to the domain is on
- OFF: power to the domain is off

For both PSC0 and PSC1, the Always ON domain, or PD0 power domain, is always in the ON state when the chip is powered-on. This domain is not programmable to OFF state.

- On PSC0 PD1/PD_DSP Domain: Controls the sleep state for DSP L1 and L2 Memories
- On PSC1 PD1/PD_SHRAM Domain: Controls the sleep state for the 128K Shared RAM

6.8.1.2 Module States

The PSC defines several possible states for a module. This states are essentially a combination of the module reset asserted or de-asserted and module clock on/enabled or off/disabled. The module states are defined in Table 6-10.

Table 6-10. Module States

Module State	Module Reset	Module Clock	Module State Definition
Enable	De-asserted	On	A module in the enable state has its module reset de-asserted and it has its clock on. This is the normal operational state for a given module
Disable	De-asserted	Off	A module in the disabled state has its module reset de-asserted and it has its module clock off. This state is typically used for disabling a module clock to save power. The device is designed in full static CMOS, so when you stop a module clock, it retains the module's state. When the clock is restarted, the module resumes operating from the stopping point.
SyncReset	Asserted	On	A module state in the SyncReset state has its module reset asserted and it has its clock on. Generally, software is not expected to initiate this state
SwRstDisable	Asserted	Off	A module in the SwResetDisable state has its module reset asserted and it has its clock disabled. After initial power-on, several modules come up in the SwRstDisable state. Generally, software is not expected to initiate this state
Auto Sleep	De-asserted	Off	A module in the Auto Sleep state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it can "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and after servicing the request it will "automatically" transition into the sleep state (with module reset re de-asserted and module clock disabled), without any software intervention. The transition from sleep to enabled and back to sleep state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data.
Auto Wake	De-asserted	Off	A module in the Auto Wake state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it will "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and will remain in the "Enabled" state from then on (with module reset re de-asserted and module clock on), without any software intervention. The transition from sleep to enabled state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data.

6.9 EDMA

The EDMA controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

6.9.1 EDMA3 Channel Synchronization Events

Each EDMA channel controller supports up to 32 channels which service peripherals and memory. Table 6-11lists the source of the EDMA synchronization events associated with each of the programmable EDMA channels.

Table 6-11. EDMA Synchronization Events

EDMA0 Channel Controller 0			
Event	**Event Name / Source**	**Event**	**Event Name / Source**
0	McASP0 Receive	16	MMCSD0 Receive
1	McASP0 Transmit	17	MMCSD0 Transmit
2	McBSP0 Receive	18	SPI1 Receive
3	McBSP0 Transmit	19	SPI1 Transmit
4	McBSP1 Receive	20	Reserved
5	McBSP1 Transmit	21	Reserved
6	GPIO Bank 0 Interrupt	22	GPIO Bank 2 Interrupt
7	GPIO Bank 1 Interrupt	23	GPIO Bank 3 Interrupt
8	UART0 Receive	24	I2C0 Receive
9	UART0 Transmit	25	I2C0 Transmit
10	Timer64P0 Event Out 12	26	I2C1 Receive
11	Timer64P0 Event Out 34	27	I2C1 Transmit
12	UART1 Receive	28	GPIO Bank 4 Interrupt
13	UART1 Transmit	29	GPIO Bank 5 Interrupt
14	SPI0 Receive	30	UART2 Receive
15	SPI0 Transmit	31	UART2 Transmit
EDMA1 Channel Controller 1			
Event	Event Name / Source	Event	Event Name / Source
0	Timer64P2 Compare Event 0	16	GPIO Bank 6 Interrupt
1	Timer64P2 Compare Event 1	17	GPIO Bank 7 Interrupt
2	Timer64P2 Compare Event 2	18	GPIO Bank 8 Interrupt
3	Timer64P2 Compare Event 3	19	Reserved
4	Timer64P2 Compare Event 4	20	Reserved
5	Timer64P2 Compare Event 5	21	Reserved
6	Timer64P2 Compare Event 6	22	Reserved
7	Timer64P2 Compare Event 7	23	Reserved
8	Timer64P3 Compare Event 0	24	Timer64P2 Event Out 12
9	Timer64P3 Compare Event 1	25	Timer64P2 Event Out 34
10	Timer64P3 Compare Event 2	26	Timer64P3 Event Out 12
11	Timer64P3 Compare Event 3	27	Timer64P3 Event Out 34
12	Timer64P3 Compare Event 4	28	MMCSD0 Receive
13	Timer64P3 Compare Event 5	29	MMCSD0 Transmit
14	Timer64P3 Compare Event 6	30	Reserved
15	Timer64P3 Compare Event 7	31	Reserved

6.9.2 EDMA Peripheral Register Descriptions

Table 6-12 is the list of EDMA3 Channel Controller Registers and Table 6-13 is the list of EDMA3 Transfer Controller registers.

Table 6-12. EDMA3 Channel Controller (EDMA3CC) Registers

EDMA0 Channel Controller 0 BYTE ADDRESS	EDMA1 Channel Controller 0 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C0 0000	0x01E3 0000	PID	Peripheral Identification Register
0x01C0 0004	0x01E3 0004	CCCFG	EDMA3CC Configuration Register
Global Registers			
0x01C0 0200	0x01E3 0200	QCHMAP0	QDMA Channel 0 Mapping Register
0x01C0 0204	0x01E3 0204	QCHMAP1	QDMA Channel 1 Mapping Register
0x01C0 0208	0x01E3 0208	QCHMAP2	QDMA Channel 2 Mapping Register
0x01C0 020C	0x01E3 020C	QCHMAP3	QDMA Channel 3 Mapping Register
0x01C0 0210	0x01E3 0210	QCHMAP4	QDMA Channel 4 Mapping Register
0x01C0 0214	0x01E3 0214	QCHMAP5	QDMA Channel 5 Mapping Register
0x01C0 0218	0x01E3 0218	QCHMAP6	QDMA Channel 6 Mapping Register
0x01C0 021C	0x01E3 021C	QCHMAP7	QDMA Channel 7 Mapping Register
0x01C0 0240	0x01E3 0240	DMAQNUM0	DMA Channel Queue Number Register 0
0x01C0 0244	0x01E3 0244	DMAQNUM1	DMA Channel Queue Number Register 1
0x01C0 0248	0x01E3 0248	DMAQNUM2	DMA Channel Queue Number Register 2
0x01C0 024C	0x01E3 024C	DMAQNUM3	DMA Channel Queue Number Register 3
0x01C0 0260	0x01E3 0260	QDMAQNUM	QDMA Channel Queue Number Register
0x01C0 0284	0x01E3 0284	QUEPRI	Queue Priority Register(1)
0x01C0 0300	0x01E3 0300	EMR	Event Missed Register
0x01C0 0308	0x01E3 0308	EMCR	Event Missed Clear Register
0x01C0 0310	0x01E3 0310	QEMR	QDMA Event Missed Register
0x01C0 0314	0x01E3 0314	QEMCR	QDMA Event Missed Clear Register
0x01C0 0318	0x01E3 0318	CCERR	EDMA3CC Error Register
0x01C0 031C	0x01E3 031C	CCERRCLR	EDMA3CC Error Clear Register
0x01C0 0320	0x01E3 0320	EEVAL	Error Evaluate Register
0x01C0 0340	0x01E3 0340	DRAE0	DMA Region Access Enable Register for Region 0
0x01C0 0348	0x01E3 0348	DRAE1	DMA Region Access Enable Register for Region 1
0x01C0 0350	0x01E3 0350	DRAE2	DMA Region Access Enable Register for Region 2
0x01C0 0358	0x01E3 0358	DRAE3	DMA Region Access Enable Register for Region 3
0x01C0 0380	0x01E3 0380	QRAE0	QDMA Region Access Enable Register for Region 0
0x01C0 0384	0x01E3 0384	QRAE1	QDMA Region Access Enable Register for Region 1
0x01C0 0388	0x01E3 0388	QRAE2	QDMA Region Access Enable Register for Region 2
0x01C0 038C	0x01E3 038C	QRAE3	QDMA Region Access Enable Register for Region 3
0x01C0 0400 - 0x01C0 043C	0x01E3 0400 - 0x01E3 043C	Q0E0-Q0E15	Event Queue Entry Registers Q0E0-Q0E15
0x01C0 0440 - 0x01C0 047C	0x01E3 0440 - 0x01E3 047C	Q1E0-Q1E15	Event Queue Entry Registers Q1E0-Q1E15
0x01C0 0600	0x01E3 0600	QSTAT0	Queue 0 Status Register
0x01C0 0604	0x01E3 0604	QSTAT1	Queue 1 Status Register
0x01C0 0620	0x01E3 0620	QWMTHRA	Queue Watermark Threshold A Register
0x01C0 0640	0x01E3 0640	CCSTAT	EDMA3CC Status Register
Global Channel Registers			

(1) On previous architectures, the EDMA3TC priority was controlled by the queue priority register (QUEPRI) in the EDMA3CC memory-map. However for this device, the priority control for the transfer controllers is controlled by the chip-level registers in the System Configuration Module. You should use the chip-level registers and not QUEPRI to configure the TC priority.

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Table 6-12. EDMA3 Channel Controller (EDMA3CC) Registers (continued)

EDMA0 Channel Controller 0 BYTE ADDRESS	EDMA1 Channel Controller 0 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C0 1000	0x01E3 1000	ER	Event Register
0x01C0 1008	0x01E3 1008	ECR	Event Clear Register
0x01C0 1010	0x01E3 1010	ESR	Event Set Register
0x01C0 1018	0x01E3 1018	CER	Chained Event Register
0x01C0 1020	0x01E3 1020	EER	Event Enable Register
0x01C0 1028	0x01E3 1028	EECR	Event Enable Clear Register
0x01C0 1030	0x01E3 1030	EESR	Event Enable Set Register
0x01C0 1038	0x01E3 1038	SER	Secondary Event Register
0x01C0 1040	0x01E3 1040	SECR	Secondary Event Clear Register
0x01C0 1050	0x01E3 1050	IER	Interrupt Enable Register
0x01C0 1058	0x01E3 1058	IECR	Interrupt Enable Clear Register
0x01C0 1060	0x01E3 1060	IESR	Interrupt Enable Set Register
0x01C0 1068	0x01E3 1068	IPR	Interrupt Pending Register
0x01C0 1070	0x01E3 1070	ICR	Interrupt Clear Register
0x01C0 1078	0x01E3 1078	IEVAL	Interrupt Evaluate Register
0x01C0 1080	0x01E3 1080	QER	QDMA Event Register
0x01C0 1084	0x01E3 1084	QEER	QDMA Event Enable Register
0x01C0 1088	0x01E3 1088	QEECR	QDMA Event Enable Clear Register
0x01C0 108C	0x01E3 108C	QEESR	QDMA Event Enable Set Register
0x01C0 1090	0x01E3 1090	QSER	QDMA Secondary Event Register
0x01C0 1094	0x01E3 1094	QSECR	QDMA Secondary Event Clear Register
Shadow Region 0 Channel Registers			
0x01C0 2000	0x01E3 2000	ER	Event Register
0x01C0 2008	0x01E3 2008	ECR	Event Clear Register
0x01C0 2010	0x01E3 2010	ESR	Event Set Register
0x01C0 2018	0x01E3 2018	CER	Chained Event Register
0x01C0 2020	0x01E3 2020	EER	Event Enable Register
0x01C0 2028	0x01E3 2028	EECR	Event Enable Clear Register
0x01C0 2030	0x01E3 2030	EESR	Event Enable Set Register
0x01C0 2038	0x01E3 2038	SER	Secondary Event Register
0x01C0 2040	0x01E3 2040	SECR	Secondary Event Clear Register
0x01C0 2050	0x01E3 2050	IER	Interrupt Enable Register
0x01C0 2058	0x01E3 2058	IECR	Interrupt Enable Clear Register
0x01C0 2060	0x01E3 2060	IESR	Interrupt Enable Set Register
0x01C0 2068	0x01E3 2068	IPR	Interrupt Pending Register
0x01C0 2070	0x01E3 2070	ICR	Interrupt Clear Register
0x01C0 2078	0x01E3 2078	IEVAL	Interrupt Evaluate Register
0x01C0 2080	0x01E3 2080	QER	QDMA Event Register
0x01C0 2084	0x01E3 2084	QEER	QDMA Event Enable Register
0x01C0 2088	0x01E3 2088	QEECR	QDMA Event Enable Clear Register
0x01C0 208C	0x01E3 208C	QEESR	QDMA Event Enable Set Register
0x01C0 2090	0x01E3 2090	QSER	QDMA Secondary Event Register
0x01C0 2094	0x01E3 2094	QSECR	QDMA Secondary Event Clear Register
Shadow Region 1 Channel Registers			
0x01C0 2200	0x01E3 2200	ER	Event Register
0x01C0 2208	0x01E3 2208	ECR	Event Clear Register

Table 6-12. EDMA3 Channel Controller (EDMA3CC) Registers (continued)

EDMA0 Channel Controller 0 BYTE ADDRESS	EDMA1 Channel Controller 0 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C0 2210	0x01E3 2210	ESR	Event Set Register
0x01C0 2218	0x01E3 2218	CER	Chained Event Register
0x01C0 2220	0x01E3 2220	EER	Event Enable Register
0x01C0 2228	0x01E3 2228	EECR	Event Enable Clear Register
0x01C0 2230	0x01E3 2230	EESR	Event Enable Set Register
0x01C0 2238	0x01E3 2238	SER	Secondary Event Register
0x01C0 2240	0x01E3 2240	SECR	Secondary Event Clear Register
0x01C0 2250	0x01E3 2250	IER	Interrupt Enable Register
0x01C0 2258	0x01E3 2258	IECR	Interrupt Enable Clear Register
0x01C0 2260	0x01E3 2260	IESR	Interrupt Enable Set Register
0x01C0 2268	0x01E3 2268	IPR	Interrupt Pending Register
0x01C0 2270	0x01E3 2270	ICR	Interrupt Clear Register
0x01C0 2278	0x01E3 2278	IEVAL	Interrupt Evaluate Register
0x01C0 2280	0x01E3 2280	QER	QDMA Event Register
0x01C0 2284	0x01E3 2284	QEER	QDMA Event Enable Register
0x01C0 2288	0x01E3 2288	QEECR	QDMA Event Enable Clear Register
0x01C0 228C	0x01E3 228C	QEESR	QDMA Event Enable Set Register
0x01C0 2290	0x01E3 2290	QSER	QDMA Secondary Event Register
0x01C0 2294	0x01E3 2294	QSECR	QDMA Secondary Event Clear Register
0x01C0 4000 - 0x01C0 4FFF	0x01E3 4000 - 0x01E3 4FFF	—	Parameter RAM (PaRAM)

Table 6-13. EDMA3 Transfer Controller (EDMA3TC) Registers

EDMA0 Transfer Controller 0 BYTE ADDRESS	EDMA0 Transfer Controller 1 BYTE ADDRESS	EDMA1 Transfer Controller 0 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C0 8000	0x01C0 8400	0x01E3 8000	PID	Peripheral Identification Register
0x01C0 8004	0x01C0 8404	0x01E3 8004	TCCFG	EDMA3TC Configuration Register
0x01C0 8100	0x01C0 8500	0x01E3 8100	TCSTAT	EDMA3TC Channel Status Register
0x01C0 8120	0x01C0 8520	0x01E3 8120	ERRSTAT	Error Status Register
0x01C0 8124	0x01C0 8524	0x01E3 8124	ERREN	Error Enable Register
0x01C0 8128	0x01C0 8528	0x01E3 8128	ERRCLR	Error Clear Register
0x01C0 812C	0x01C0 852C	0x01E3 812C	ERRDET	Error Details Register
0x01C0 8130	0x01C0 8530	0x01E3 8130	ERRCMD	Error Interrupt Command Register
0x01C0 8140	0x01C0 8540	0x01E3 8140	RDRATE	Read Command Rate Register
0x01C0 8240	0x01C0 8640	0x01E3 8240	SAOPT	Source Active Options Register
0x01C0 8244	0x01C0 8644	0x01E3 8244	SASRC	Source Active Source Address Register
0x01C0 8248	0x01C0 8648	0x01E3 8248	SACNT	Source Active Count Register
0x01C0 824C	0x01C0 864C	0x01E3 824C	SADST	Source Active Destination Address Register
0x01C0 8250	0x01C0 8650	0x01E3 8250	SABIDX	Source Active B-Index Register
0x01C0 8254	0x01C0 8654	0x01E3 8254	SAMPPRXY	Source Active Memory Protection Proxy Register
0x01C0 8258	0x01C0 8658	0x01E3 8258	SACNTRLD	Source Active Count Reload Register
0x01C0 825C	0x01C0 865C	0x01E3 825C	SASRCBREF	Source Active Source Address B-Reference Register
0x01C0 8260	0x01C0 8660	0x01E3 8260	SADSTBREF	Source Active Destination Address B-Reference Register
0x01C0 8280	0x01C0 8680	0x01E3 8280	DFCNTRLD	Destination FIFO Set Count Reload Register
0x01C0 8284	0x01C0 8684	0x01E3 8284	DFSRCBREF	Destination FIFO Set Source Address B-Reference Register

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Table 6-13. EDMA3 Transfer Controller (EDMA3TC) Registers (continued)

EDMA0 Transfer Controller 0 BYTE ADDRESS	EDMA0 Transfer Controller 1 BYTE ADDRESS	EDMA1 Transfer Controller 0 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C0 8288	0x01C0 8688	0x01E3 8288	DFDSTBREF	Destination FIFO Set Destination Address B-Reference Register
0x01C0 8300	0x01C0 8700	0x01E3 8300	DFOPT0	Destination FIFO Options Register 0
0x01C0 8304	0x01C0 8704	0x01E3 8304	DFSRC0	Destination FIFO Source Address Register 0
0x01C0 8308	0x01C0 8708	0x01E3 8308	DFCNT0	Destination FIFO Count Register 0
0x01C0 830C	0x01C0 870C	0x01E3 830C	DFDST0	Destination FIFO Destination Address Register 0
0x01C0 8310	0x01C0 8710	0x01E3 8310	DFBIDX0	Destination FIFO B-Index Register 0
0x01C0 8314	0x01C0 8714	0x01E3 8314	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
0x01C0 8340	0x01C0 8740	0x01E3 8340	DFOPT1	Destination FIFO Options Register 1
0x01C0 8344	0x01C0 8744	0x01E3 8344	DFSRC1	Destination FIFO Source Address Register 1
0x01C0 8348	0x01C0 8748	0x01E3 8348	DFCNT1	Destination FIFO Count Register 1
0x01C0 834C	0x01C0 874C	0x01E3 834C	DFDST1	Destination FIFO Destination Address Register 1
0x01C0 8350	0x01C0 8750	0x01E3 8350	DFBIDX1	Destination FIFO B-Index Register 1
0x01C0 8354	0x01C0 8754	0x01E3 8354	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
0x01C0 8380	0x01C0 8780	0x01E3 8380	DFOPT2	Destination FIFO Options Register 2
0x01C0 8384	0x01C0 8784	0x01E3 8384	DFSRC2	Destination FIFO Source Address Register 2
0x01C0 8388	0x01C0 8788	0x01E3 8388	DFCNT2	Destination FIFO Count Register 2
0x01C0 838C	0x01C0 878C	0x01E3 838C	DFDST2	Destination FIFO Destination Address Register 2
0x01C0 8390	0x01C0 8790	0x01E3 8390	DFBIDX2	Destination FIFO B-Index Register 2
0x01C0 8394	0x01C0 8794	0x01E3 8394	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
0x01C0 83C0	0x01C0 87C0	0x01E3 83C0	DFOPT3	Destination FIFO Options Register 3
0x01C0 83C4	0x01C0 87C4	0x01E3 83C4	DFSRC3	Destination FIFO Source Address Register 3
0x01C0 83C8	0x01C0 87C8	0x01E3 83C8	DFCNT3	Destination FIFO Count Register 3
0x01C0 83CC	0x01C0 87CC	0x01E3 83CC	DFDST3	Destination FIFO Destination Address Register 3
0x01C0 83D0	0x01C0 87D0	0x01E3 83D0	DFBIDX3	Destination FIFO B-Index Register 3
0x01C0 83D4	0x01C0 87D4	0x01E3 83D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3

Table 6-14 shows an abbreviation of the set of registers which make up the parameter set for each of 128 EDMA events. Each of the parameter register sets consist of 8 32-bit word entries. Table 6-15 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.

Table 6-14. EDMA Parameter Set RAM

EDMA0 Channel Controller 0 BYTE ADDRESS RANGE	EDMA1 Channel Controller 0 BYTE ADDRESS RANGE	DESCRIPTION
0x01C0 4000 - 0x01C0 401F	0x01E3 4000 - 0x01E3 401F	Parameters Set 0 (8 32-bit words)
0x01C0 4020 - 0x01C0 403F	0x01E3 4020 - 0x01E3 403F	Parameters Set 1 (8 32-bit words)
0x01C0 4040 - 0x01CC0 405F	0x01E3 4040 - 0x01CE3 405F	Parameters Set 2 (8 32-bit words)
0x01C0 4060 - 0x01C0 407F	0x01E3 4060 - 0x01E3 407F	Parameters Set 3 (8 32-bit words)
0x01C0 4080 - 0x01C0 409F	0x01E3 4080 - 0x01E3 409F	Parameters Set 4 (8 32-bit words)
0x01C0 40A0 - 0x01C0 40BF	0x01E3 40A0 - 0x01E3 40BF	Parameters Set 5 (8 32-bit words)
...	...	...
0x01C0 4FC0 - 0x01C0 4FDF	0x01E3 4FC0 - 0x01E3 4FDF	Parameters Set 126 (8 32-bit words)
0x01C0 4FE0 - 0x01C0 4FFF	0x01E3 4FE0 - 0x01E3 4FFF	Parameters Set 127 (8 32-bit words)

Table 6-15. Parameter Set Entries

OFFSET BYTE ADDRESS WITHIN THE PARAMETER SET	ACRONYM	PARAMETER ENTRY
0x0000	OPT	Option
0x0004	SRC	Source Address
0x0008	A_B_CNT	A Count, B Count
0x000C	DST	Destination Address
0x0010	SRC_DST_BIDX	Source B Index, Destination B Index
0x0014	LINK_BCNTRLD	Link Address, B Count Reload
0x0018	SRC_DST_CIDX	Source C Index, Destination C Index
0x001C	CCNT	C Count

6.10 External Memory Interface A (EMIFA)

EMIFA is one of two external memory interfaces supported on the device. It is primarily intended to support asynchronous memory types, such as NAND and NOR flash and Asynchronous SRAM. However on this device, EMIFA also provides a secondary interface to SDRAM.

6.10.1 EMIFA Asynchronous Memory Support

EMIFA supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIFA data bus width is up to 16-bits.The device supports up to 24 address lines and two external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIFA (EMA_CS[5:2]).

Each chip select has the following individually programmable attributes:

- Data Bus Width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes.

6.10.2 EMIFA Synchronous DRAM Memory Support

The device supports 16-bit SDRAM in addition to the asynchronous memories listed in Section 6.10.1. It has a single SDRAM chip select (EMA_CS[0]). SDRAM configurations that are supported are:

- One, Two, and Four Bank SDRAM devices
- Devices with Eight, Nine, Ten, and Eleven Column Address
- CAS Latency of two or three clock cycles
- Sixteen Bit Data Bus Width

Additionally, the SDRAM interface of EMIFA supports placing the SDRAM in Self Refresh and Powerdown Modes. Self Refresh mode allows the SDRAM to be put into a low power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the device. Powerdown mode achieves even lower power, except the device must periodically wake the SDRAM up and issue refreshes if data retention is required.

Finally, note that the EMIFA does not support Mobile SDRAM devices.

Table 6-16 shows the supported SDRAM configurations for EMIFA.

Table 6-16. EMIFA Supported SDRAM Configurations(1)

SDRAM Memory Data Bus Width (bits)	Number of Memories	EMIFA Data Bus Size (bits)	Rows	Columns	Banks	Total Memory (Mbits)	Total Memory (Mbytes)	Memory Density (Mbits)
16	1	16	16	8	1	256	32	256
	1	16	16	8	2	512	64	512
	1	16	16	8	4	1024	128	1024
	1	16	16	9	1	512	64	512
	1	16	16	9	2	1024	128	1024
	1	16	16	9	4	2048	256	2048
	1	16	16	10	1	1024	128	1024
	1	16	16	10	2	2048	256	2048
	1	16	16	10	4	4096	512	4096
	1	16	16	11	1	2048	256	2048
	1	16	16	11	2	4096	512	4096
	1	16	15	11	4	4096	512	4096
8	2	16	16	8	1	256	32	128
	2	16	16	8	2	512	64	256
	2	16	16	8	4	1024	128	512
	2	16	16	9	1	512	64	256
	2	16	16	9	2	1024	128	512
	2	16	16	9	4	2048	256	1024
	2	16	16	10	1	1024	128	512
	2	16	16	10	2	2048	256	1024
	2	16	16	10	4	4096	512	2048
	2	16	16	11	1	2048	256	1024
	2	16	16	11	2	4096	512	2048
	2	16	15	11	4	4096	512	2048

(1) The shaded cells indicate configurations that are possible on the EMIFA interface but as of this writing SDRAM memories capable of supporting these densities are not available in the market.

6.10.3 EMIFA SDRAM Loading Limitations

EMIFA supports SDRAM up to 100 MHz with up to two SDRAM or asynchronous memory loads. Additional loads will limit the SDRAM operation to lower speeds and the maximum speed should be confirmed by board simulation using IBIS models.

6.10.5 External Memory Interface Register Descriptions

Table 6-17 is a list of the EMIF registers. For more information about these registers, see the C674x DSP External Memory Interface (EMIF) User's Guide (literature number SPRUFL6).

Table 6-17. External Memory Interface (EMIFA) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x6800 0000	MIDR	Module ID Register
0x6800 0004	AWCC	Asynchronous Wait Cycle Configuration Register
0x6800 0008	SDCR	SDRAM Configuration Register
0x6800 000C	SDRCR	SDRAM Refresh Control Register
0x6800 0010	CE2CFG	Asynchronous 1 Configuration Register
0x6800 0014	CE3CFG	Asynchronous 2 Configuration Register
0x6800 0018	CE4CFG	Asynchronous 3 Configuration Register
0x6800 001C	CE5CFG	Asynchronous 4 Configuration Register
0x6800 0020	SDTIMR	SDRAM Timing Register
0x6800 003C	SDSRETR	SDRAM Self Refresh Exit Timing Register
0x6800 0040	INTRAW	EMIFA Interrupt Raw Register
0x6800 0044	INTMSK	EMIFA Interrupt Mask Register
0x6800 0048	INTMSKSET	EMIFA Interrupt Mask Set Register
0x6800 004C	INTMSKCLR	EMIFA Interrupt Mask Clear Register
0x6800 0060	NANDFCR	NAND Flash Control Register
0x6800 0064	NANDFSR	NAND Flash Status Register
0x6800 0070	NANDF1ECC	NAND Flash 1 ECC Register (CS2 Space)
0x6800 0074	NANDF2ECC	NAND Flash 2 ECC Register (CS3 Space)
0x6800 0078	NANDF3ECC	NAND Flash 3 ECC Register (CS4 Space)
0x6800 007C	NANDF4ECC	NAND Flash 4 ECC Register (CS5 Space)
0x6800 00BC	NAND4BITECCLOAD	NAND Flash 4-Bit ECC Load Register
0x6800 00C0	NAND4BITECC1	NAND Flash 4-Bit ECC Register 1
0x6800 00C4	NAND4BITECC2	NAND Flash 4-Bit ECC Register 2
0x6800 00C8	NAND4BITECC3	NAND Flash 4-Bit ECC Register 3
0x6800 00CC	NAND4BITECC4	NAND Flash 4-Bit ECC Register 4
0x6800 00D0	NANDERRADD1	NAND Flash 4-Bit ECC Error Address Register 1
0x6800 00D4	NANDERRADD2	NAND Flash 4-Bit ECC Error Address Register 2
0x6800 00D8	NANDERRVAL1	NAND Flash 4-Bit ECC Error Value Register 1
0x6800 00DC	NANDERRVAL2	NAND Flash 4-Bit ECC Error Value Register 2

6.10.6 EMIFA Electrical Data/Timing

Table 6-18 through Table 6-21 assume testing over recommended operating conditions.

Table 6-18. Timing Requirements for EMIFA SDRAM Interface

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
19	$t_{su(EMA\_DV-EM\_CLKH)}$	Input setup time, read data valid on EMA_D[31:0] before EMA_CLK rising	2		3		3		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMA_D[31:0] after EMA_CLK rising	1.6		1.6		1.6		ns

Table 6-19. Switching Characteristics for EMIFA SDRAM Interface

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMA_CLK	10		15		20		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMA_CLK high or low	3		5		8		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMA_CLK rising to $\overline{EMA\_CS[0]}$ valid		7		9.5		13	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA\_CS[0]}$ invalid	1		1		1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] valid		7		9.5		13	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid	1		1		1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] valid		7		9.5		13	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid	1		1		1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMA_CLK rising to EMA_D[15:0] valid		7		9.5		13	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMA_CLK rising to EMA_D[15:0] invalid	1		1		1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMA_CLK rising to $\overline{EMA\_RAS}$ valid		7		9.5		13	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA\_RAS}$ invalid	1		1		1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMA_CLK rising to $\overline{EMA\_CAS}$ valid		7		9.5		13	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA\_CAS}$ invalid	1		1		1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMA_CLK rising to $\overline{EMA\_WE}$ valid		7		9.5		13	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA\_WE}$ invalid	1		1		1		ns
17	$t_{dis(CLKH-DHZ)}$	Delay time, EMA_CLK rising to EMA_D[15:0] tri-stated		7		9.5		13	ns
18	$t_{ena(CLKH-DLZ)}$	Output hold time, EMA_CLK rising to EMA_D[15:0] driving	1		1		1		ns

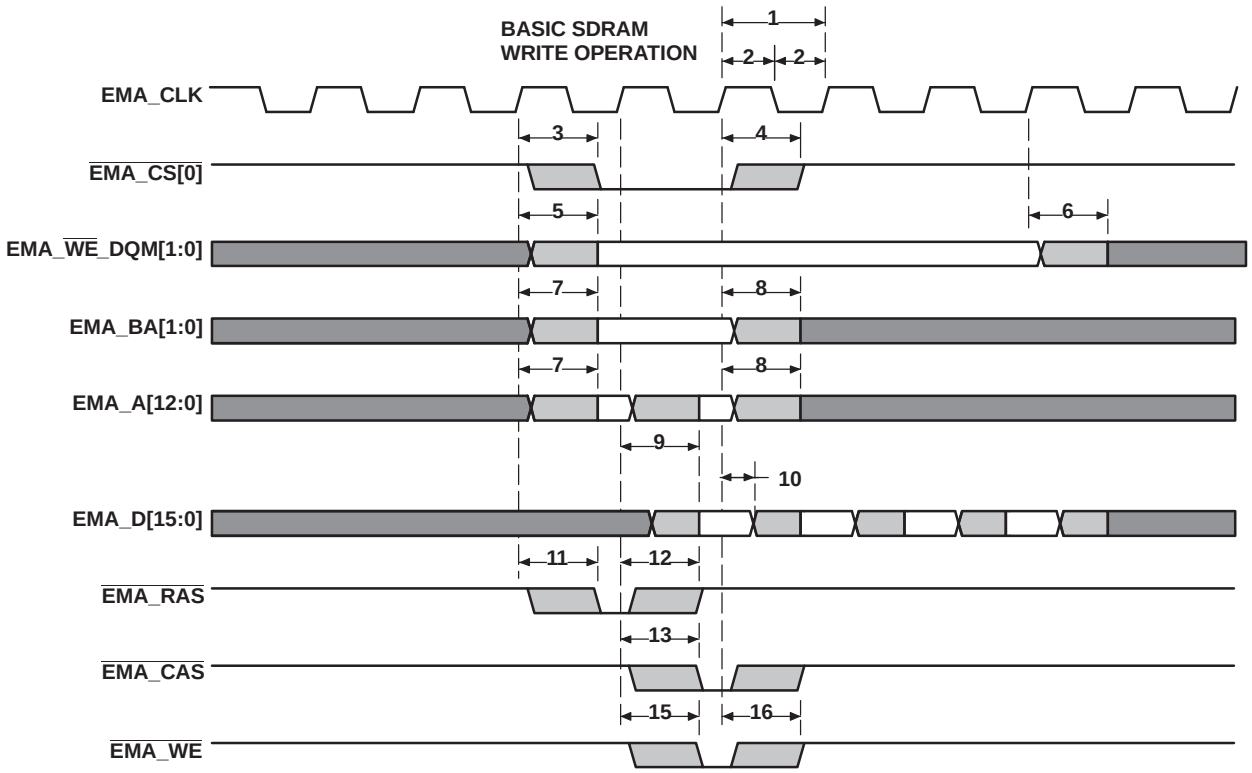

Figure 6-12. EMIFA Basic SDRAM Write Operation

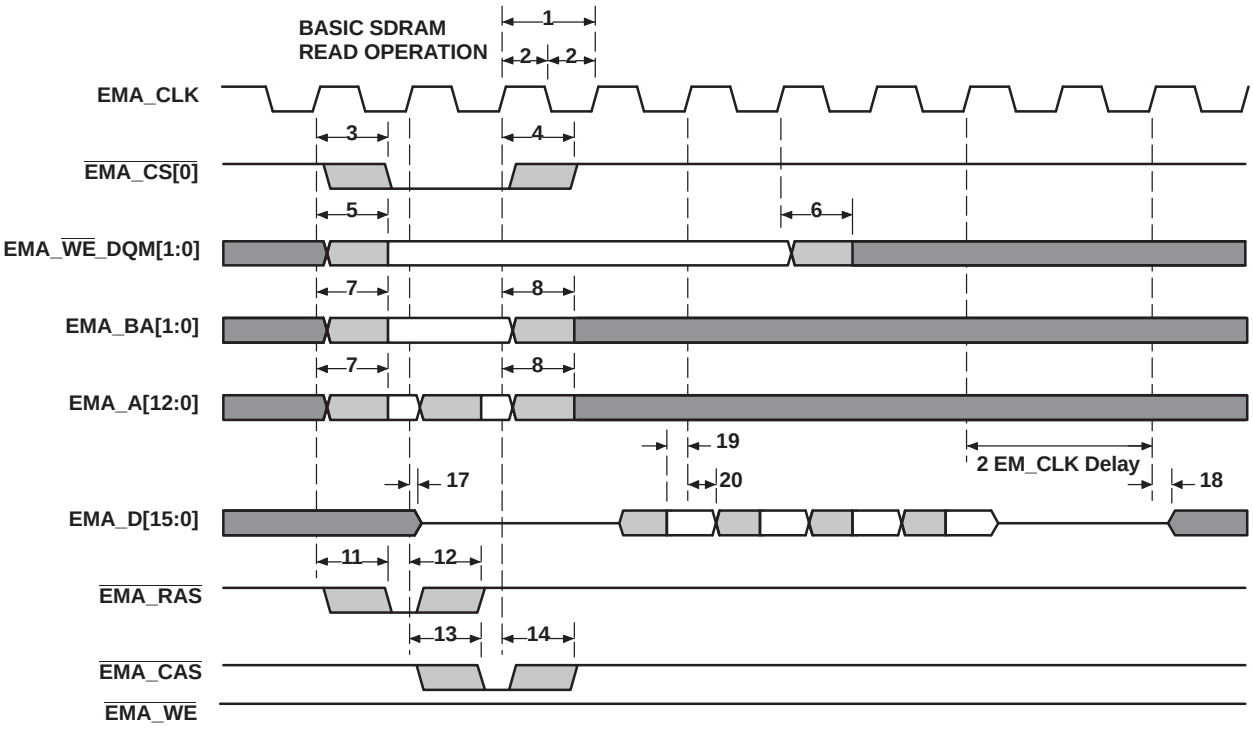

Figure 6-13. EMIFA Basic SDRAM Read Operation

Table 6-20. Timing Requirements for EMIFA Asynchronous Memory Interface (1)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
READS and WRITES									
2	$t_{w(EM\_WAIT)}$	Pulse duration, EM_WAIT assertion and deassertion	2E		2E		2E		ns
READS									
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM\_OE}$ high	3		TBD		TBD		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM\_OE}$ high	0.5		TBD		TBD		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EM_WAIT asserted before end of Strobe Phase (2)	4E+3		4E+3		4E+3		ns
WRITES									
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EM_WAIT asserted before end of Strobe Phase (2)	4E+3		4E+3		4E+3		ns

(1) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 6-16 and Figure 6-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 6-21. Switching Characteristics for EMIFA Asynchronous Memory Interface (1)(2)(3)

NO.	PARAMETER		1.2V, 1.1V, 1.0V			UNIT
			MIN	Nom	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 3	(TA)*E	(TA)*E + 3	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 3	(RS+RST+RH)*E	(RS+RST+RH)*E + 3	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 3	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 3	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMA\_CE[5:2]}$ low to $\overline{EMA\_OE}$ low (SS = 0)	(RS)*E-3	(RS)*E	(RS)*E+3	ns
		Output setup time, $\overline{EMA\_CE[5:2]}$ low to $\overline{EMA\_OE}$ low (SS = 1)	-3	0	+3	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMA\_OE}$ high to $\overline{EMA\_CE[5:2]}$ high (SS = 0)	(RH)*E - 3	(RH)*E	(RH)*E + 3	ns
		Output hold time, $\overline{EMA\_OE}$ high to $\overline{EMA\_CE[5:2]}$ high (SS = 1)	-3	0	+3	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, $\overline{EMA\_BA[1:0]}$ valid to $\overline{EMA\_OE}$ low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMA\_OE}$ high to $\overline{EMA\_BA[1:0]}$ invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, $\overline{EMA\_A[13:0]}$ valid to $\overline{EMA\_OE}$ low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMA\_OE}$ high to $\overline{EMA\_A[13:0]}$ invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns
10	$t_{w(EMOEL)}$	$\overline{EMA\_OE}$ active low width (EW = 0)	(RST)*E-3	(RST)*E	(RST)*E+3	ns
		$\overline{EMA\_OE}$ active low width (EW = 1)	(RST+(EWC*16))*E-3	(RST+(EWC*16))*E	(RST+(EWC*16))*E+3	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following range of values: TA[4-1], RS[16-1], RST[64-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256].
(2) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.
(3) EWC = external wait cycles determined by EMA_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 6-21. Switching Characteristics for EMIFA Asynchronous Memory Interface (continued)

NO.	PARAMETER		1.2V, 1.1V, 1.0V			UNIT
			MIN	Nom	MAX	
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMA_WAIT deasserted to EMA_OE high	3E-3	4E	4E+3	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E-3	(WS+WST+WH)*E	(WS+WST+WH)*E+3	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 3	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 3	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, EMA_CE[5:2] low to EMA_WE low (SS = 0)	(WS)*E - 3	(WS)*E	(WS)*E + 3	ns
		Output setup time, EMA_CE[5:2] low to EMA_WE low (SS = 1)	-3	0	+3	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, EMA_WE high to EMA_CE[5:2] high (SS = 0)	(WH)*E-3	(WH)*E	(WH)*E+3	ns
		Output hold time, EMA_WE high to EMA_CE[5:2] high (SS = 1)	-3	0	+3	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMA_BA[1:0] valid to EMA_WE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, EMA_WE high to EMA_BA[1:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMA_BA[1:0] valid to EMA_WE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, EMA_WE high to EMA_BA[1:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMA_A[13:0] valid to EMA_WE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, EMA_WE high to EMA_A[13:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
24	$t_{w(EMWEL)}$	EMA_WE active low width (EW = 0)	(WST)*E-3	(WST)*E	(WST)*E+3	ns
		EMA_WE active low width (EW = 1)	(WST+(EWC*16))*E-3	(WST+(EWC*16))*E	(WST+(EWC*16))*E+3	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMA_WAIT deasserted to EMA_WE high	3E-3	4E	4E+3	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMA_D[15:0] valid to EMA_WE low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, EMA_WE high to EMA_D[15:0] invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns

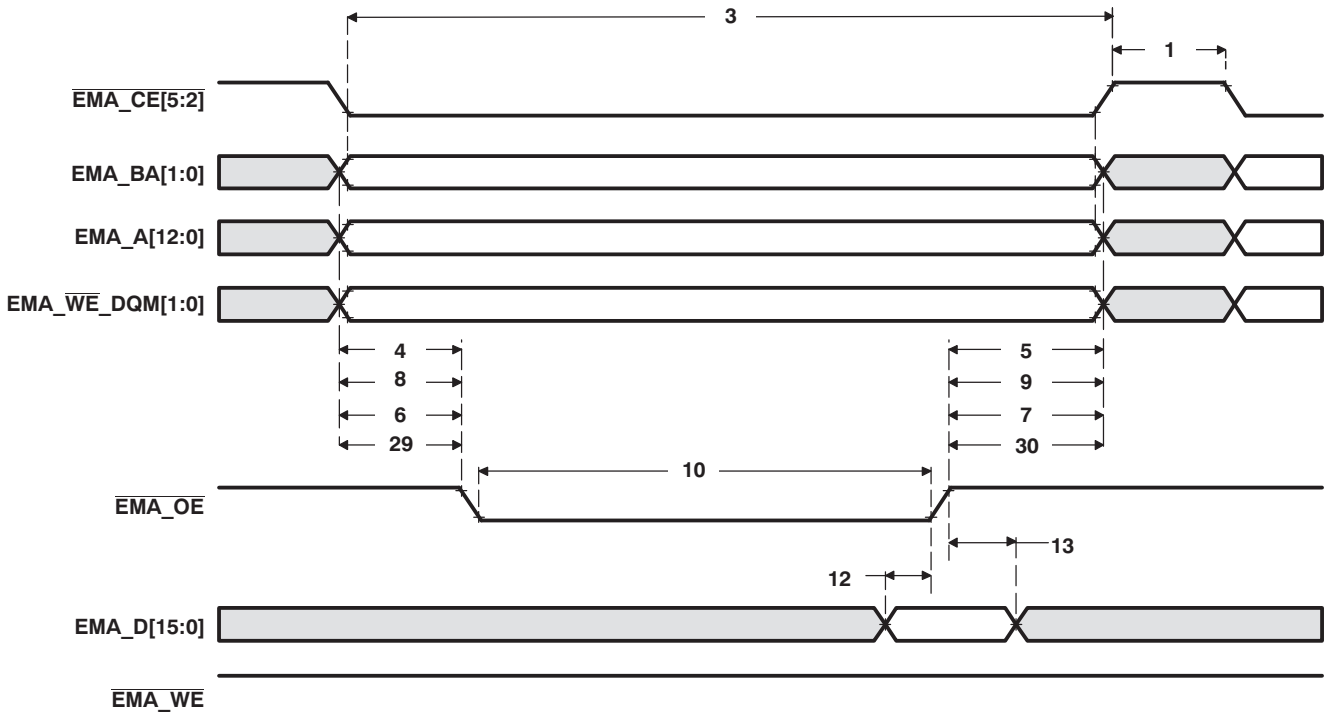

Figure 6-14. Asynchronous Memory Read Timing for EMIFA

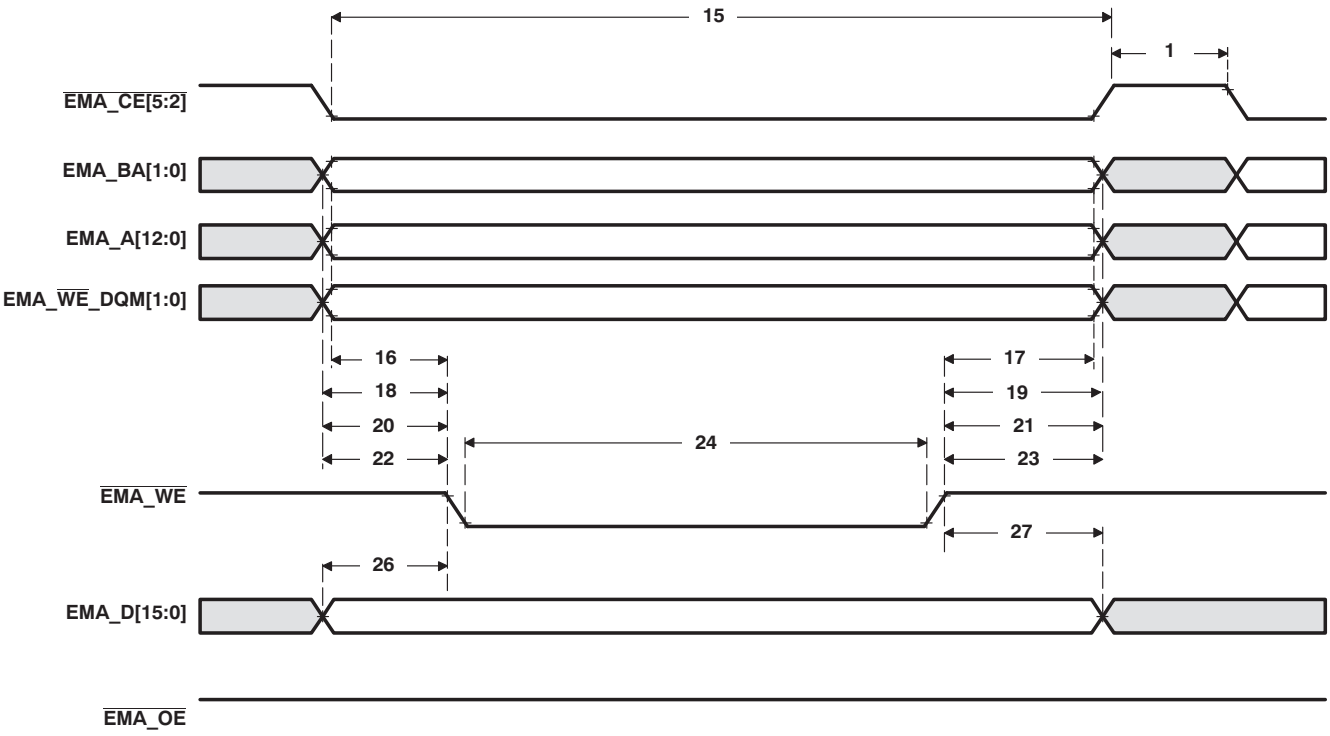

Figure 6-15. Asynchronous Memory Write Timing for EMIFA

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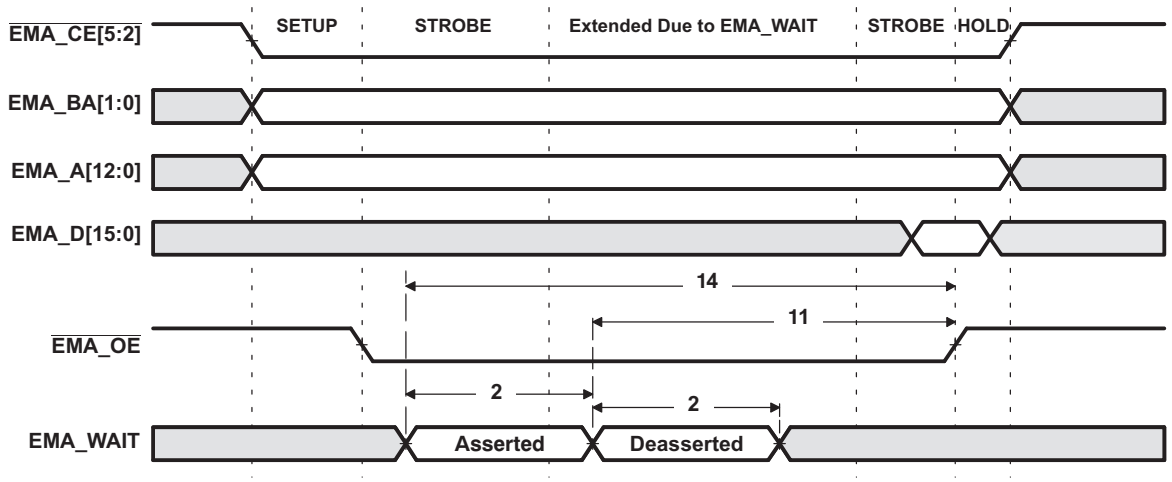

Figure 6-16. EMA_WAIT Read Timing Requirements

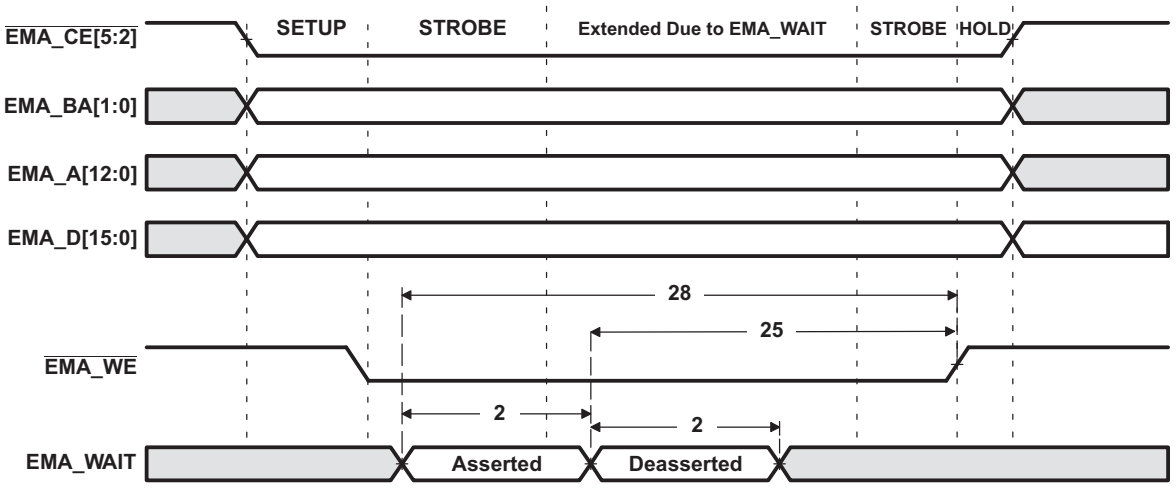

Figure 6-17. EMA_WAIT Write Timing Requirements

6.11 DDR2/mDDR Controller

The DDR2/mDDR Memory Controller is a dedicated interface to DDR2/mDDR SDRAM. It supports JESD79D-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices.

The DDR2/mDDR Memory Controller support the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- Mobile DDR SDRAM
- 512 MByte memory space for DDR2
- 256 MByte memory space for mDDR
- CAS latencies:
  - DDR2: 2, 3, 4 and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4 and 8
  - mDDR:1, 2 and 4
- Burst length: 8
- Burst type: sequential
- 1 chip select (CS) signal
- Page sizes: 256, 512, 1024 and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

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6.11.1 DDR2/mDDR Memory Controller Electrical Data/Timing

Table 6-22. Switching Characteristics Over Recommended Operating Conditions for DDR2/mDDR Memory Controller

No.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(DDR\_CLK)}$	Cycle time, DDR_CLKP / DDR_CLKN	DDR2	125	150	125	150	—(1)	—(1)	MHz
			mDDR	100	133	100	133	100	133	

(1) DDR2 is not supported at this voltage operating point.

6.11.2 DDR2/mDDR Controller Register Description(s)

Table 6-23. DDR2/mDDR Controller Registers

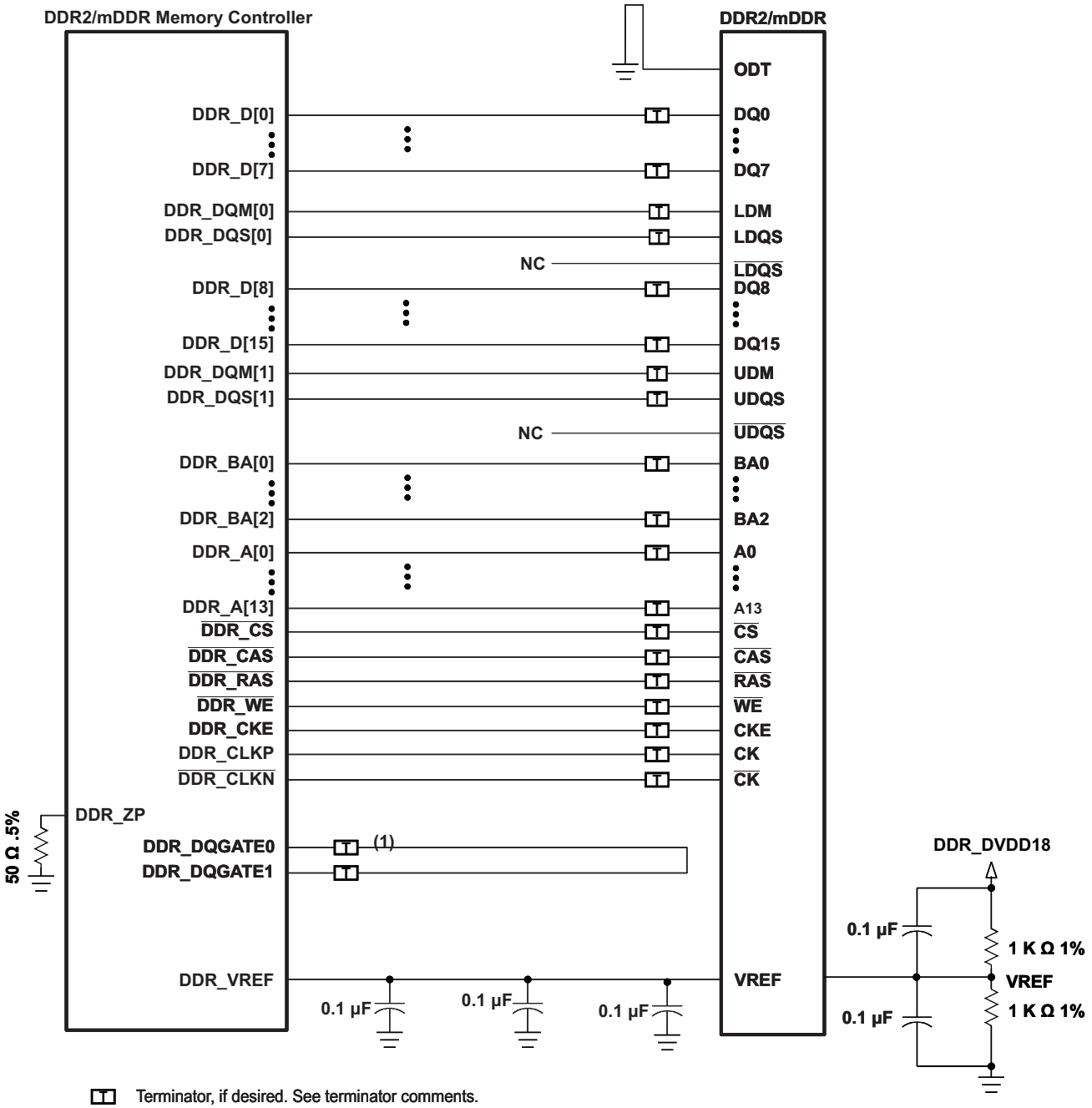
BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0xB000 0000	REVID	Revision ID Register
0xB000 0004	SDRSTAT	SDRAM Status Register
0xB000 0008	SDCR	SDRAM Configuration Register
0xB000 000C	SDRCR	SDRAM Refresh Control Register
0xB000 0010	SDTIMR1	SDRAM Timing Register 1
0xB000 0014	SDTIMR2	SDRAM Timing Register 2
0xB000 001C	SDCR2	SDRAM Configuration Register 2
0xB000 0020	PBBPR	Peripheral Bus Burst Priority Register
0xB000 0040	PC1	Performance Counter 1 Registers
0xB000 0044	PC2	Performance Counter 2 Register
0xB000 0048	PCC	Performance Counter Configuration Register
0xB000 004C	PCMRS	Performance Counter Master Region Select Register
0xB000 0050	PCT	Performance Counter Time Register
0xB000 00C0	IRR	Interrupt Raw Register
0xB000 00C4	IMR	Interrupt Mask Register
0xB000 00C8	IMSR	Interrupt Mask Set Register
0xB000 00CC	IMCR	Interrupt Mask Clear Register
0xB000 00E4	DRPYC1R	DDR PHY Control Register 1
0x01E2 C000	VTPIO_CTL	VTP IO Control Register

6.11.3 DDR2/mDDR Interface

This section provides the timing specification for the DDR2/mDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2/mDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2/mDDR specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

6.11.3.1 DDR2/mDDR Interface Schematic

Figure 6-18 shows the DDR2/mDDR interface schematic for a single-memory DDR2/mDDR system. The dual-memory system shown in Figure 6-19. Pin numbers for the device can be obtained from the pin description section.



(1) See Figure 6-25 for DQGATE routing specifications.

Figure 6-18. DDR2/mDDR Single-Memory High Level Schematic

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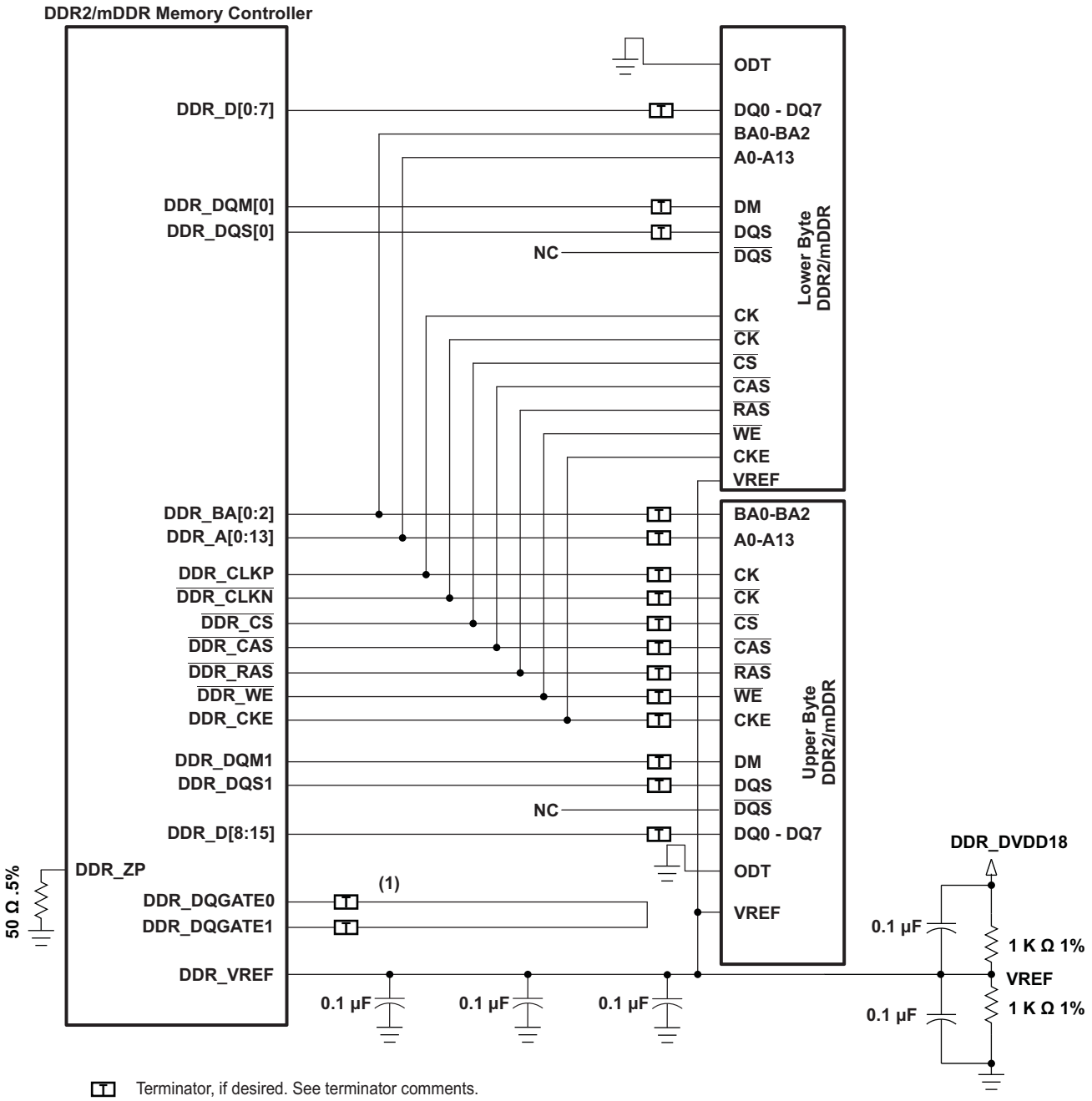

Terminator, if desired. See terminator comments.

(1) See Figure 6-25 for DQGATE routing specifications.

Figure 6-19. DDR2/mDDR Dual-Memory High Level Schematic

6.11.3.2 Compatible JEDEC DDR2/mDDR Devices

Table 6-24 shows the parameters of the JEDEC DDR2/mDDR devices that are compatible with this interface. Generally, the DDR2/mDDR interface is compatible with x16 DDR2/mDDR-400 speed grade DDR2/mDDR devices.

The device also supports JEDEC DDR2/mDDR x8 devices in the dual chip configuration. In this case, one chip supplies the upper byte and the second chip supplies the lower byte. Addresses and most control signals are shared just like regular dual chip memory configurations.

Table 6-24. Compatible JEDEC DDR2/mDDR Devices

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2/mDDR Device Speed Grade	DDR2/mDDR-400			See Note (1)
2	JEDEC DDR2/mDDR Device Bit Width	x8	x16	Bits	
3	JEDEC DDR2/mDDR Device Count	1	2	Devices	

(1) Higher DDR2/mDDR speed grades are supported due to inherent JEDEC DDR2/mDDR backwards compatibility.

6.11.3.3 PCB Stackup

The minimum stackup required for routing the device is a six layer stack as shown in Table 6-25. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.Complete stack up specifications are provided in Table 6-26.

Table 6-25. C6748 Minimum PCB Stack Up

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

Table 6-26. PCB Stack Up Specifications

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PCB Routing/Plane Layers	6				
2	Signal Routing Layers	3				
3	Full ground layers under DDR2/mDDR routing region	2				
4	Number of ground plane cuts allowed within DDR routing region			0		
5	Number of ground reference planes required for each DDR2/mDDR routing layer	1				
6	Number of layers between DDR2/mDDR routing layer and reference ground plane			0		
7	PCB Routing Feature Size		4		Mils	
8	PCB Trace Width w		4		Mils	
8	PCB BGA escape via pad size		18		Mils	
9	PCB BGA escape via hole size		8		Mils	
10	DSP Device BGA pad size					See Note (1)
11	DDR2/mDDR Device BGA pad size					See Note (2)
12	Single Ended Impedance, Zo	50		75	Ω	
13	Impedance Control	Z-5	Z	Z+5	Ω	See Note (3)

(1) Please refer to the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for device BGA pad size.
(2) Please refer to the DDR2/mDDR device manufacturer documentation for the DDR2/mDDR device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

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6.11.3.4 Placement

Figure 6-19 shows the required placement for the C6748 device as well as the DDR2/mDDR devices. The dimensions for Figure 6-20 are defined in Table 6-27. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2/mDDR systems, the second DDR2/mDDR device is omitted from the placement.

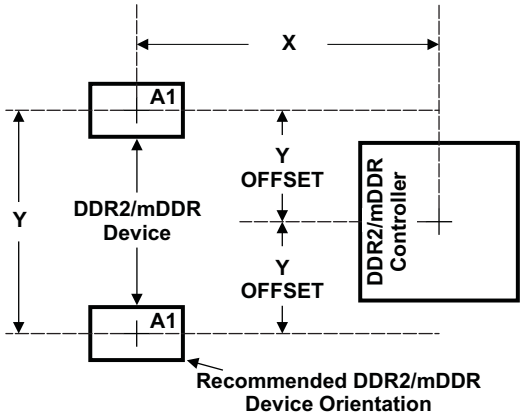


Figure 6-20. C6748 and DDR2/mDDR Device Placement

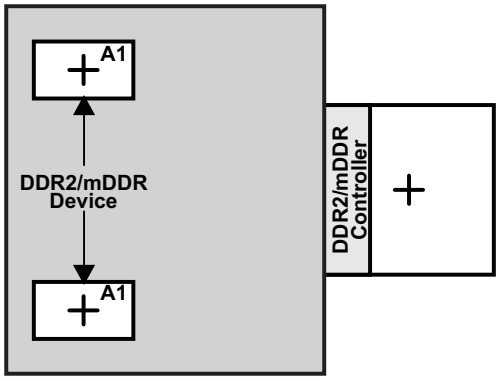
Table 6-27. Placement Specifications

No.	Parameter	Min	Max	Unit	Notes
1	X		1750	Mils	See Notes (1), (2)
2	Y		1280	Mils	See Notes (1), (2)
3	Y Offset		650	Mils	See Notes (1), (2), (3)
4	Clearance from non-DDR2/mDDR signal to DDR2/mDDR Keepout Region	4		w	See Note (4)

(1) See Figure 6-20 for dimension definitions.
(2) Measurements from center of device to center of DDR2/mDDR device.
(3) For single memory systems it is recommended that Y Offset be as small as possible.
(4) Non-DDR2/mDDR signals allowed within DDR2/mDDR keepout region provided they are separated from DDR2/mDDR routing layers by a ground plane.

6.11.3.5 DDR2/mDDR Keep Out Region

The region of the PCB used for the DDR2/mDDR circuitry must be isolated from other signals. The DDR2/mDDR keep out region is defined for this purpose and is shown in Figure 6-21. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 6-27.



Region should encompass all DDR2/mDDR circuitry and varies depending on placement. Non-DDR2/mDDR signals should not be routed on the DDR signal layers within the DDR2/mDDR keep out region. Non-DDR2/mDDR signals may be routed in the region provided they are routed on layers separated from DDR2/mDDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 6-21. DDR2/mDDR Keepout Region

6.11.3.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2/mDDR and other circuitry. Table 6-28 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DSP and DDR2/mDDR interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

Table 6-28. Bulk Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	DDR_DVDD18 Supply Bulk Bypass Capacitor Count	3		Devices	See Note (1)
2	DDR_DVDD18 Supply Bulk Bypass Total Capacitance	30		µF	
3	DDR#1 Bulk Bypass Capacitor Count	1		Devices	See Note (1)
4	DDR#1 Bulk Bypass Total Capacitance	22		µF	
5	DDR#2 Bulk Bypass Capacitor Count	1		Devices	See Notes (1), (2)
6	DDR#2 Bulk Bypass Total Capacitance	22		µF	See Note (2)

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on dual-memory systems

6.11.3.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2/mDDR interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, DSP/DDR2/mDDR power, and DSP/DDR2/mDDR ground connections. Table 6-29 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

Table 6-29. High-Speed Bypass Capacitors

No.	Parameter	Min	Max	Unit	Notes
1	HS Bypass Capacitor Package Size		0402	10 Mils	See Note (1)
2	Distance from HS bypass capacitor to device being bypassed		250	Mils	
3	Number of connection vias for each HS bypass capacitor	2		Vias	See Note (2)
4	Trace length from bypass capacitor contact to connection via	1	30	Mils	
5	Number of connection vias for each DDR2/mDDR device power or ground balls	1		Vias	
6	Trace length from DDR2/mDDR device power ball to connection via		35	Mils	
7	DDR_DVDD18 Supply HS Bypass Capacitor Count	10		Devices	See Note (3)
8	DDR_DVDD18 Supply HS Bypass Capacitor Total Capacitance	0.6		µF	
9	DDR#1 HS Bypass Capacitor Count	8		Devices	See Note (3)
10	DDR#1 HS Bypass Capacitor Total Capacitance	0.4		µF	
11	DDR#2 HS Bypass Capacitor Count	8		Devices	See Notes (3), (4)
12	DDR#2 HS Bypass Capacitor Total Capacitance	0.4		µF	See Note (4)

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on dual-memory systems

6.11.3.8 Net Classes

Table 6-30 lists the clock net classes for the DDR2/mDDR interface. Table 6-31 lists the signal net classes, and associated clock net classes, for the signals in the DDR2/mDDR interface. These net classes are used for the termination and routing rules that follow.

Table 6-30. Clock Net Class Definitions

Clock Net Class	DSP Pin Names
CK	DDR_CLKP / $\overline{\text{DDR\_CLKN}}$
DQS0	DDR_DQS[0]
DQS1	DDR_DQS[1]

Table 6-31. Signal Net Class Definitions

Clock Net Class	Associated Clock Net Class	DSP Pin Names
ADDR_CTRL	CK	DDR_BA[2:0], DDR_A[13:0], $\overline{\text{DDR\_CS}}$, $\overline{\text{DDR\_CAS}}$, $\overline{\text{DDR\_RAS}}$, $\overline{\text{DDR\_WE}}$, DDR_CKE
D0	DQS0	DDR_D[7:0], DDR_DQM0
D1	DQS1	DDR_D[15:8], DDR_DQM1
DQGATE	CK, DQS0, DQS1	DDR_DQGATE0, DDR_DQGATE1

6.11.3.9 DDR2/mDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-32 shows the specifications for the series terminators.

Table 6-32. DDR2/mDDR Signal Terminations

No.	Parameter	Min	Typ	Max	Unit	Notes
1	CK Net Class	0		10	Ω	See Note (1)
2	ADDR_CTRL Net Class	0	22	Zo	Ω	See Notes (1), (2), (3)
3	Data Byte Net Classes (DQS[0], DQS[1], D0, D1)	0	22	Zo	Ω	See Notes (1), (2), (3), (4)
4	DQGATE Net Class (DQGATE)	0	10	Zo	Ω	See Notes (1), (2), (3)

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ω), the DDR2/mDDR devices must be programmed to operate in 60% strength mode.

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6.11.3.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2/mDDR memories as well as the C6748. VREF is intended to be half the DDR2/mDDR power supply voltage and should be created using a resistive divider as shown in Figure 6-18. Other methods of creating VREF are not recommended. Figure 6-22 shows the layout guidelines for VREF.

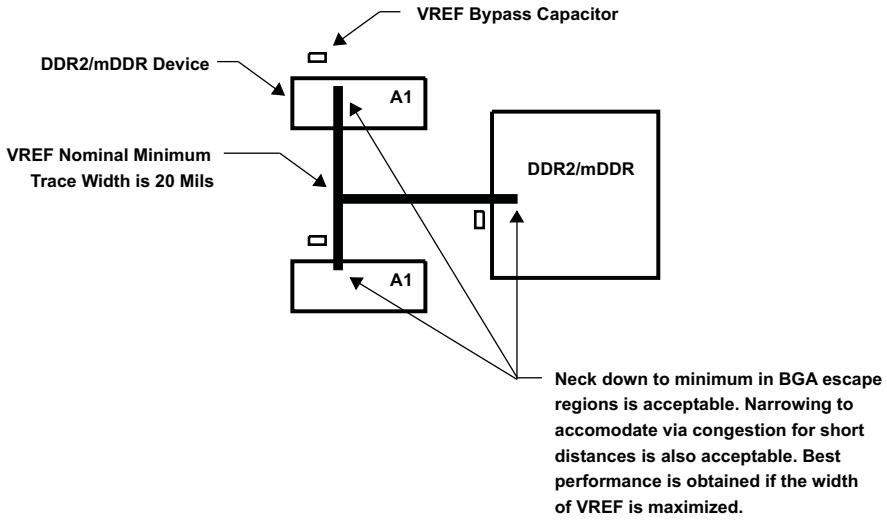

Figure 6-22. VREF Routing and Topology

6.11.3.11 DDR2/mDDR CK and ADDR_CTRL Routing

Figure 6-23 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

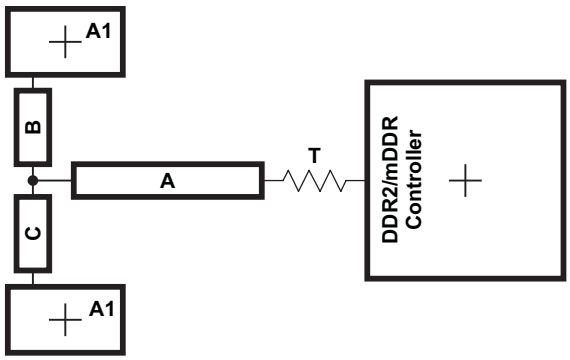

Figure 6-23. CK and ADDR_CTRL Routing and Topology

Table 6-33. CK and ADDR_CTRL Routing Specification

No.	Parameter	Min	Typ	Max	Unit	Notes
1	CK A to B/A to C Skew Length Mismatch			25	Mils	See Note (1)
2	CK B to C Skew Length Mismatch			25	Mils	
3	Center to center CK to other DDR2/mDDR trace spacing	4w				See Note (2)
4	CK/ADDR_CTRL nominal trace length	CACLM-50	CACLM	CACLM+50	Mils	See Note (3)
5	ADDR_CTRL to CK Skew Length Mismatch			100	Mils	
6	ADDR_CTRL to ADDR_CTRL Skew Length Mismatch			100	Mils	
7	Center to center ADDR_CTRL to other DDR2/mDDR trace spacing	4w				See Note (2)
8	Center to center ADDR_CTRL to other ADDR_CTRL trace spacing	3w				See Note (2)
9	ADDR_CTRL A to B/A to C Skew Length Mismatch			100	Mils	See Note (1)
10	ADDR_CTRL B to C Skew Length Mismatch			100	Mils	

(1) Series terminator, if used, should be located closest to DSP.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 6-24 shows the topology and routing for the DQS and DQ net class; the routes are point to point. Skew matching across bytes is not needed nor recommended.

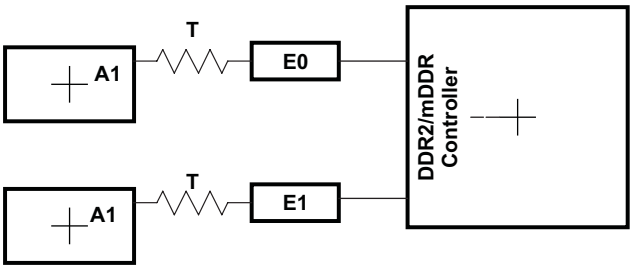

Figure 6-24. DQS and DQ Routing and Topology

Table 6-34. DQS and DQ Routing Specification

No.	Parameter	Min	Typ	Max	Unit	Notes
1	DQS E Skew Length Mismatch			25	Mils	
2	Center to center DQS to other DDR2/mDDR trace spacing	4w				See Note (1)
3	DQS/D nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	See Notes (2), (3)
4	D to DQS Skew Length Mismatch			100	Mils	See Note (3)
5	D to D Skew Length Mismatch			100	Mils	See Note (3)
6	Center to center D to other DDR2/mDDR trace spacing	4w				See Notes (1), (4)
7	Center to Center D to other D trace spacing	3w				See Notes (5), (1)
8	DQ/DQS E Skew Length Mismatch			100	Mils	See Note (3)

(1) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) Series terminator, if used, should be located closest to DDR.
(3) There is no need and it is not recommended to skew match across data bytes, i.e., from DQS0 and data byte 0 to DQS1 and data byte 1.
(4) D's from other DQS domains are considered *other DDR2/mDDR trace*.
(5) DQLM is the longest Manhattan distance of each of the DQS and D net class.

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Figure 6-25 shows the routing for the DQGATE net class. Table 6-35 contains the routing specification.

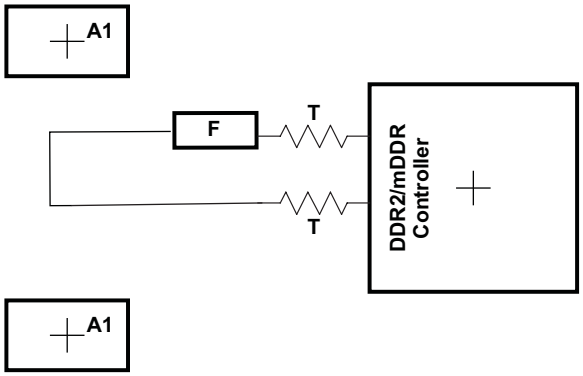

Figure 6-25. DQGATE Routing

Table 6-35. DQGATE Routing Specification

No.	Parameter	Min	Typ	Max	Unit	Notes
1	DQGATE Length F		CKB0B1			See Note (1)
2	Center to center DQGATE to any other trace spacing	4w				
3	DQS/D nominal trace length	DQLM-50	DQLM	DQLM+50	Mils	
4	DQGATE Skew			100	Mils	See Note (2)

(1) CKB0B1 is the sum of the length of the CK net plus the average length of the DQS0 and DQS1 nets.
(2) Skew from CKB0B1

6.12 MMC / SD / SDIO (MMCSD0, MMCSD1)

6.12.1 MMCSD Peripheral Description

The device includes an two MMCSD controllers which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V1.1 and Secure Digital Input Output (SDIO) V2.0 specifications.

The MMC/SD Controller have following features:

- MultiMediaCard (MMC).
- Secure Digital (SD) Memory Card.
- MMC/SD protocol support.
- SDIO protocol support.
- Programmable clock frequency.
- 512 bit Read/Write FIFO to lower system overhead.
- Slave EDMA transfer capability.

The device MMC/SD Controller does not support SPI mode.

6.12.2 MMCSD Peripheral Register Description(s)

Table 6-36. Multimedia Card/Secure Digital (MMC/SD) Card Controller Registers

MMCSD0 BYTE ADDRESS	MMCSD1 BYTE ADDRESS	ACRONYM	REGISTER DESCSRIPTION
0x01C4 0000	0x01E1 B000	MMCCTL	MMC Control Register
0x01C4 0004	0x01E1 B004	MMCCLK	MMC Memory Clock Control Register
0x01C4 0008	0x01E1 B008	MMCST0	MMC Status Register 0
0x01C4 000C	0x01E1 B00C	MMCST1	MMC Status Register 1
0x01C4 0010	0x01E1 B010	MMCIM	MMC Interrupt Mask Register
0x01C4 0014	0x01E1 B014	MMCTOR	MMC Response Time-Out Register
0x01C4 0018	0x01E1 B018	MMCTOD	MMC Data Read Time-Out Register
0x01C4 001C	0x01E1 B01C	MMCBLEN	MMC Block Length Register
0x01C4 0020	0x01E1 B020	MMCNBLK	MMC Number of Blocks Register
0x01C4 0024	0x01E1 B024	MMCNBLC	MMC Number of Blocks Counter Register
0x01C4 0028	0x01E1 B028	MMCDRR	MMC Data Receive Register
0x01C4 002C	0x01E1 B02C	MMCDXR	MMC Data Transmit Register
0x01C4 0030	0x01E1 B030	MMCCMD	MMC Command Register
0x01C4 0034	0x01E1 B034	MMCARGHL	MMC Argument Register
0x01C4 0038	0x01E1 B038	MMCRSP01	MMC Response Register 0 and 1
0x01C4 003C	0x01E1 B03C	MMCRSP23	MMC Response Register 2 and 3
0x01C4 0040	0x01E1 B040	MMCRSP45	MMC Response Register 4 and 5
0x01C4 0044	0x01E1 B044	MMCRSP67	MMC Response Register 6 and 7
0x01C4 0048	0x01E1 B048	MMCDRSP	MMC Data Response Register
0x01C4 0050	0x01E1 B050	MMCCIDX	MMC Command Index Register
0x01C4 0064	0x01E1 B064	SDIOCTL	SDIO Control Register
0x01C4 0068	0x01E1 B068	SDIOST0	SDIO Status Register 0
0x01C4 006C	0x01E1 B06C	SDIOIEN	SDIO Interrupt Enable Register
0x01C4 0070	0x01E1 B070	SDIOIST	SDIO Interrupt Status Register
0x01C4 0074	0x01E1 B074	MMCFIFOCTL	MMC FIFO Control Register

6.12.3 MMC/SD Electrical Data/Timing

Table 6-37 through Table 6-38 assume testing over recommended operating conditions.

Table 6-37. Timing Requirements for MMC/SD (see Figure 6-27 and Figure 6-29)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(CMDV-CLKH)}$	Setup time, MMCSD_CMD valid before MMCSD_CLK high	4		4		6		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, MMCSD_CMD valid after MMCSD_CLK high	2.5		2.5		2.5		ns
3	$t_{su(DATV-CLKH)}$	Setup time, MMCSD_DATx valid before MMCSD_CLK high	4.5		5		6		ns
4	$t_{h(CLKH-DATV)}$	Hold time, MMCSD_DATx valid after MMCSD_CLK high	2.5		2.5		2.5		ns

Table 6-38. Switching Characteristics for MMC/SD (see Figure 6-26 through Figure 6-29)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
7	$f_{(CLK)}$	Operating frequency, MMCSD_CLK	0	52	0	50	0	25	MHz
8	$f_{(CLK\_ID)}$	Identification mode frequency, MMCSD_CLK	0	400	0	400	0	400	KHz
9	$t_{W(CLKL)}$	Pulse width, MMCSD_CLK low	6.5		6.5		10		ns
10	$t_{W(CLKH)}$	Pulse width, MMCSD_CLK high	6.5		6.5		10		ns
11	$t_{r(CLK)}$	Rise time, MMCSD_CLK		3		3		10	ns
12	$t_{f(CLK)}$	Fall time, MMCSD_CLK		3		3		10	ns
13	$t_{d(CLKL-CMD)}$	Delay time, MMCSD_CLK low to MMCSD_CMD transition	-4	2.5	-4	3	-4	4	ns
14	$t_{d(CLKL-DAT)}$	Delay time, MMCSD_CLK low to MMCSD_DATx transition	-4	3.3	-4	3.5	-4	4	ns

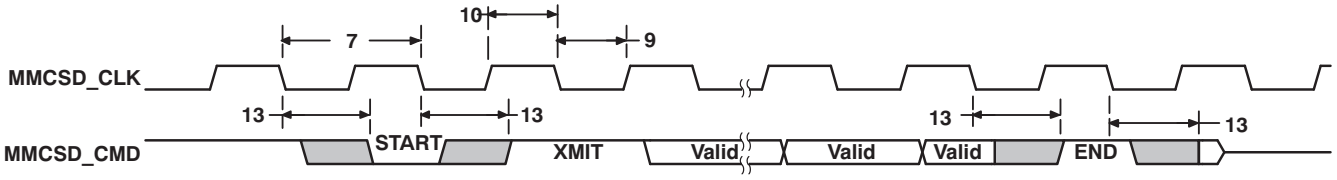

Figure 6-26. MMC/SD Host Command Timing

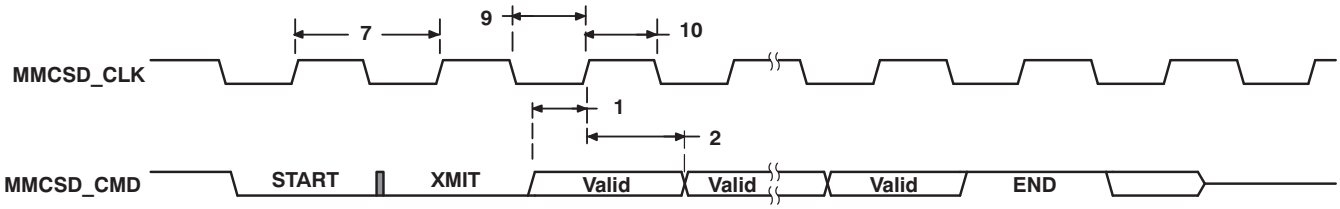

Figure 6-27. MMC/SD Card Response Timing

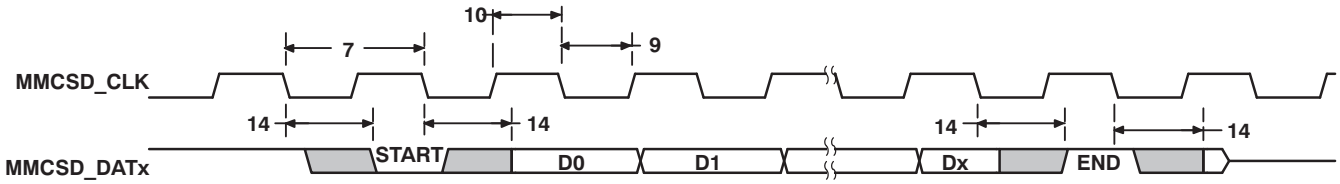

Figure 6-28. MMC/SD Host Write Timing

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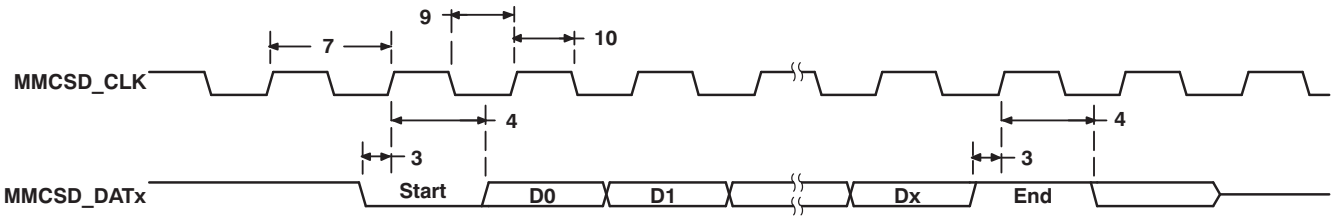

Figure 6-29. MMC/SD Host Read and Card CRC Status Timing

6.13 Serial ATA Controller (SATA)

The Serial ATA Controller (SATA) provides a single HBA port operating in AHCI mode and is used to interface to data storage devices at both 1.5 Gbits/second and 3.0 Gbits/second line speeds. AHCI describes a system memory structure that contains a generic area for control and status, and a table of entries describing a command list where each command list entry contains information necessary to program an SATA device, and a pointer to a descriptor table for transferring data between system memory and the device.

The SATA Controller supports the following features:

- Serial ATA 1.5 Gbps (Gen 1i) and 3 Gbps (Gen 2i) line speeds
- Support for the AHCI controller spec 1.1
- Integrated SERDES PHY
- Integrated Rx and Tx data buffers
- Supports all SATA power management features
- Internal DMA engine per port
- Hardware-assisted native command queuing (NCQ) for up to 32 entries
- 32-bit addressing
- Supports port multiplier with command-based switching
- Activity LED support
- Mechanical presence switch
- Cold presence detect

6.13.1 SATA Register Descriptions

Table 6-39 is a list of the SATA Controller registers.

Table 6-39. SATA Controller Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 8000	CAP	HBA Capabilities Register
0x01E1 8004	GHC	Global HBA Control Register
0x01E1 8008	IS	Interrupt Status Register
0x01E1 800C	PI	Ports Implemented Register
0x01E1 8010	VS	AHCI Version Register
0x01E1 8014	CCC_CTL	Command Completion Coalescing Control Register
0x01E1 8018	CCC_PORTS	Command Completion Coalescing Ports Register
0x01E1 80A0	BISTAFR	BIST Active FIS Register
0x01E1 80A4	BISTCR	BIST Control Register
0x01E1 80A8	BISTFCTR	BIST FIS Count Register
0x01E1 80AC	BISTSR	BIST Status Register
0x01E1 80B0	BISTDECR	BIST DWORD Error Count Register
0x01E1 80E0	TIMER1MS	BIST DWORD Error Count Register
0x01E1 80E8	GPARAM1R	Global Parameter 1 Register
0x01E1 80EC	GPARAM2R	Global Parameter 2 Register
0x01E1 80F0	PPARAMR	Port Parameter Register
0x01E1 80F4	TESTR	Test Register
0x01E1 80F8	VERSIONR	Version Register
0x01E1 80FC	IDR	ID Register
0x01E1 8100	P0CLB	Port Command List Base Address Register
0x01E1 8108	P0FB	Port FIS Base Address Register
0x01E1 8110	P0IS	Port Interrupt Status Register

Table 6-39. SATA Controller Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 8114	P0IE	Port Interrupt Enable Register
0x01E1 8118	P0CMD	Port Command Register
0x01E1 8120	P0TFD	Port Task File Data Register
0x01E1 8124	P0SIG	Port Signature Register
0x01E1 8128	P0SSTS	Port Serial ATA Status Register
0x01E1 812C	P0SCTL	Port Serial ATA Control Register
0x01E1 8130	P0SERR	Port Serial ATA Error Register
0x01E1 8134	P0SACT	Port Serial ATA Active Register
0x01E1 8138	P0CI	Port Command Issue Register
0x01E1 813C	P0SNTF	Port Serial ATA Notification Register
0x01E1 8170	P0DMACR	Port DMA Control Register
0x01E1 8178	P0PHYCR	Port PHY Control Register
0x01E1 817C	P0PHYSR	Port PHY Status Register

6.13.2 SATA Design Considerations

The electrical behavior of the SATA interface conforms to the SATA specification and as such will not be included in this datasheet. A future revision of this datasheet will include design and layout recommendations to meet the SATA specification requirements.

6.14 Multichannel Audio Serial Port (McASP)

The McASP serial port is specifically designed for multichannel audio applications. Its key features are:

- Flexible clock and frame sync generation logic and on-chip dividers
- Up to sixteen transmit or receive data pins and serializers
- Large number of serial data format options, including:
  - TDM Frames with 2 to 32 time slots per frame (periodic) or 1 slot per frame (burst)
  - Time slots of 8,12,16, 20, 24, 28, and 32 bits
  - First bit delay 0, 1, or 2 clocks
  - MSB or LSB first bit order
  - Left- or right-aligned data words within time slots
- DIT Mode with 384-bit Channel Status and 384-bit User Data registers
- Extensive error checking and mute generation logic
- All unused pins GPIO-capable
- Transmit & Receive FIFO Buffers allow the McASP to operate at a higher sample rate by making it more tolerant to DMA latency.
- Dynamic Adjustment of Clock Dividers
  - Clock Divider Value may be changed without resetting the McASP

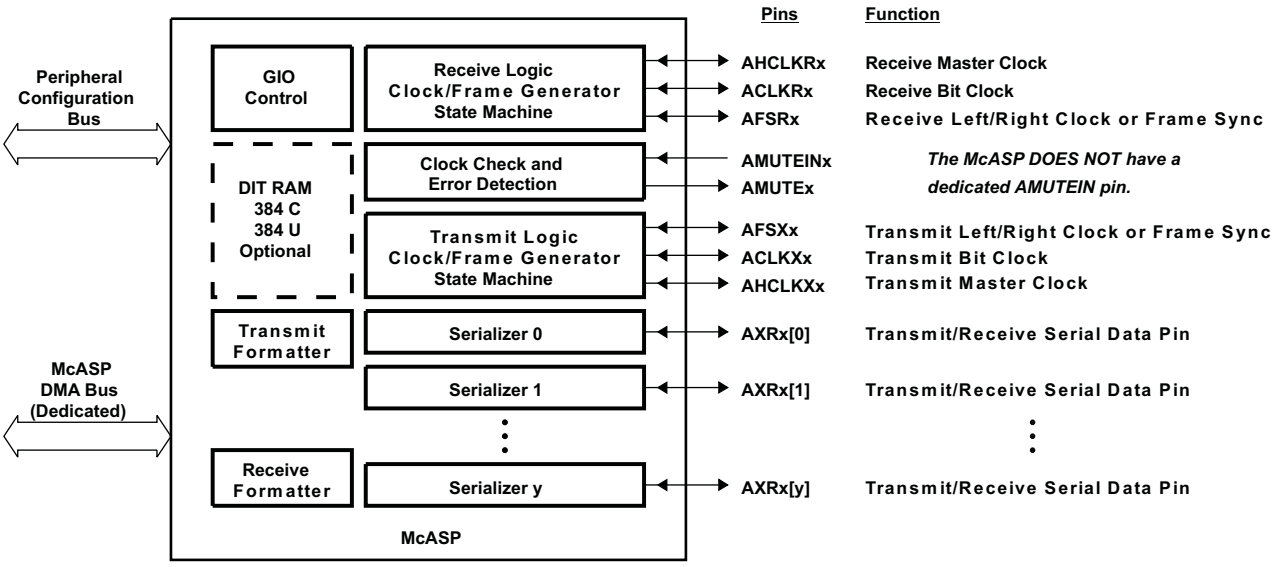

Figure 6-30. McASP Block Diagram

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6.14.1 McASP Peripheral Registers Description(s)

Registers for the McASP are summarized in Table 6-40. The registers are accessed through the peripheral configuration port. The receive buffer registers (RBUF) and transmit buffer registers (XBUF) can also be accessed through the DMA port, as listed in Table 6-41

Registers for the McASP Audio FIFO (AFIFO) are summarized in Table 6-42. Note that the AFIFO Write FIFO (WFIFO) and Read FIFO (RFIFO) have independent control and status registers. The AFIFO control registers are accessed through the peripheral configuration port.

Table 6-40. McASP Registers Accessed Through Peripheral Configuration Port

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01D0 0000	REV	Revision identification register
0x01D0 0010	PFUNC	Pin function register
0x01D0 0014	PDIR	Pin direction register
0x01D0 0018	PDOUT	Pin data output register
0x01D0 001C	PDIN	Read returns: Pin data input register
0x01D0 001C	PDSET	Writes affect: Pin data set register (alternate write address: PDOUT)
0x01D0 0020	PDCLR	Pin data clear register (alternate write address: PDOUT)
0x01D0 0044	GBLCTL	Global control register
0x01D0 0048	AMUTE	Audio mute control register
0x01D0 004C	DLBCTL	Digital loopback control register
0x01D0 0050	DITCTL	DIT mode control register
0x01D0 0060	RGBLCTL	Receiver global control register: Alias of GBLCTL, only receive bits are affected - allows receiver to be reset independently from transmitter
0x01D0 0064	RMASK	Receive format unit bit mask register
0x01D0 0068	RFMT	Receive bit stream format register
0x01D0 006C	AFSRCTL	Receive frame sync control register
0x01D0 0070	ACLKRCTL	Receive clock control register
0x01D0 0074	AHCLKRCTL	Receive high-frequency clock control register
0x01D0 0078	RTDM	Receive TDM time slot 0-31 register
0x01D0 007C	RINTCTL	Receiver interrupt control register
0x01D0 0080	RSTAT	Receiver status register
0x01D0 0084	RSLOT	Current receive TDM time slot register
0x01D0 0088	RCLKCHK	Receive clock check control register
0x01D0 008C	REVTCTL	Receiver DMA event control register
0x01D0 00A0	XGBLCTL	Transmitter global control register. Alias of GBLCTL, only transmit bits are affected - allows transmitter to be reset independently from receiver
0x01D0 00A4	XMASK	Transmit format unit bit mask register
0x01D0 00A8	XFMT	Transmit bit stream format register
0x01D0 00AC	AFSXCTL	Transmit frame sync control register
0x01D0 00B0	ACLKXCTL	Transmit clock control register
0x01D0 00B4	AHCLKXCTL	Transmit high-frequency clock control register
0x01D0 00B8	XTDM	Transmit TDM time slot 0-31 register
0x01D0 00BC	XINTCTL	Transmitter interrupt control register
0x01D0 00C0	XSTAT	Transmitter status register
0x01D0 00C4	XSLOT	Current transmit TDM time slot register
0x01D0 00C8	XCLKCHK	Transmit clock check control register
0x01D0 00CC	XEVTCTL	Transmitter DMA event control register
0x01D0 0100	DITCSRA0	Left (even TDM time slot) channel status register (DIT mode) 0
0x01D0 0104	DITCSRA1	Left (even TDM time slot) channel status register (DIT mode) 1

Table 6-40. McASP Registers Accessed Through Peripheral Configuration Port (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01D0 0108	DITCSRA2	Left (even TDM time slot) channel status register (DIT mode) 2
0x01D0 010C	DITCSRA3	Left (even TDM time slot) channel status register (DIT mode) 3
0x01D0 0110	DITCSRA4	Left (even TDM time slot) channel status register (DIT mode) 4
0x01D0 0114	DITCSRA5	Left (even TDM time slot) channel status register (DIT mode) 5
0x01D0 0118	DITCSRB0	Right (odd TDM time slot) channel status register (DIT mode) 0
0x01D0 011C	DITCSRB1	Right (odd TDM time slot) channel status register (DIT mode) 1
0x01D0 0120	DITCSRB2	Right (odd TDM time slot) channel status register (DIT mode) 2
0x01D0 0124	DITCSRB3	Right (odd TDM time slot) channel status register (DIT mode) 3
0x01D0 0128	DITCSRB4	Right (odd TDM time slot) channel status register (DIT mode) 4
0x01D0 012C	DITCSRB5	Right (odd TDM time slot) channel status register (DIT mode) 5
0x01D0 0130	DITUDRA0	Left (even TDM time slot) channel user data register (DIT mode) 0
0x01D0 0134	DITUDRA1	Left (even TDM time slot) channel user data register (DIT mode) 1
0x01D0 0138	DITUDRA2	Left (even TDM time slot) channel user data register (DIT mode) 2
0x01D0 013C	DITUDRA3	Left (even TDM time slot) channel user data register (DIT mode) 3
0x01D0 0140	DITUDRA4	Left (even TDM time slot) channel user data register (DIT mode) 4
0x01D0 0144	DITUDRA5	Left (even TDM time slot) channel user data register (DIT mode) 5
0x01D0 0148	DITUDRB0	Right (odd TDM time slot) channel user data register (DIT mode) 0
0x01D0 014C	DITUDRB1	Right (odd TDM time slot) channel user data register (DIT mode) 1
0x01D0 0150	DITUDRB2	Right (odd TDM time slot) channel user data register (DIT mode) 2
0x01D0 0154	DITUDRB3	Right (odd TDM time slot) channel user data register (DIT mode) 3
0x01D0 0158	DITUDRB4	Right (odd TDM time slot) channel user data register (DIT mode) 4
0x01D0 015C	DITUDRB5	Right (odd TDM time slot) channel user data register (DIT mode) 5
0x01D0 0180	SRCTL0	Serializer control register 0
0x01D0 0184	SRCTL1	Serializer control register 1
0x01D0 0188	SRCTL2	Serializer control register 2
0x01D0 018C	SRCTL3	Serializer control register 3
0x01D0 0190	SRCTL4	Serializer control register 4
0x01D0 0194	SRCTL5	Serializer control register 5
0x01D0 0198	SRCTL6	Serializer control register 6
0x01D0 019C	SRCTL7	Serializer control register 7
0x01D0 01A0	SRCTL8	Serializer control register 8
0x01D0 01A4	SRCTL9	Serializer control register 9
0x01D0 01A8	SRCTL10	Serializer control register 10
0x01D0 01AC	SRCTL11	Serializer control register 11
0x01D0 01B0	SRCTL12	Serializer control register 12
0x01D0 01B4	SRCTL13	Serializer control register 13
0x01D0 01B8	SRCTL14	Serializer control register 14
0x01D0 01BC	SRCTL15	Serializer control register 15
0x01D0 0200	XBUF0(1)	Transmit buffer register for serializer 0
0x01D0 0204	XBUF1(1)	Transmit buffer register for serializer 1
0x01D0 0208	XBUF2(1)	Transmit buffer register for serializer 2
0x01D0 020C	XBUF3(1)	Transmit buffer register for serializer 3
0x01D0 0210	XBUF4(1)	Transmit buffer register for serializer 4
0x01D0 0214	XBUF5(1)	Transmit buffer register for serializer 5
0x01D0 0218	XBUF6(1)	Transmit buffer register for serializer 6
0x01D0 021C	XBUF7(1)	Transmit buffer register for serializer 7

(1) Writes to XRBUF originate from peripheral configuration port only when XBUSEL = 1 in XFMT.

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Table 6-40. McASP Registers Accessed Through Peripheral Configuration Port (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01D0 0220	XBUF8(1)	Transmit buffer register for serializer 8
0x01D0 0224	XBUF9(1)	Transmit buffer register for serializer 9
0x01D0 0228	XBUF10(1)	Transmit buffer register for serializer 10
0x01D0 022C	XBUF11(1)	Transmit buffer register for serializer 11
0x01D0 0230	XBUF12(1)	Transmit buffer register for serializer 12
0x01D0 0234	XBUF13(1)	Transmit buffer register for serializer 13
0x01D0 0238	XBUF14(1)	Transmit buffer register for serializer 14
0x01D0 023C	XBUF15(1)	Transmit buffer register for serializer 15
0x01D0 0280	RBUF0(2)	Receive buffer register for serializer 0
0x01D0 0284	RBUF1(2)	Receive buffer register for serializer 1
0x01D0 0288	RBUF2(2)	Receive buffer register for serializer 2
0x01D0 028C	RBUF3(2)	Receive buffer register for serializer 3
0x01D0 0290	RBUF4(2)	Receive buffer register for serializer 4
0x01D0 0294	RBUF5(2)	Receive buffer register for serializer 5
0x01D0 0298	RBUF6(2)	Receive buffer register for serializer 6
0x01D0 029C	RBUF7(2)	Receive buffer register for serializer 7
0x01D0 02A0	RBUF8(2)	Receive buffer register for serializer 8
0x01D0 02A4	RBUF9(2)	Receive buffer register for serializer 9
0x01D0 02A8	RBUF10(2)	Receive buffer register for serializer 10
0x01D0 02AC	RBUF11(2)	Receive buffer register for serializer 11
0x01D0 02B0	RBUF12(2)	Receive buffer register for serializer 12
0x01D0 02B4	RBUF13(2)	Receive buffer register for serializer 13
0x01D0 02B8	RBUF14(2)	Receive buffer register for serializer 14
0x01D0 02BC	RBUF15(2)	Receive buffer register for serializer 15

(2) Reads from XRBUF originate on peripheral configuration port only when RBUSEL = 1 in RFMT.

Table 6-41. McASP Registers Accessed Through DMA Port

ACCESS TYPE	BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
Read Accesses	0x01D0 2000	RBUF	Receive buffer DMA port address. Cycles through receive serializers, skipping over transmit serializers and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Reads from DMA port only if XBUSEL = 0 in XFMT.
Write Accesses	0x01D0 2000	XBUF	Transmit buffer DMA port address. Cycles through transmit serializers, skipping over receive and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Writes to DMA port only if RBUSEL = 0 in RFMT.

Table 6-42. McASP AFIFO Registers Accessed Through Peripheral Configuration Port

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01D0 1000	AFIFOREV	AFIFO revision identification register
0x01D0 1010	WFIFOCTL	Write FIFO control register
0x01D0 1014	WFIFOSTS	Write FIFO status register
0x01D0 1018	RFIFOCTL	Read FIFO control register
0x01D0 101C	RFIFOSTS	Read FIFO status register

6.14.2 McASP Electrical Data/Timing

6.14.2.1 Multichannel Audio Serial Port 0 (McASP0) Timing

Table 6-43 and Table 6-45 assume testing over recommended operating conditions (see Figure 6-31 and Figure 6-32).

Table 6-43. Timing Requirements for McASP0 (1.2V, 1.1V)(1)(2)

NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		22		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		10		11		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	AHCLKR/X ext	20(3)		22(3)		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/W high or low	AHCLKR/X ext	10		11		ns
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, AFSR/X input to ACLKR/X (4)	AHCLKR/X int	11.5		12		ns
			AHCLKR/X ext input	4		5		ns
			AHCLKR/X ext output	4		5		ns
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, AFSR/X input after ACLKR/X(4)	AHCLKR/X int	-1		-2		ns
			AHCLKR/X ext input	0.4		1		ns
			AHCLKR/X ext output	0.4		1		ns
7	$t_{su(AXR-ACLKRX)}$	Setup time, AXR0[n] input to ACLKR/X(4)(5)	AHCLKR/X int	11.5		12		ns
			AHCLKR/X ext	4		5		ns
8	$t_{h(ACLKRX-AXR)}$	Hold time, AXR0[n] input after ACLKR/X(4)(5)	AHCLKR/X int	-1		-2		ns
			AHCLKR/X ext input	0.4		1		ns
			AHCLKR/X ext output	0.4		1		ns

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0

Table 6-44. Timing Requirements for McASP0 (1.0V)(1)(2)

NO.	PARAMETER			1.0V MIN	1.0V MAX	UNIT
1	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		26.6		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		13.3		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	AHCLKR/X ext	26.6(3)		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/W high or low	AHCLKR/X ext	13.3		ns
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, AFSR/X input to ACLKR/X (4)	AHCLKR/X int	16		ns
			AHCLKR/X ext input	5.5		ns
			AHCLKR/X ext output	5.5		ns
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, AFSR/X input after ACLKR/X(4)	AHCLKR/X int	-2		ns
			AHCLKR/X ext input	1		ns
			AHCLKR/X ext output	1		ns
7	$t_{su(AXR-ACLKRX)}$	Setup time, AXR0[n] input to ACLKR/X(4)(5)	AHCLKR/X int	16		ns
			AHCLKR/X ext	5.5		ns
8	$t_{h(ACLKRX-AXR)}$	Hold time, AXR0[n] input after ACLKR/X(4)(5)	AHCLKR/X int	-2		ns
			AHCLKR/X ext input	1		ns
			AHCLKR/X ext output	1		ns

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0

Table 6-45. Switching Characteristics for McASP0 (1.2V, 1.1V)(1)

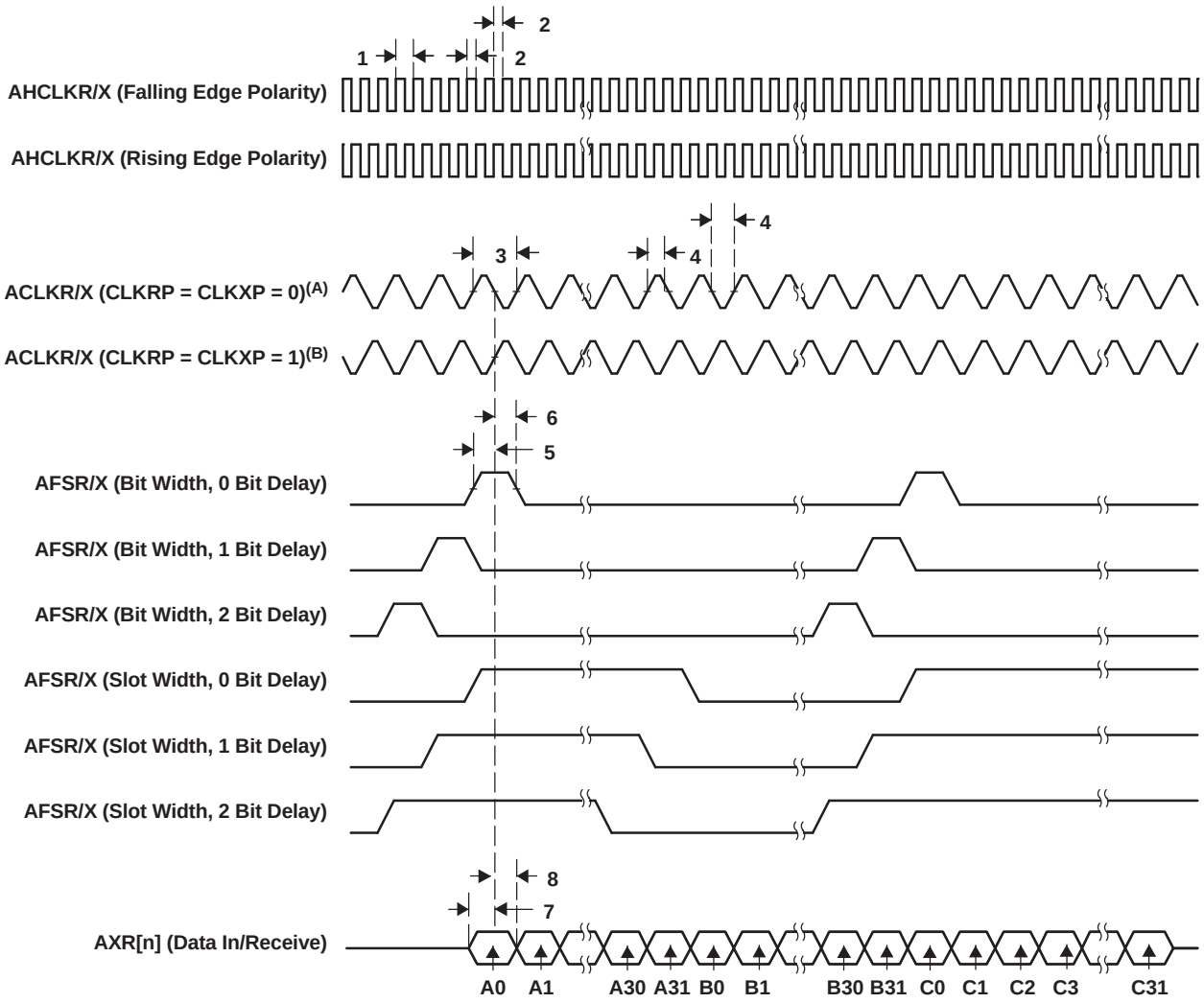
NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
9	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		20		22		ns
10	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		AH – 2.5(2)		AH – 2.5(2)		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	ACLKR/X int	20(3)(4)		22(3)(4)		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X int	A – 2.5(5)		A – 2.5(5)		ns
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid(6)	ACLKR/X int	0	6	0	8	ns
			ACLKR/X ext input	2	13.5	2	14.5	ns
			ACLKR/X ext output	2	13.5	2	14.5	ns
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX transmit edge to AXR output valid	ACLKR/X int	0	6	0	8	ns
			ACLKR/X ext input	2	13.5	2	14.5	ns
			ACLKR/X ext output	2	13.5	2	14.5	ns
15	$t_{dis(ACLKX-AXRHZ)}$	Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit	ACLKR/X int	0	6	0	8	ns
			ACLKR/X ext	2	13.5	2	14.5	ns

(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

Table 6-46. Switching Characteristics for McASP0 (1.0V)(1)

NO.	PARAMETER			1.0V		UNIT
				MIN	MAX	
9	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR/X		26.6		ns
10	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR/X high or low		AH – 2.5(2)		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	ACLKR/X int	26.6(3)(4)		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X int	A – 2.5(5)		ns
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid(6)	ACLKR/X int	0	10	ns
			ACLKR/X ext input	2	19	ns
			ACLKR/X ext output	2	19	ns
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX transmit edge to AXR output valid	ACLKR/X int	0	10	ns
			ACLKR/X ext input	2	19	ns
			ACLKR/X ext output	2	19	ns
15	$t_{dis(ACLKX-AXRHZ)}$	Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit	ACLKR/X int	0	10	ns
			ACLKR/X ext	2	19	ns

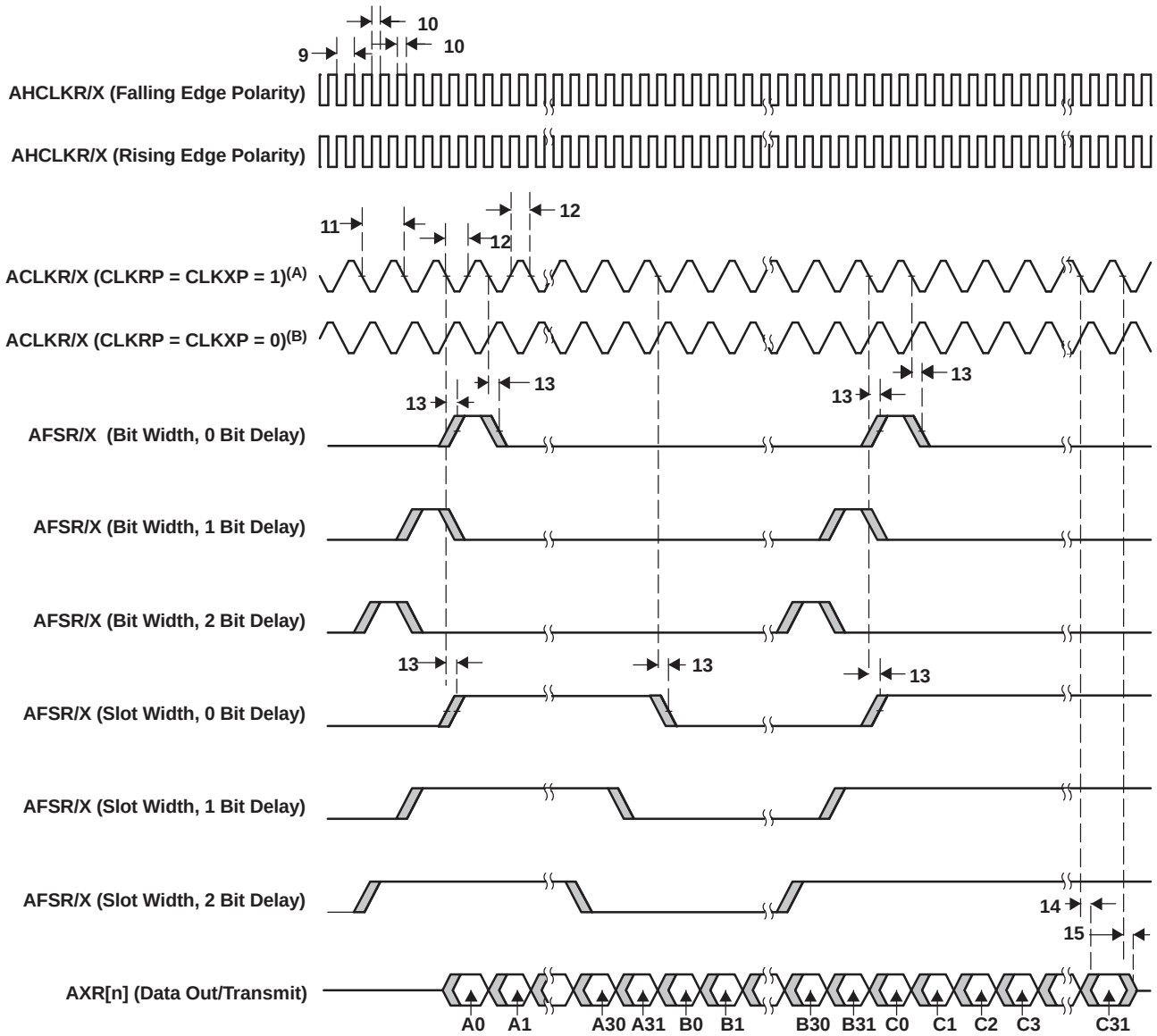
(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 6-31. McASP Input Timings



A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 6-32. McASP Output Timings

PRODUCT PREVIEW

6.15 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Transmit & Receive FIFO Buffers allow the McBSP to operate at a higher sample rate by making it more tolerant to DMA latency

If internal clock source is used, the CLKGDV field of the Sample Rate Generator Register (SRGR) must always be set to a value of 1 or greater.

6.15.1 McBSP Peripheral Register Description(s)

Table 6-47. McBSP/FIFO Registers

McBSP0 BYTE ADDRESS	McBSP1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
McBSP Registers			
0x01D1 0000	0x01D1 1000	DRR	McBSP Data Receive Register (read-only)
0x01D1 0004	0x01D1 1004	DXR	McBSP Data Transmit Register
0x01D1 0008	0x01D1 1008	SPCR	McBSP Serial Port Control Register
0x01D1 000C	0x01D1 100C	RCR	McBSP Receive Control Register
0x01D1 0010	0x01D1 1010	XCR	McBSP Transmit Control Register
0x01D1 0014	0x01D1 1014	SRGR	McBSP Sample Rate Generator register
0x01D1 0018	0x01D1 1018	MCR	McBSP Multichannel Control Register
0x01D1 001C	0x01D1 101C	RCERE0	McBSP Enhanced Receive Channel Enable Register 0 Partition A/B
0x01D1 0020	0x01D1 1020	XCERE0	McBSP Enhanced Transmit Channel Enable Register 0 Partition A/B
0x01D1 0024	0x01D1 1024	PCR	McBSP Pin Control Register
0x01D1 0028	0x01D1 1028	RCERE1	McBSP Enhanced Receive Channel Enable Register 1 Partition C/D
0x01D1 002C	0x01D1 102C	XCERE1	McBSP Enhanced Transmit Channel Enable Register 1 Partition C/D
0x01D1 0030	0x01D1 1030	RCERE2	McBSP Enhanced Receive Channel Enable Register 2 Partition E/F
0x01D1 0034	0x01D1 1034	XCERE2	McBSP Enhanced Transmit Channel Enable Register 2 Partition E/F
0x01D1 0038	0x01D1 1038	RCERE3	McBSP Enhanced Receive Channel Enable Register 3 Partition G/H
0x01D1 003C	0x01D1 103C	XCERE3	McBSP Enhanced Transmit Channel Enable Register 3 Partition G/H
McBSP FIFO Control and Status Registers			
0x01D1 0800	0x01D1 1800	BFIFOREV	BFIFO Revision Identification Register
0x01D1 0810	0x01D1 1810	WFIFOCTL	Write FIFO Control Register
0x01D1 0814	0x01D1 1814	WFIFOSTS	Write FIFO Status Register
0x01D1 0818	0x01D1 1818	RFIFOCTL	Read FIFO Control Register
0x01D1 081C	0x01D1 181C	RFIFOSTS	Read FIFO Status Register
McBSP FIFO Data Registers			
0x01F1 0000	0x01F1 1000	RBUF	McBSP FIFO Receive Buffer
0x01F1 0000	0x01F1 1000	XBUF	McBSP FIFO Transmit Buffer

6.15.2 McBSP Electrical Data/Timing

The following assume testing over recommended operating conditions.

6.15.2.1 Multichannel Buffered Serial Port (McBSP) Timing

Table 6-48. Timing Requirements for McBSP0 [1.2V, 1.1V](1) (see Figure 6-33)

NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P or 20(2)(3)		2P or 25(2)(3)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P - 1(4)		P - 1(4)		ns
4	t_t	Transition time, rising edge or falling edge			5		5	
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	14		15.5		ns
			CLKR ext	4		5		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		6		ns
			CLKR ext	3		3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	14		15.5		ns
			CLKR ext	4		5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		3		ns
			CLKR ext	3		3		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	14		15.5		ns
			CLKX ext	4		5		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		6		ns
			CLKX ext	3		3		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 6-49. Timing Requirements for McBSP0 [1.0V](1) (see Figure 6-33)

NO.	PARAMETER			1.0V MIN	1.0V MAX	UNIT
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P or 26.6(2)(3)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P - 1(4)		ns
4	t_t	Transition time, rising edge or falling edge			5	
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	20		ns
			CLKR ext	5		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	20		ns
			CLKR ext	5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	3		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	20		ns
			CLKX ext	5		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 6-50. Switching Characteristics for McBSP0 [1.2V, 1.1V](1)(2)
(see Figure 6-33)

NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		2	14.5	2	16	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P or 20(3)(4)(5)		2P or 25(3)(4)(5)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 2(6)	C + 2(6)	C - 2(6)	C + 2(6)	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-4	5.5	-4	5.5	ns
			CLKR ext	2	14.5	2	16	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-4	5.5	-4	5.5	ns
			CLKX ext	2	14.5	2	16	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-4	7.5	-5.5	7.5	ns
			CLKX ext	-2	16	-22	16	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-4 + D1(7)	5.5 + D2(7)	-4 + D1(7)	5.5 + D2(7)	ns
			CLKX ext	2 + D1(7)	14.5 + D2(7)	2 + D1(7)	16 + D2(7)	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-4(8)	5(8)	-4(8)	5(8)	ns
			FSX ext	-2(8)	14.5(8)	-2(8)	16(8)	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

Table 6-51. Switching Characteristics for McBSP0 [1.0V](1)(2) (see Figure 6-33)

NO.	PARAMETER			1.0V MIN	1.0V MAX	UNIT
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		3	21.5	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P or 26.6(3)(4)(5)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 2(6)	C + 2(6)	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-4	10	ns
			CLKR ext	2.5	21.5	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-4	10	ns
			CLKX ext	2.5	21.5	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-4	10	ns
			CLKX ext	-2	21.5	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-4 + D1(7)	10 + D2(7)	ns
			CLKX ext	2.5 + D1(7)	21.5 + D2(7)	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-4(8)	5(8)	ns
			FSX ext	-2(8)	21.5(8)	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

Table 6-52. Timing Requirements for McBSP1 [1.2V, 1.1V](1) (see Figure 6-33)

NO.	PARAMETER			1.2V MIN	1.2V MAX	1.1V MIN	1.1V MAX	UNIT
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P or 20(2)(3)		2P or 25(2)(4)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P - 1(5)		P - 1(6)		ns
4	t_t	Transition time, rising edge or falling edge			5		5	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(5) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.
(6) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 6-52. Timing Requirements for McBSP1 [1.2V, 1.1V] (see Figure 6-33) (continued)

NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	15		18		ns
			CLKR ext	5		5		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		6		ns
			CLKR ext	3		3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	15		18		ns
			CLKR ext	5		5		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		3		ns
			CLKR ext	3		3		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	15		18		ns
			CLKX ext	5		5		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		6		ns
			CLKX ext	3		3		

Table 6-53. Timing Requirements for McBSP1 [1.0V](1) (see Figure 6-33)

NO.	PARAMETER			1.0V		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P or 26.6(2)(3)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P - 1(4)		ns
4	t_t	Transition time, rising edge or falling edge			5	
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	21		ns
			CLKR ext	10		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	21		ns
			CLKR ext	10		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	3		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	21		ns
			CLKX ext	10		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

Table 6-54. Switching Characteristics for McBSP1 [1.2V, 1.1V](1)(2)
(see Figure 6-33)

NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		2.5	16.5	3	18	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P or 20(3)(4)(5)		2P or 25(3)(4)(5)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 2(6)	C + 2(6)	C - 2(6)	C + 2(6)	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-4	6.5	-4	13	ns
			CLKR ext	2.5	16.5	2.5	18	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-4	6.5	-4	13	ns
			CLKX ext	2.5	16.5	2.5	18	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-4	6.5	-4	13	ns
			CLKX ext	-2	16.5	-2	18	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-4 + D1(7)	6.5 + D2(7)	-4 + D1(7)	13 + D2(7)	ns
			CLKX ext	2.5 + D1(7)	16.5 + D2(7)	2.5 + D1(7)	18 + D2(7)	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-4(8)	6.5(8)	-4(8)	13(8)	ns
			FSX ext	-2(8)	16.5(8)	-2(8)	18(9)	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(9) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

Table 6-55. Switching Characteristics for McBSP1 [1.0V](1)(2)
(see Figure 6-33)

NO.	PARAMETER			1.0V		UNIT
				MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		3	23	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P or 26.6(3)(4)(5)		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 2(6)	C + 2(6)	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	-4	13	ns
			CLKR ext	2.5	23	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-4	13	ns
			CLKX ext	2.5	23	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	-4	13	ns
			CLKX ext	-2	23	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-4 + D1(7)	13 + D2(8)	ns
			CLKX ext	2.5 + D1(8)	23 + D2(8)	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	-4(9)	13(9)	ns
			FSX ext	-2(9)	23(9)	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(9) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

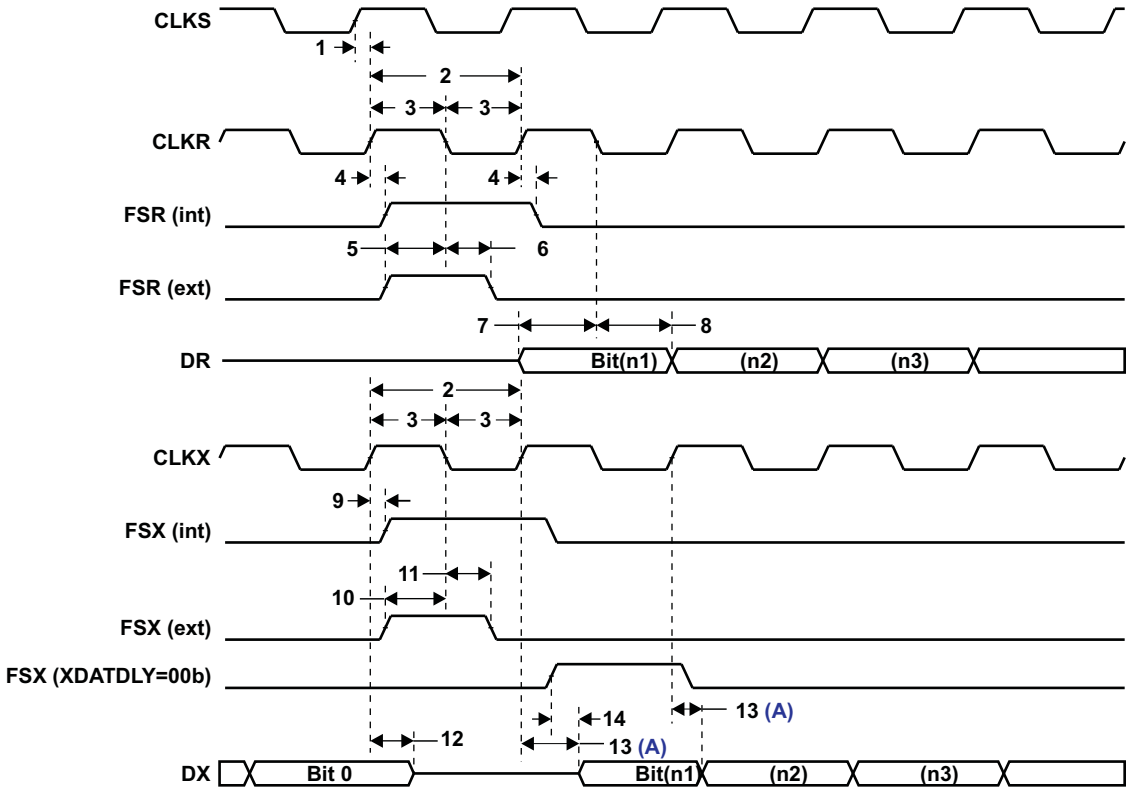


Figure 6-33. McBSP Timing(B)

Table 6-56. Timing Requirements for McBSP0 FSR When GSYNC = 1 (see Figure 6-34)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	4		4.5		5		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		4		4		ns

Table 6-57. Timing Requirements for McBSP1 FSR When GSYNC = 1 (see Figure 6-34)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	5		5		10		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		4		4		ns

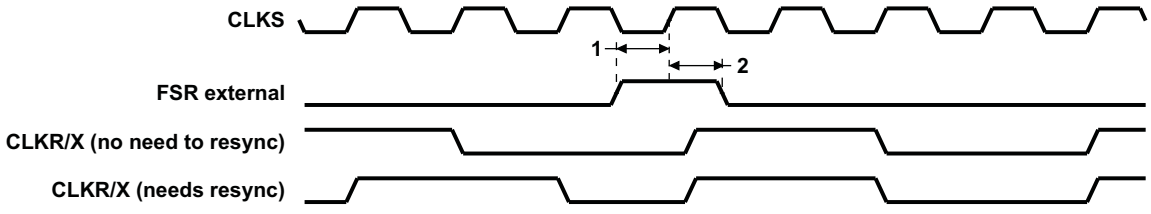


Figure 6-34. FSR Timing When GSYNC = 1

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6.16 Serial Peripheral Interface Ports (SPI0, SPI1)

Figure 6-35 is a block diagram of the SPI module, which is a simple shift register and buffer plus control logic. Data is written to the shift register before transmission occurs and is read from the buffer at the end of transmission. The SPI can operate either as a master, in which case, it initiates a transfer and drives the SPIx_CLK pin, or as a slave. Four clock phase and polarity options are supported as well as many data formatting options.

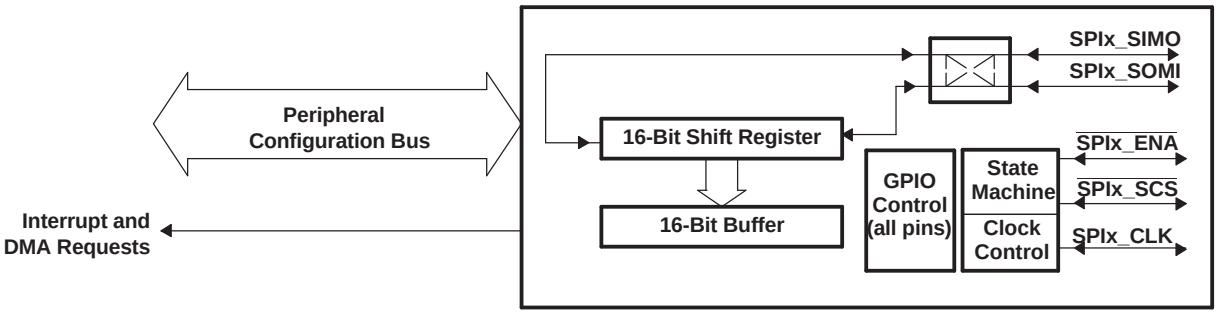

Figure 6-35. Block Diagram of SPI Module

The SPI supports 3-, 4-, and 5-pin operation with three basic pins (SPIx_CLK, SPIx_SIMO, and SPIx_SOMI) and two optional pins ($\overline{\text{SPIx\_SCS}}$, $\overline{\text{SPIx\_ENA}}$).

The optional $\overline{\text{SPIx\_SCS}}$ (Slave Chip Select) pin is most useful to enable in slave mode when there are other slave devices on the same SPI port. The device will only shift data and drive the SPIx_SOMI pin when $\overline{\text{SPIx\_SCS}}$ is held low.

In slave mode, $\overline{\text{SPIx\_ENA}}$ is an optional output and can be driven in either a push-pull or open-drain manner. The $\overline{\text{SPIx\_ENA}}$ output provides the status of the internal transmit buffer (SPIDAT0/1 registers). In four-pin mode with the enable option, $\overline{\text{SPIx\_ENA}}$ is asserted only when the transmit buffer is full, indicating that the slave is ready to begin another transfer. In five-pin mode, the $\overline{\text{SPIx\_ENA}}$ is additionally qualified by $\overline{\text{SPIx\_SCS}}$ being asserted. This allows a single handshake line to be shared by multiple slaves on the same SPI bus.

In master mode, the $\overline{\text{SPIx\_ENA}}$ pin is an optional input and the master can be configured to delay the start of the next transfer until the slave asserts $\overline{\text{SPIx\_ENA}}$. The addition of this handshake signal simplifies SPI communications and, on average, increases SPI bus throughput since the master does not need to delay each transfer long enough to allow for the worst-case latency of the slave device. Instead, each transfer can begin as soon as both the master and slave have actually serviced the previous SPI transfer.

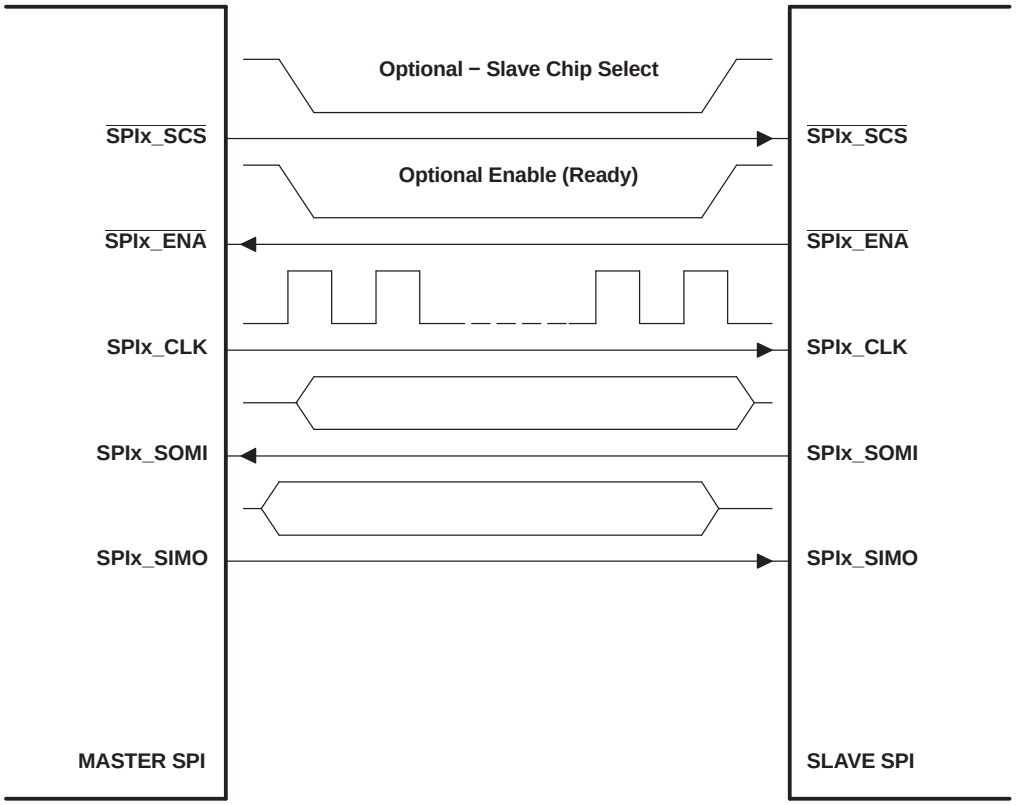

Figure 6-36. Illustration of SPI Master-to-SPI Slave Connection

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6.16.1 SPI Peripheral Registers Description(s)

Table 6-58 is a list of the SPI registers.

Table 6-58. SPIx Configuration Registers

SPI0 BYTE ADDRESS	SPI1 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01C4 1000	0x01F0 E000	SPIGCR0	Global Control Register 0
0x01C4 1004	0x01F0 E004	SPIGCR1	Global Control Register 1
0x01C4 1008	0x01F0 E008	SPIINT0	Interrupt Register
0x01C4 100C	0x01F0 E00C	SPILVL	Interrupt Level Register
0x01C4 1010	0x01F0 E010	SPIFLG	Flag Register
0x01C4 1014	0x01F0 E014	SPIPC0	Pin Control Register 0 (Pin Function)
0x01C4 1018	0x01F0 E018	SPIPC1	Pin Control Register 1 (Pin Direction)
0x01C4 101C	0x01F0 E01C	SPIPC2	Pin Control Register 2 (Pin Data In)
0x01C4 1020	0x01F0 E020	SPIPC3	Pin Control Register 3 (Pin Data Out)
0x01C4 1024	0x01F0 E024	SPIPC4	Pin Control Register 4 (Pin Data Set)
0x01C4 1028	0x01F0 E028	SPIPC5	Pin Control Register 5 (Pin Data Clear)
0x01C4 102C	0x01F0 E02C	Reserved	Reserved - Do not write to this register
0x01C4 1030	0x01F0 E030	Reserved	Reserved - Do not write to this register
0x01C4 1034	0x01F0 E034	Reserved	Reserved - Do not write to this register
0x01C4 1038	0x01F0 E038	SPIDAT0	Shift Register 0 (without format select)
0x01C4 103C	0x01F0 E03C	SPIDAT1	Shift Register 1 (with format select)
0x01C4 1040	0x01F0 E040	SPIBUF	Buffer Register
0x01C4 1044	0x01F0 E044	SPIEMU	Emulation Register
0x01C4 1048	0x01F0 E048	SPIDELAY	Delay Register
0x01C4 104C	0x01F0 E04C	SPIDEF	Default Chip Select Register
0x01C4 1050	0x01F0 E050	SPIFMT0	Format Register 0
0x01C4 1054	0x01F0 E054	SPIFMT1	Format Register 1
0x01C4 1058	0x01F0 E058	SPIFMT2	Format Register 2
0x01C4 105C	0x01F0 E05C	SPIFMT3	Format Register 3
0x01C4 1060	0x01F0 E060	INTVEC0	Interrupt Vector for SPI INT0
0x01C4 1064	0x01F0 E064	INTVEC1	Interrupt Vector for SPI INT1

6.16.2 SPI Electrical Data/Timing

6.16.2.1 Serial Peripheral Interface (SPI) Timing

Table 6-59 through Table 6-74 assume testing over recommended operating conditions (see Figure 6-37 through Figure 6-40).

Table 6-59. General Timing Requirements for SPI0 Master Modes(1)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle Time, SPI0_CLK, All Master Modes		20(2)	256P	30(2)	256P	40(2)	256P	ns
2	$t_{w(SPCH)M}$	Pulse Width High, SPI0_CLK, All Master Modes		0.5M-1		0.5M-1		0.5M-1		ns
3	$t_{w(SPCL)M}$	Pulse Width Low, SPI0_CLK, All Master Modes		0.5M-1		0.5M-1		0.5M-1		ns
4	$t_{d(SIMO\_SPC)M}$	Delay, initial data bit valid on SPI0_SIMO after initial edge on SPI0_CLK(3)	Polarity = 0, Phase = 0, to SPI0_CLK rising		5		5		6	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		-0.5M+5		-0.5M+5		-0.5M+6	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		5		5		6	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		-0.5M+5		-0.5M+5		-0.5M+6	
5	$t_{d(SPC\_SIMO)M}$	Delay, subsequent bits valid on SPI0_SIMO after transmit edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK rising		5		5		6	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		5		5		6	
			Polarity = 1, Phase = 0, from SPI0_CLK falling		5		5		6	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		5		5		6	
6	$t_{oh(SPC\_SIMO)M}$	Output hold time, SPI0_SIMO valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5M-3		0.5M-3		0.5M-3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	0.5M-3		0.5M-3		0.5M-3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5M-3		0.5M-3		0.5M-3		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	0.5M-3		0.5M-3		0.5M-3		
7	$t_{su(SOMI\_SPC)M}$	Input Setup Time, SPI0_SOMI valid before receive edge of SPI0_CLK	Polarity = 0, Phase = 0, to SPI0_CLK falling	1.5		1.5		1.5		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 0, to SPI0_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	1.5		1.5		1.5		

(1) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(2) This timing is limited by the timing shown or 2P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI0_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI0_SOMI.

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Table 6-59. General Timing Requirements for SPI0 Master Modes (continued)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
8	$t_{ih(SPC\_SOMI)M}$	Input Hold Time, SPI0_SOMI valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	4		4		5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	4		4		5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	4		4		5		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	4		4		5		

Table 6-60. General Timing Requirements for SPI0 Slave Modes(1)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
9	$t_{c(SPC)S}$	Cycle Time, SPI0_CLK, All Slave Modes		40(2)	256P	50(2)	256P	60(2)	256P	ns
10	$t_{w(SPCH)S}$	Pulse Width High, SPI0_CLK, All Slave Modes		18		22		27		ns
11	$t_{w(SPCL)S}$	Pulse Width Low, SPI0_CLK, All Slave Modes		18		22		27		ns
12	$t_{su(SOMI\_SPC)S}$	Setup time, transmit data written to SPI before initial clock edge from master.(3)(4)	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P		2P		2P		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	2P		2P		2P		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P		2P		2P		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	2P		2P		2P		
13	$t_{d(SPC\_SOMI)S}$	Delay, subsequent bits valid on SPI0_SOMI after transmit edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK rising		17		20		27	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		17		20		27	
			Polarity = 1, Phase = 0, from SPI0_CLK falling		17		20		27	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		17		20		27	
14	$t_{oh(SPC\_SOMI)S}$	Output hold time, SPI0_SOMI valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5S-6		0.5S-16		0.5S-20		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	0.5S-6		0.5S-16		0.5S-20		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5S-6		0.5S-16		0.5S-20		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	0.5S-6		0.5S-16		0.5S-20		
15	$t_{su(SIMO\_SPC)S}$	Input Setup Time, SPI0_SIMO valid before receive edge of SPI0_CLK	Polarity = 0, Phase = 0, to SPI0_CLK falling	1.5		1.5		1.5		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 0, to SPI0_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	1.5		1.5		1.5		

(1) P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period)
(2) This timing is limited by the timing shown or 2P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI0_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI0_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the DSP CPU.

Table 6-60. General Timing Requirements for SPI0 Slave Modes (continued)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
16	$t_{ih(SPC\_SIMO)S}$	Input Hold Time, SPI0_SIMO valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	4		4		5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	4		4		5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	4		4		5		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	4		4		5		

Table 6-61. Additional SPI0 Master Timings, 4-Pin Enable Option [1][2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
17	$t_{d(ENA\_SPC)M}$	Delay from slave assertion of $\overline{\text{SPI0\_ENA}}$ active to first SPI0_CLK from master.[4]	Polarity = 0, Phase = 0, to SPI0_CLK rising		3P+5		3P+5		3P+6	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		3P+5		3P+5		3P+6	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert $\overline{\text{SPI0\_ENA}}$ after final SPI0_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPI0_CLK falling		0.5M+P+5		0.5M+P+5		0.5M+P+6	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		P+5		P+5		P+6	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		0.5M+P+5		0.5M+P+5		0.5M+P+6	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		P+5		P+5		P+6	

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-59).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{\text{SPI0\_ENA}}$ assertion.
(5) In the case where the master SPI is ready with new data before $\overline{\text{SPI0\_EN A}}$ deassertion.

Table 6-62. Additional SPI0 Master Timings, 4-Pin Chip Select Option (1)(2)(3)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
19	$t_{d(SCS\_SPC)M}$	Delay from $\overline{\text{SPI0\_SCS}}$ active to first SPI0_CLK (4)(5)	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P-1		2P-2		2P-3		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	0.5M+2P-1		0.5M+2P-2		0.5M+2P-3		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P-1		2P-2		2P-3		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	0.5M+2P-1		0.5M+2P-2		0.5M+2P-3		
20	$t_{d(SPC\_SCS)M}$	Delay from final SPI0_CLK edge to master deasserting $\overline{\text{SPI0\_SCS}}$ (6)(7)	Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5M+P-1		0.5M+P-2		0.5M+P-3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	P-1		P-2		P-3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5M+P-1		0.5M+P-2		0.5M+P-3		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	P-1		P-2		P-3		

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-59).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{\text{SPI0\_SCS}}$ assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, $\overline{\text{SPI0\_SCS}}$ will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

Table 6-63. Additional SPI0 Master Timings, 5-Pin Option (1)(2)(3)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert SPI0_ENA after final SPI0_CLK edge to ensure master does not begin the next transfer.(4)	Polarity = 0, Phase = 0, from SPI0_CLK falling		0.5M+P+5		0.5M+P+5		0.5M+P+6	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		P+5		P+5		P+6	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		0.5M+P+5		0.5M+P+5		0.5M+P+6	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		P+5		P+5		P+6	
20	$t_{d(SPC\_SCS)M}$	Delay from final SPI0_CLK edge to master deasserting SPI0_SCS (5)(6)	Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5M+P-2		0.5M+P-2		0.5M+P-3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	P-2		P-2		P-3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5M+P-2		0.5M+P-2		0.5M+P-3		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	P-2		P-2		P-3		
21	$t_{d(SCSL\_ENAL)M}$	Max delay for slave SPI to drive SPI0_ENA valid after master asserts SPI0_SCS to delay the master from beginning the next transfer,			C2TDELAY+P		C2TDELAY+P		C2TDELAY+P	ns
22	$t_{d(SCS\_SPC)M}$	Delay from SPI0_SCS active to first SPI0_CLK(7)(8)(9)	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P-2		2P-2		2P-3		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	0.5M+2P-2		0.5M+2P-2		0.5M+2P-3		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P-2		2P-2		2P-3		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	0.5M+2P-2		0.5M+2P-2		0.5M+2P-3		

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-60).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI0_ENA deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI0_SCS will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(7) If SPI0_ENA is asserted immediately such that the transmission is not delayed by SPI0_ENA.
(8) In the case where the master SPI is ready with new data before SPI0_SCS assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].

Table 6-63. Additional SPI0 Master Timings, 5-Pin Option (continued)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
23	$t_{d(ENA\_SPC)M}$	Delay from assertion of $\overline{SPI0\_ENA}$ low to first SPI0_CLK edge.(10)	Polarity = 0, Phase = 0, to SPI0_CLK rising		3P+5		3P+5		3P+6	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		3P+5		3P+5		3P+6	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	

(10) If $\overline{SPI0\_ENA}$ was initially deasserted high and SPI0_CLK is delayed.

Table 6-64. Additional SPI0 Slave Timings, 4-Pin Enable Option [1][2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
24	$t_{d(SPC\_ENAH)S}$	Delay from final SPI0_CLK edge to slave deasserting SPI0_ENA.	Polarity = 0, Phase = 0, from SPI0_CLK falling	1.5P-3	2.5P+17.5	1.5P-3	2.5P+20	1.5P-3	2.5P+27	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	– 0.5M+1.5P-3	– 0.5M+2.5P+17.5	– 0.5M+1.5P-3	– 0.5M+2.5P+20	– 0.5M+1.5P-3	– 0.5M+2.5P+27	
			Polarity = 1, Phase = 0, from SPI0_CLK rising	1.5P-3	2.5P+17.5	1.5P-3	2.5P+20	1.5P-3	2.5P+27	
			Polarity = 1, Phase = 1, from SPI0_CLK rising	– 0.5M+1.5P-3	– 0.5+2.5P+17.5	– 0.5M+1.5P-3	– 0.5+2.5P+20	– 0.5M+1.5P-3	– 0.5+2.5P+27	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-60).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 6-65. Additional SPI0 Slave Timings, 4-Pin Chip Select Option (1)(2)(3)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{SPI0\_SCS}$ asserted at slave to first SPI0_CLK edge at slave.	P + 1.5		P + 1.5		P + 1.5		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final SPI0_CLK edge before $\overline{SPI0\_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5M+P+4		0.5M+P+4		0.5M+P+5		ns
		Polarity = 0, Phase = 1, from SPI0_CLK falling	P+4		P+4		P+5		
		Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5M+P+4		0.5M+P+4		0.5M+P+5		
		Polarity = 1, Phase = 1, from SPI0_CLK rising	P+4		P+4		P+5		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{SPI0\_SCS}$ to slave driving SPI0_SOMI valid		P+17.5		P+20		P+27	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{SPI0\_SCS}$ to slave 3-stating SPI0_SOMI		P+17.5		P+20		P+27	ns

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-60).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 6-66. Additional SPI0 Slave Timings, 5-Pin Option (1)(2)(3)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{SPI0\_SCS}$ asserted at slave to first SPI0_CLK edge at slave.		P + 1.5		P + 1.5		P + 1.5		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final SPI0_CLK edge before $\overline{SPI0\_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI0_CLK falling	0.5M+P +4		0.5M+P +4		0.5M+P +5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	P+4		P+4		P+5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	0.5M+P +4		0.5M+P +4		0.5M+P +5		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	P+4		P+4		P+5		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{SPI0\_SCS}$ to slave driving SPI0_SOMI valid			P+17.5		P+20		P+27	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{SPI0\_SCS}$ to slave 3-stating SPI0_SOMI			P+17.5		P+20		P+27	ns
29	$t_{ena(SCSL\_ENA)S}$	Delay from master deasserting $\overline{SPI0\_SCS}$ to slave driving $\overline{SPI0\_ENA}$ valid			17.5		20		27	ns
30	$t_{dis(SPC\_ENA)S}$	Delay from final clock receive edge on SPI0_CLK to slave 3-stating or driving high $\overline{SPI0\_ENA}$.(4)	Polarity = 0, Phase = 0, from SPI0_CLK falling		2.5P+17 .5		2.5P+20		2.5P+27	ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising		2.5P+17 .5		2.5P+20		2.5P+27	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		2.5P+17 .5		2.5P+20		2.5P+27	
			Polarity = 1, Phase = 1, from SPI0_CLK falling		2.5P+17 .5		2.5P+20		2.5P+27	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-60).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(4) $\overline{SPI0\_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.

Table 6-67. General Timing Requirements for SPI1 Master Modes(1)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle Time, SPI1_CLK, All Master Modes		20(2)	256P	30(2)	256P	40(2)	256P	ns
2	$t_{w(SPCH)M}$	Pulse Width High, SPI1_CLK, All Master Modes		0.5M-1		0.5M-1		0.5M-1		ns
3	$t_{w(SPCL)M}$	Pulse Width Low, SPI1_CLK, All Master Modes		0.5M-1		0.5M-1		0.5M-1		ns
4,5	$t_{d(SIMO\_SPC)M}$	Delay, initial data bit valid on SPI1_SIMO to initial edge on SPI1_CLK(3)	Polarity = 0, Phase = 0, to SPI1_CLK rising		5		5		6	ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising		-0.5M+5		-0.5M+5		-0.5M+6	
			Polarity = 1, Phase = 0, to SPI1_CLK falling		5		5		6	
			Polarity = 1, Phase = 1, to SPI1_CLK falling		-0.5M+5		-0.5M+5		-0.5M+6	
5	$t_{d(SPC\_SIMO)M}$	Delay, subsequent bits valid on SPI1_SIMO after transmit edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK rising		5		5		6	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		5		5		6	
			Polarity = 1, Phase = 0, from SPI1_CLK falling		5		5		6	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		5		5		6	
6	$t_{oh(SPC\_SIMO)M}$	Output hold time, SPI1_SIMO valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5M-3		0.5M-3		0.5M-3		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	0.5M-3		0.5M-3		0.5M-3		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5M-3		0.5M-3		0.5M-3		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	0.5M-3		0.5M-3		0.5M-3		

(1) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(2) This timing is limited by the timing shown or 2P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI1_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI1_SOMI.

Table 6-67. General Timing Requirements for SPI1 Master Modes (continued)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
7	$t_{su(SOMI\_SPC)M}$	Input Setup Time, SPI1_SOMI valid before receive edge of SPI1_CLK	Polarity = 0, Phase = 0, to SPI1_CLK falling	1.5		1.5		1.5		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 0, to SPI1_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	1.5		1.5		1.5		
8	$t_{ih(SPC\_SOMI)M}$	Input Hold Time, SPI1_SOMI valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	4		5		6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	4		5		6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	4		5		6		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	4		5		6		

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Table 6-68. General Timing Requirements for SPI1 Slave Modes(1)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
9	$t_{c(SPC)S}$	Cycle Time, SPI1_CLK, All Slave Modes		40(2)	256P	50(2)	256P	60(2)	256P	ns
10	$t_{w(SPCH)S}$	Pulse Width High, SPI1_CLK, All Slave Modes		18		22		27		ns
11	$t_{w(SPCL)S}$	Pulse Width Low, SPI1_CLK, All Slave Modes		18		22		27		ns
12	$t_{su(SOMI\_SPC)S}$	Setup time, transmit data written to SPI before initial clock edge from master.(3)(4)	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P		2P		2P		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	2P		2P		2P		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P		2P		2P		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	2P		2P		2P		
13	$t_{d(SPC\_SOMI)S}$	Delay, subsequent bits valid on SPI1_SOMI after transmit edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK rising		15		17		19	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		15		17		19	
			Polarity = 1, Phase = 0, from SPI1_CLK falling		15		17		19	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		15		17		19	
14	$t_{oh(SPC\_SOMI)S}$	Output hold time, SPI1_SOMI valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5S-4		0.5S-10		0.5S-12		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	0.5S-4		0.5S-10		0.5S-12		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5S-4		0.5S-10		0.5S-12		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	0.5S-4		0.5S-10		0.5S-12		
15	$t_{su(SIMO\_SPC)S}$	Input Setup Time, SPI1_SIMO valid before receive edge of SPI1_CLK	Polarity = 0, Phase = 0, to SPI1_CLK falling	1.5		1.5		1.5		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 0, to SPI1_CLK rising	1.5		1.5		1.5		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	1.5		1.5		1.5		
16	$t_{ih(SPC\_SIMO)S}$	Input Hold Time, SPI1_SIMO valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	4		5		6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	4		5		6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	4		5		6		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	4		5		6		

(1) P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period)
(2) This timing is limited by the timing shown or 2P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI1_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI1_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the DSP CPU.

Table 6-69. Additional[1] SPI1 Master Timings, 4-Pin Enable Option[2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
17	$t_{d(EN\ A\_SPC)M}$	Delay from slave assertion of SPI1_ENA active to first SPI1_CLK from master.[4]	Polarity = 0, Phase = 0, to SPI1_CLK rising		3P+5		3P+5		3P+6	ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
			Polarity = 1, Phase = 0, to SPI1_CLK falling		3P+5		3P+5		3P+6	
			Polarity = 1, Phase = 1, to SPI1_CLK falling		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPI1_CLK falling		0.5M+P+5		0.5M+P+5		0.5M+P+6	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		P+5		P+5		P+6	
			Polarity = 1, Phase = 0, from SPI1_CLK rising		0.5M+P+5		0.5M+P+5		0.5M+P+6	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		P+5		P+5		P+6	

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-67).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA assertion.
(5) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.

Table 6-70. Additional[1] SPI1 Master Timings, 4-Pin Chip Select Option[2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
19	$t_{d(SCS\_SPC)M}$	Delay from SPI1_SCS active to first SPI1_CLK[4][5]	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P-1		2P-5		2P-6		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	0.5M+2P-1		0.5M+2P-5		0.5M+2P-6		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P-1		2P-5		2P-6		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	0.5M+2P-1		0.5M+2P-5		0.5M+2P-6		
20	$t_{d(SPC\_SCS)M}$	Delay from final SPI1_CLK edge to master deasserting SPI1_SCS[6][7]	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5M+P-1		0.5M+P-5		0.5M+P-6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	P-1		P-5		P-6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5M+P-1		0.5M+P-5		0.5M+P-6		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	P-1		P-5		P-6		

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-67).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

Table 6-71. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[4]	Polarity = 0, Phase = 0, from SPI1_CLK falling		0.5M+P+5		0.5M+P+5		0.5M+P+6	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		P+5		P+5		P+6	
			Polarity = 1, Phase = 0, from SPI1_CLK rising		0.5M+P+5		0.5M+P+5		0.5M+P+6	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		P+5		P+5		P+6	
20	$t_{d(SPC\_SCS)M}$	Delay from final SPI1_CLK edge to master deasserting SPI1_SCS [5][6]	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5M+P-1		0.5M+P-5		0.5M+P-6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	P-1		P-5		P-6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5M+P-1		0.5M+P-5		0.5M+P-6		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	P-1		P-5		P-6		
21	$t_{d(SCSL\_ENAL)M}$	Max delay for slave SPI to drive SPI1_ENA valid after master asserts SPI1_SCS to delay the master from beginning the next transfer,		C2TDELAY+P		C2TDELAY+P		C2TDELAY+P		ns
22	$t_{d(SCS\_SPC)M}$	Delay from SPI1_SCS active to first SPI1_CLK[7][8][9]	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P-1		2P-5		2P-6		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	0.5M+2P-1		0.5M+2P-5		0.5M+2P-6		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P-1		2P-5		2P-6		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	0.5M+2P-1		0.5M+2P-5		0.5M+2P-6		

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-68).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(7) If SPI1_ENA is asserted immediately such that the transmission is not delayed by SPI1_ENA.
(8) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].

Table 6-71. Additional SPI1 Master Timings, 5-Pin Option (continued)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
23	$t_{d(ENA\_SPC)M}$	Delay from assertion of $\overline{SPI1\_ENA}$ low to first SPI1_CLK edge.(10)	Polarity = 0, Phase = 0, to SPI1_CLK rising		3P+5		3P+5		3P+6	ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	
			Polarity = 1, Phase = 0, to SPI1_CLK falling		3P+5		3P+5		3P+6	
			Polarity = 1, Phase = 1, to SPI1_CLK falling		0.5M+3P+5		0.5M+3P+5		0.5M+3P+6	

(10) If $\overline{SPI1\_ENA}$ was initially deasserted high and SPI1_CLK is delayed.

Table 6-72. Additional[1] SPI1 Slave Timings, 4-Pin Enable Option[2][3]

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
24	$t_{d(SPC\_ENAH)S}$	Delay from final SPI1_CLK edge to slave deasserting SPI1_ENA.							
		Polarity = 0, Phase = 0, from SPI1_CLK falling	1.5P-3	2.5P+15	1.5P-10	2.5P+17	1.5P-12	2.5P+19	ns
		Polarity = 0, Phase = 1, from SPI1_CLK falling	–0.5M+1.5P-3	–0.5M+2.5P+15	–0.5M+1.5P-10	–0.5M+2.5P+17	–0.5M+1.5P-12	–0.5M+2.5P+19	
		Polarity = 1, Phase = 0, from SPI1_CLK rising	1.5P-3	2.5P+15	1.5P-10	2.5P+17	1.5P-12	2.5P+19	
		Polarity = 1, Phase = 1, from SPI1_CLK rising	–0.5M+1.5P-3	–0.5M+2.5P+15	–0.5M+1.5P-10	–0.5M+2.5P+17	–0.5M+1.5P-12	–0.5M+2.5P+19	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-68).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 6-73. Additional[1] SPI1 Slave Timings, 4-Pin Chip Select Option[2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{SPI1\_SCS}$ asserted at slave to first SPI1_CLK edge at slave.		P+1.5		P+1.5		P+1.5		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final SPI1_CLK edge before $\overline{SPI1\_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5M+P+4		0.5M+P+5		0.5M+P+6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	P+4		P+5		P+6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5M+P+4		0.5M+P+5		0.5M+P+6		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	P+4		P+5		P+6		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{SPI1\_SCS}$ to slave driving SPI1_SOMI valid			P+15		P+17		P+19	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{SPI1\_SCS}$ to slave 3-stating SPI1_SOMI			P+15		P+17		P+19	ns

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-68).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 6-74. Additional[1] SPI1 Slave Timings, 5-Pin Option[2][3]

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{SPI1\_SCS}$ asserted at slave to first SPI1_CLK edge at slave.		P+1.5		P+1.5		P+1.5		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final SPI1_CLK edge before $\overline{SPI1\_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI1_CLK falling	0.5M+P+4		0.5M+P+5		0.5M+P+6		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	P+4		P+5		P+6		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	0.5M+P+4		0.5M+P+5		0.5M+P+6		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	P+4		P+5		P+6		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{SPI1\_SCS}$ to slave driving SPI1_SOMI valid			P+15		P+17		P+19	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{SPI1\_SCS}$ to slave 3-stating SPI1_SOMI			P+15		P+17		P+19	ns
29	$t_{ena(SCSL\_ENA)S}$	Delay from master deasserting $\overline{SPI1\_SCS}$ to slave driving $\overline{SPI1\_ENA}$ valid			15		17		19	ns
30	$t_{dis(SPC\_ENA)S}$	Delay from final clock receive edge on SPI1_CLK to slave 3-stating or driving high $\overline{SPI1\_ENA}$.[4]	Polarity = 0, Phase = 0, from SPI1_CLK falling		2.5P+15		2.5P+17		2.5P+19	ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising		2.5P+15		2.5P+17		2.5P+19	
			Polarity = 1, Phase = 0, from SPI1_CLK rising		2.5P+15		2.5P+17		2.5P+19	
			Polarity = 1, Phase = 1, from SPI1_CLK falling		2.5P+15		2.5P+17		2.5P+19	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-68).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(4) $\overline{SPI1\_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.

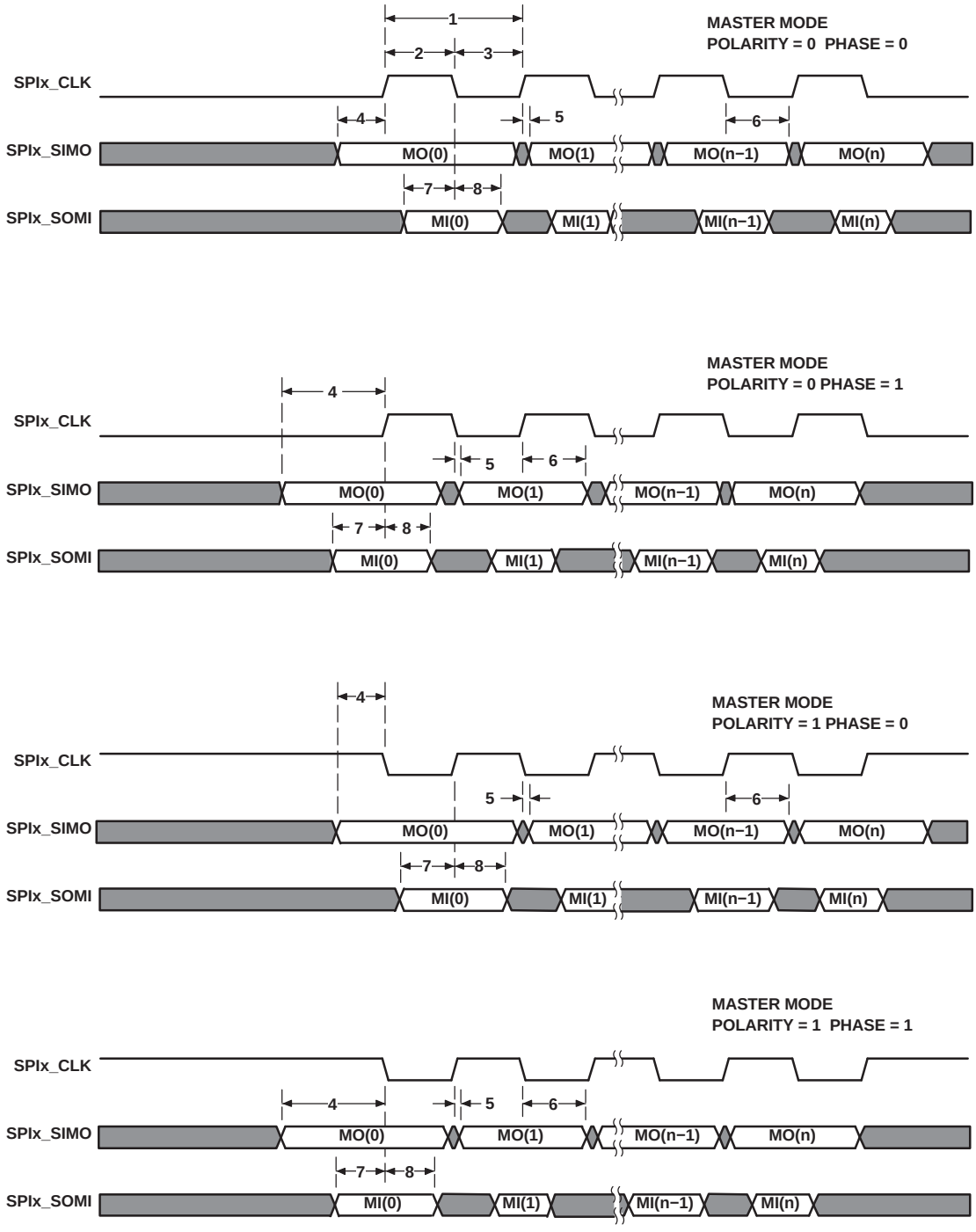

Figure 6-37. SPI Timings—Master Mode

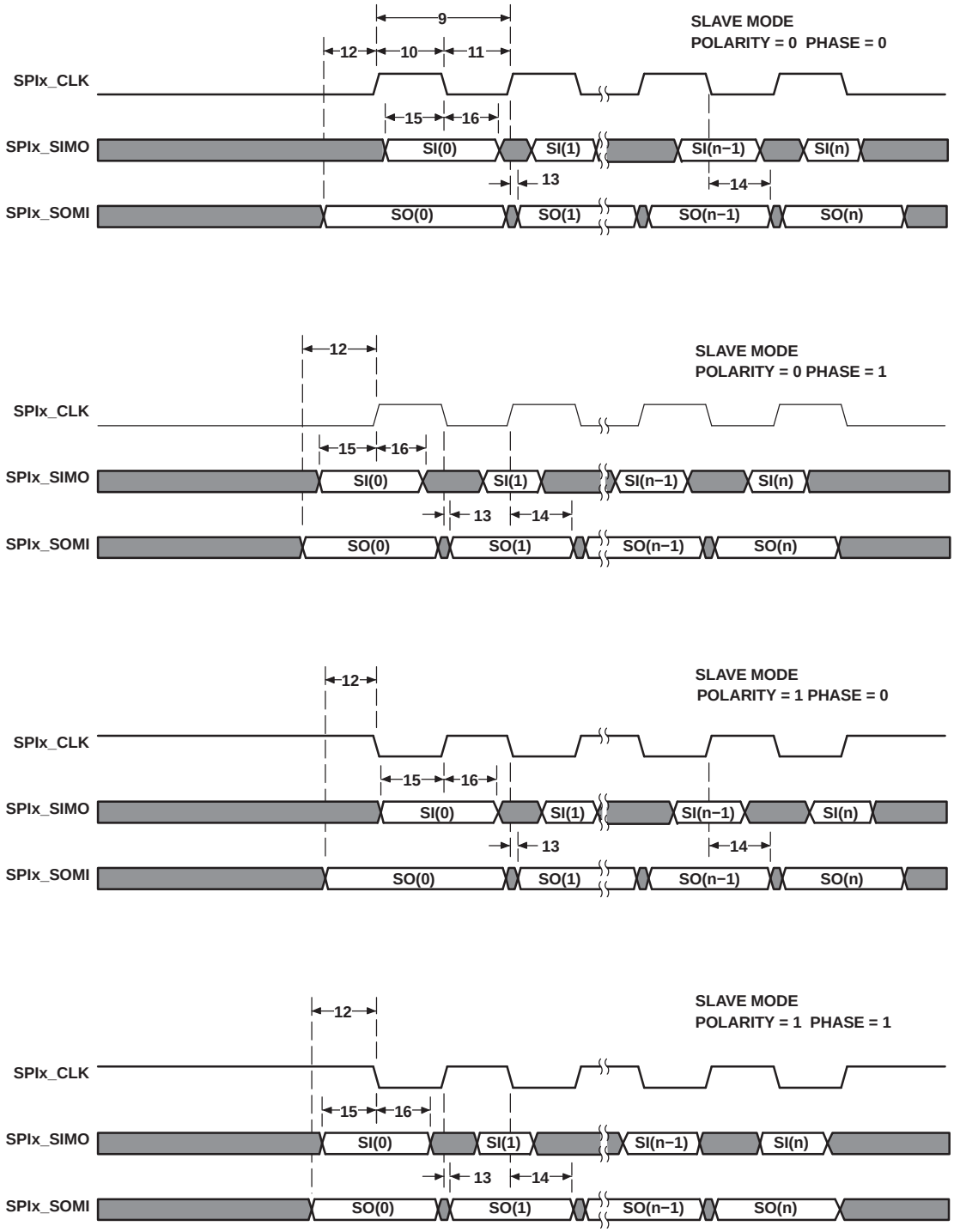

Figure 6-38. SPI Timings—Slave Mode

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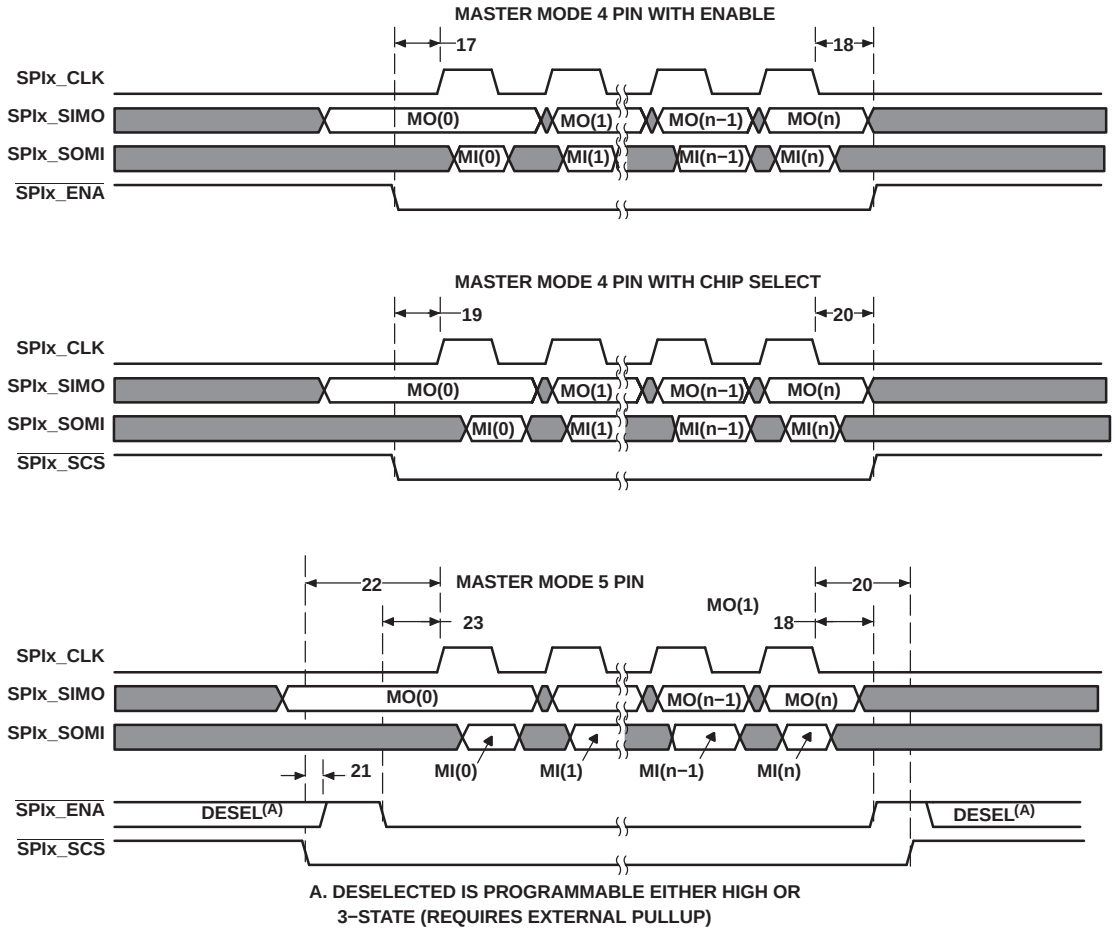

Figure 6-39. SPI Timings—Master Mode (4-Pin and 5-Pin)

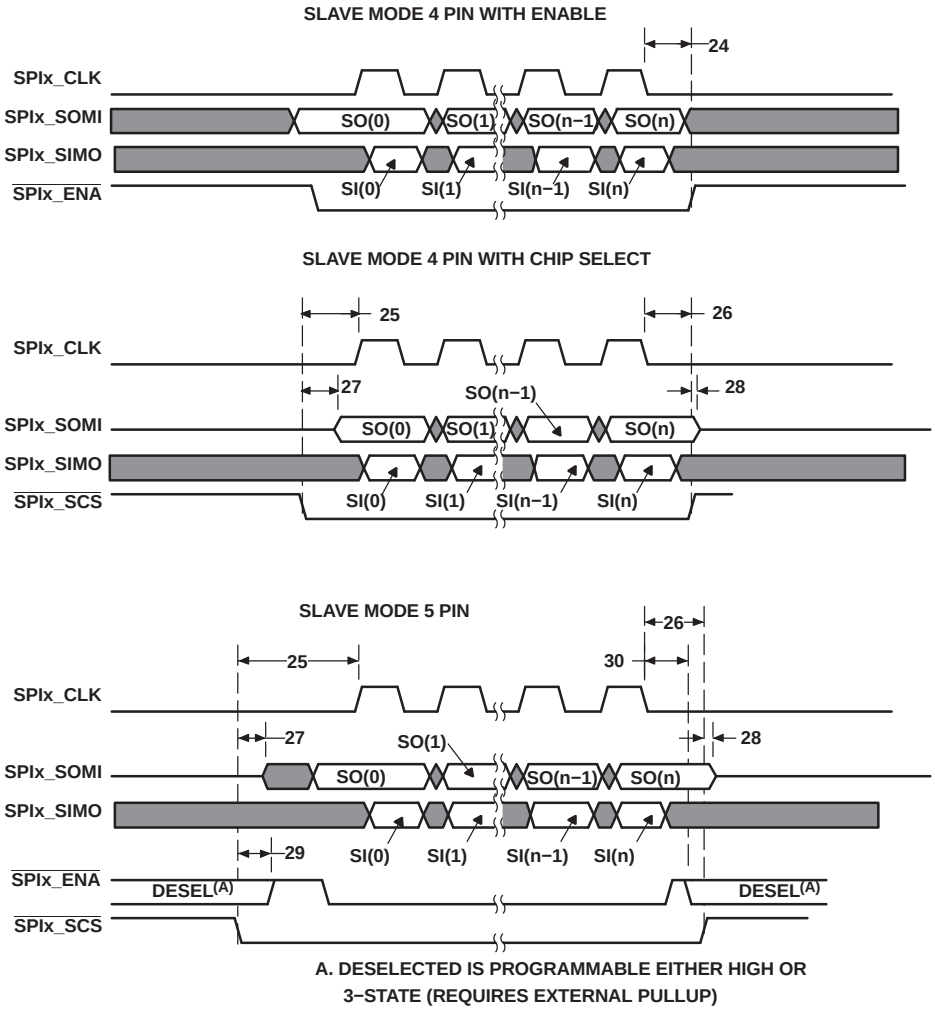

Figure 6-40. SPI Timings—Slave Mode (4-Pin and 5-Pin)

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6.17 Inter-Integrated Circuit Serial Ports (I2C)

6.17.1 I2C Device-Specific Information

Each I2C port supports:

- Compatible with Philips® I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- General-Purpose I/O Capability if not used as I2C

Figure 6-41 is block diagram of the device I2C Module.

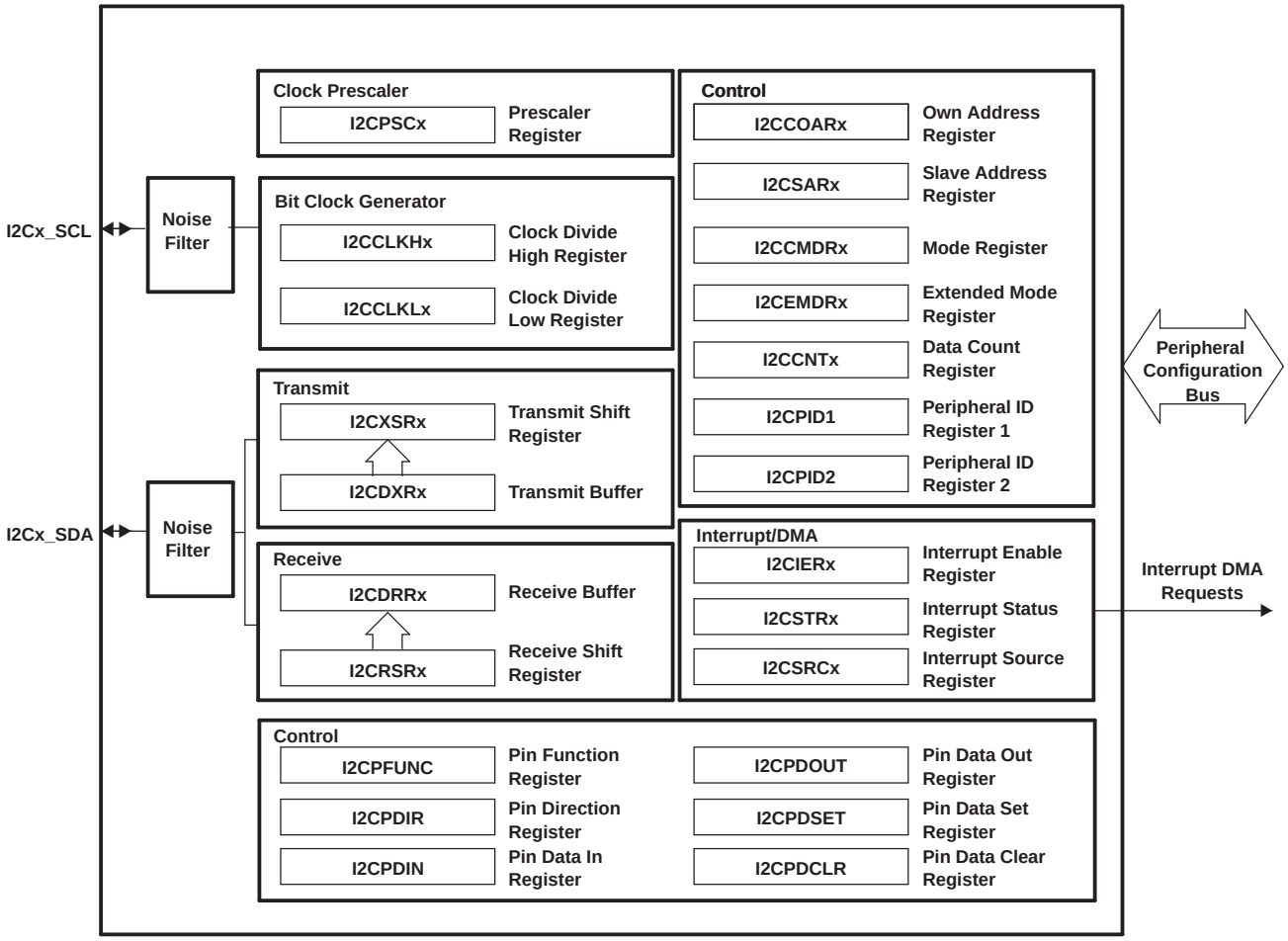

Figure 6-41. I2C Module Block Diagram

6.17.2 I2C Peripheral Registers Description(s)

Table 6-75 is the list of the I2C registers.

Table 6-75. Inter-Integrated Circuit (I2C) Registers

I2C0 BYTE ADDRESS	I2C1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C2 2000	0x01E2 8000	ICOAR	I2C Own Address Register
0x01C2 2004	0x01E2 8004	ICIMR	I2C Interrupt Mask Register
0x01C2 2008	0x01E2 8008	ICSTR	I2C Interrupt Status Register
0x01C2 200C	0x01E2 800C	ICCLKL	I2C Clock Low-Time Divider Register
0x01C2 2010	0x01E2 8010	ICCLKH	I2C Clock High-Time Divider Register
0x01C2 2014	0x01E2 8014	ICCNT	I2C Data Count Register
0x01C2 2018	0x01E2 8018	ICDRR	I2C Data Receive Register
0x01C2 201C	0x01E2 801C	ICSAR	I2C Slave Address Register
0x01C2 2020	0x01E2 8020	ICDXR	I2C Data Transmit Register
0x01C2 2024	0x01E2 8024	ICMDR	I2C Mode Register
0x01C2 2028	0x01E2 8028	ICIVR	I2C Interrupt Vector Register
0x01C2 202C	0x01E2 802C	ICEMDR	I2C Extended Mode Register
0x01C2 2030	0x01E2 8030	ICPSC	I2C Prescaler Register
0x01C2 2034	0x01E2 8034	REVID1	I2C Revision Identification Register 1
0x01C2 2038	0x01E2 8038	REVID2	I2C Revision Identification Register 2
0x01C2 2048	0x01E2 8048	ICPFUNC	I2C Pin Function Register
0x01C2 204C	0x01E2 804C	ICPDIR	I2C Pin Direction Register
0x01C2 2050	0x01E2 8050	ICPDIN	I2C Pin Data In Register
0x01C2 2054	0x01E2 8054	ICPDOUT	I2C Pin Data Out Register
0x01C2 2058	0x01E2 8058	ICPDSET	I2C Pin Data Set Register
0x01C2 205C	0x01E2 805C	ICPDCLR	I2C Pin Data Clear Register

6.17.3 I2C Electrical Data/Timing

6.17.3.1 Inter-Integrated Circuit (I2C) Timing

Table 6-76 and Table 6-77 assume testing over recommended operating conditions (see Figure 6-42 and Figure 6-43).

Table 6-76. Timing Requirements for I2C Input

NO.	PARAMETER		1.2V, 1.1V, 1.0V				UNIT
			Standard Mode		Fast Mode		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	4		0.6		µs
6	$t_{su(SDA-SCLH)}$	Setup time, I2Cx_SDA before I2Cx_SCL high	250		100		ns
7	$t_{h(SDA-SCLL)}$	Hold time, I2Cx_SDA after I2Cx_SCL low	0		0	0.9	µs
8	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, I2Cx_SDA		1000	$20 + 0.1C_b$	300	ns
10	$t_{r(SCL)}$	Rise time, I2Cx_SCL		1000	$20 + 0.1C_b$	300	ns
11	$t_{f(SDA)}$	Fall time, I2Cx_SDA		300	$20 + 0.1C_b$	300	ns
12	$t_{f(SCL)}$	Fall time, I2Cx_SCL		300	$20 + 0.1C_b$	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	N/A		0	50	ns
15	C_b	Capacitive load for each bus line		400		400	pF

Table 6-77. Switching Characteristics for I2C (1)

NO.	PARAMETER		1.2V, 1.1V, 1.0V				UNIT
			Standard Mode		Fast Mode		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	10		2.5		µs
17	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	4.7		0.6		µs
18	$t_{h(SDAL-SCLL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	4		0.6		µs
21	$t_{su(SDAV-SCLH)}$	Setup time, I2Cx_SDA valid before I2Cx_SCL high	250		100		ns
22	$t_{h(SCLL-SDAV)}$	Hold time, I2Cx_SDA valid after I2Cx_SCL low	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	4.7		1.3		µs
28	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	4		0.6		µs

(1) I2C must be configured correctly to meet the timings in Table 6-77.

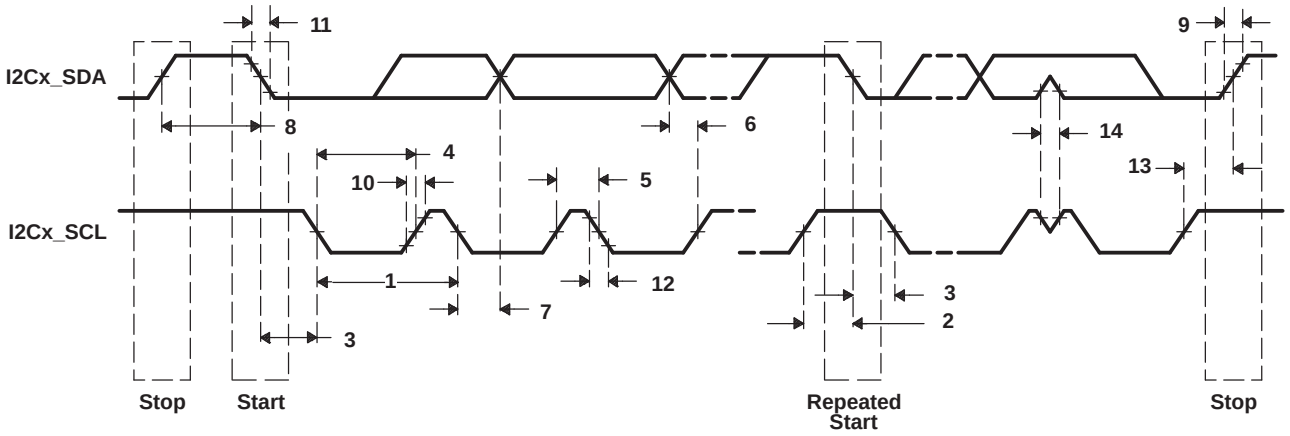

Figure 6-42. I2C Receive Timings

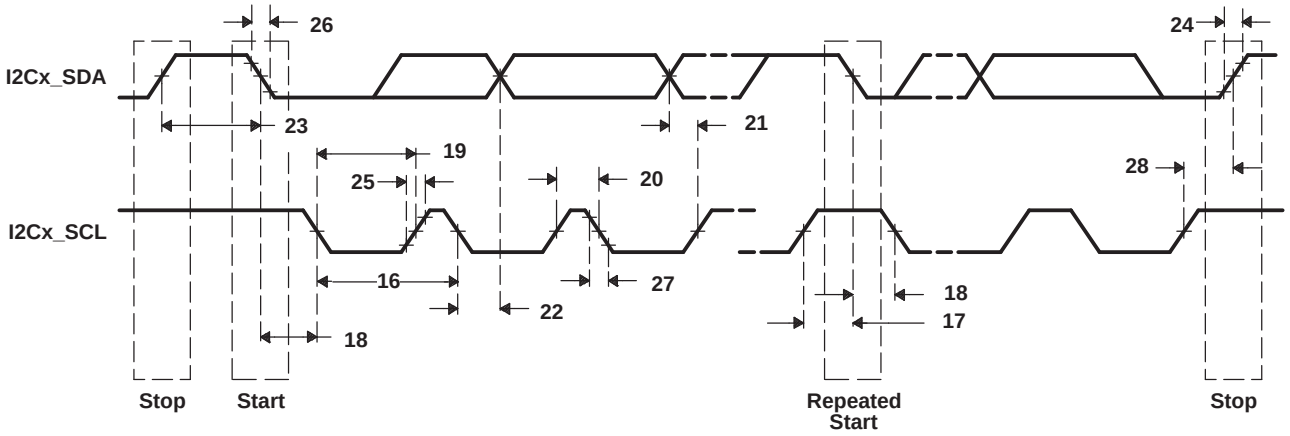

Figure 6-43. I2C Transmit Timings

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6.18 Universal Asynchronous Receiver/Transmitter (UART)

Each UART has the following features:

- 16-byte storage space for both the transmitter and receiver FIFOs
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- Programmable auto-rts and auto-cts for autoflow control
- Programmable Baud Rate up to 3MBaud
- Programmable Oversampling Options of x13 and x16
- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- Prioritized interrupts
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions (CTS, RTS)

The UART registers are listed in Section 6.18.1

6.18.1 UART Peripheral Registers Description(s)

Table 6-78 is the list of UART registers.

Table 6-78. UART Registers

UART0 BYTE ADDRESS	UART1 BYTE ADDRESS	UART2 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C4 2000	0x01D0 C000	0x01D0 D000	RBR	Receiver Buffer Register (read only)
0x01C4 2000	0x01D0 C000	0x01D0 D000	THR	Transmitter Holding Register (write only)
0x01C4 2004	0x01D0 C004	0x01D0 D004	IER	Interrupt Enable Register
0x01C4 2008	0x01D0 C008	0x01D0 D008	IIR	Interrupt Identification Register (read only)
0x01C4 2008	0x01D0 C008	0x01D0 D008	FCR	FIFO Control Register (write only)
0x01C4 200C	0x01D0 C00C	0x01D0 D00C	LCR	Line Control Register
0x01C4 2010	0x01D0 C010	0x01D0 D010	MCR	Modem Control Register
0x01C4 2014	0x01D0 C014	0x01D0 D014	LSR	Line Status Register
0x01C4 2018	0x01D0 C018	0x01D0 D018	MSR	Modem Status Register
0x01C4 201C	0x01D0 C01C	0x01D0 D01C	SCR	Scratchpad Register
0x01C4 2020	0x01D0 C020	0x01D0 D020	DLL	Divisor LSB Latch
0x01C4 2024	0x01D0 C024	0x01D0 D024	DLH	Divisor MSB Latch
0x01C4 2028	0x01D0 C028	0x01D0 D028	REVID1	Revision Identification Register 1
0x01C4 2030	0x01D0 C030	0x01D0 D030	PWREMU_MGMT	Power and Emulation Management Register
0x01C4 2034	0x01D0 C034	0x01D0 D034	MDR	Mode Definition Register

6.18.2 UART Electrical Data/Timing

Table 6-79. Timing Requirements for UART Receive[1] (see Figure 6-44)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (RXDn)	0.96U	1.05U	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.96U	1.05U	ns

(1) U = UART baud time = 1/programmed baud rate.

Table 6-80. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit[1] (see Figure 6-44)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$f_{(baud)}$	Maximum programmable baud rate		3	MBaud
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (TXDn)	U - 2	U + 2	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit	U - 2	U + 2	ns

(1) U = UART baud time = 1/programmed baud rate.

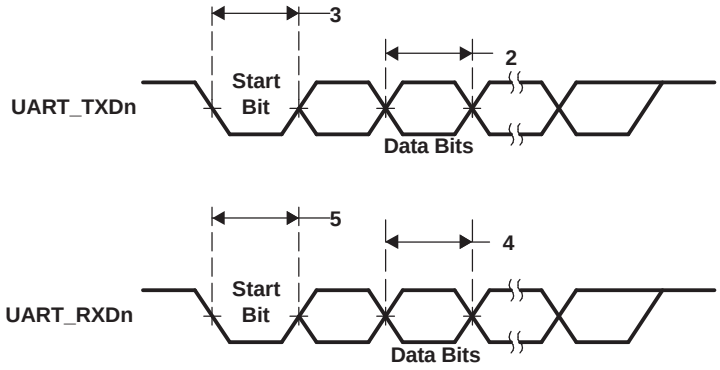

Figure 6-44. UART Transmit/Receive Timing

PRODUCT PREVIEW

6.19 Universal Serial Bus OTG Controller (USB0) [USB2.0 OTG]

The USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s - C6747 only) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 4 Transmit (TX) and 4 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

Table 6-81 is the list of USB OTG registers.

Table 6-81. Universal Serial Bus OTG (USB0) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E0 0000	REVID	Revision Register
0x01E0 0004	CTRLR	Control Register
0x01E0 0008	STATR	Status Register
0x01E0 000C	EMUR	Emulation Register
0x01E0 0010	MODE	Mode Register
0x01E0 0014	AUTOREQ	Autorequest Register
0x01E0 0018	SRPFIXTIME	SRP Fix Time Register
0x01E0 001C	TEARDOWN	Teardown Register
0x01E0 0020	INTSRCR	USB Interrupt Source Register
0x01E0 0024	INTSETR	USB Interrupt Source Set Register
0x01E0 0028	INTCLRR	USB Interrupt Source Clear Register
0x01E0 002C	INTMSKR	USB Interrupt Mask Register
0x01E0 0030	INTMSKSETR	USB Interrupt Mask Set Register
0x01E0 0034	INTMSKCLRR	USB Interrupt Mask Clear Register
0x01E0 0038	INTMASKEDR	USB Interrupt Source Masked Register
0x01E0 003C	EOIR	USB End of Interrupt Register
0x01E0 0040	INTVECTR	USB Interrupt Vector Register
0x01E0 0050	GENRNDISSZ1	Generic RNDIS Size EP1
0x01E0 0054	GENRNDISSZ2	Generic RNDIS Size EP2
0x01E0 0058	GENRNDISSZ3	Generic RNDIS Size EP3
0x01E0 005C	GENRNDISSZ4	Generic RNDIS Size EP4
0x01E0 0400	FADDR	Function Address Register
0x01E0 0401	POWER	Power Management Register
0x01E0 0402	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
0x01E0 0404	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
0x01E0 0406	INTRTXE	Interrupt enable register for INTRTX
0x01E0 0408	INTRRXE	Interrupt Enable Register for INTRRX
0x01E0 040A	INTRUSB	Interrupt Register for Common USB Interrupts
0x01E0 040B	INTRUSBE	Interrupt Enable Register for INTRUSB
0x01E0 040C	FRAME	Frame Number Register
0x01E0 040E	INDEX	Index Register for Selecting the Endpoint Status and Control Registers
0x01E0 040F	TESTMODE	Register to Enable the USB 2.0 Test Modes

Table 6-81. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
Indexed Registers These registers operate on the endpoint selected by the INDEX register		
0x01E0 0410	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint (Index register set to select Endpoints 1-4 only)
0x01E0 0412	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
0x01E0 0414	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint (Index register set to select Endpoints 1-4 only)
0x01E0 0416	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint. (Index register set to select Endpoints 1-4)
0x01E0 0418	COUNT0	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
0x01E0 041A	HOST_TYPE0	Defines the speed of Endpoint 0
	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041B	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0. (Index register set to select Endpoint 0)
	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041F	CONFIGDATA	Returns details of core configuration. (Index register set to select Endpoint 0)
FIFO		
0x01E0 0420	FIFO0	Transmit and Receive FIFO Register for Endpoint 0
0x01E0 0424	FIFO1	Transmit and Receive FIFO Register for Endpoint 1
0x01E0 0428	FIFO2	Transmit and Receive FIFO Register for Endpoint 2
0x01E0 042C	FIFO3	Transmit and Receive FIFO Register for Endpoint 3
0x01E0 0430	FIFO4	Transmit and Receive FIFO Register for Endpoint 4
OTG Device Control		
0x01E0 0460	DEVCTL	Device Control Register
Dynamic FIFO Control		
0x01E0 0462	TXFIFOSZ	Transmit Endpoint FIFO Size (Index register set to select Endpoints 1-4 only)
0x01E0 0463	RXFIFOSZ	Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4 only)
0x01E0 0464	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4 only)
0x01E0 0464	HWVERS	Hardware Version Register
0x01E0 0466	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4 only)
Target Endpoint 0 Control Registers, Valid Only in Host Mode		

Table 6-81. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E0 0480	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 0482	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0483	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0484	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 0486	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0487	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 1 Control Registers, Valid Only in Host Mode		
0x01E0 0488	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 048A	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048B	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048C	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 048E	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048F	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 2 Control Registers, Valid Only in Host Mode		
0x01E0 0490	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 0492	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0493	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0494	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 0496	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0497	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 3 Control Registers, Valid Only in Host Mode		
0x01E0 0498	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 049A	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049B	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049C	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 049E	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049F	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 4 Control Registers, Valid Only in Host Mode		
0x01E0 04A0	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.

Table 6-81. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E0 04A2	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A3	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A4	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 04A6	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A7	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Control and Status Register for Endpoint 0		
0x01E0 0502	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01E0 0508	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01E0 050A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01E0 050B	HOST_NAKLIMIT0	Sets the NAK Response Timeout on Endpoint 0
0x01E0 050F	CONFIGDATA	Returns details of core configuration.
Control and Status Register for Endpoint 1		
0x01E0 0510	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0512	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0514	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0516	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0518	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 051A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 051B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 051C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 051D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 2		
0x01E0 0520	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0522	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0524	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0526	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0528	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 052A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 052B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 052C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.

Table 6-81. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E0 052D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 3		
0x01E0 0530	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0532	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0534	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0536	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0538	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 053A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 053B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 053C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 053D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 4		
0x01E0 0540	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0542	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0544	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0546	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0548	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 054A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 054B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 054C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 054D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
DMA Registers		
0x01E0 1000	DMAREVID	DMA Revision Register
0x01E0 1004	TDFDQ	DMA Teardown Free Descriptor Queue Control Register
0x01E0 1008	DMAEMU	DMA Emulation Control Register
0x01E0 1800	TXGCR[0]	Transmit Channel 0 Global Configuration Register
0x01E0 1808	RXGCR[0]	Receive Channel 0 Global Configuration Register
0x01E0 180C	RXHPCRA[0]	Receive Channel 0 Host Packet Configuration Register A
0x01E0 1810	RXHPCRB[0]	Receive Channel 0 Host Packet Configuration Register B
0x01E0 1820	TXGCR[1]	Transmit Channel 1 Global Configuration Register
0x01E0 1828	RXGCR[1]	Receive Channel 1 Global Configuration Register
0x01E0 182C	RXHPCRA[1]	Receive Channel 1 Host Packet Configuration Register A
0x01E0 1830	RXHPCRB[1]	Receive Channel 1 Host Packet Configuration Register B
0x01E0 1840	TXGCR[2]	Transmit Channel 2 Global Configuration Register

Table 6-81. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E0 1848	RXGCR[2]	Receive Channel 2 Global Configuration Register
0x01E0 184C	RXHPCRA[2]	Receive Channel 2 Host Packet Configuration Register A
0x01E0 1850	RXHPCRB[2]	Receive Channel 2 Host Packet Configuration Register B
0x01E0 1860	TXGCR[3]	Transmit Channel 3 Global Configuration Register
0x01E0 1868	RXGCR[3]	Receive Channel 3 Global Configuration Register
0x01E0 186C	RXHPCRA[3]	Receive Channel 3 Host Packet Configuration Register A
0x01E0 1870	RXHPCRB[3]	Receive Channel 3 Host Packet Configuration Register B
0x01E0 2C00	DMA_SCHED_CTRL	DMA Scheduler Control Register
0x01E0 2D00	ENTRY[0]	DMA Scheduler Table Word 0
0x01E0 2D04	ENTRY[1]	DMA Scheduler Table Word 1
. . .	. . .	. . .
0x01E0 2DFC	ENTRY[63]	DMA Scheduler Table Word 63
Queue Manager Registers		
0x01E0 4000	QMGRREVID	Queue Manager Revision Register
0x01E0 4008	DIVERSION	Queue Diversion Register
0x01E0 4020	FDBSC0	Free Descriptor/Buffer Starvation Count Register 0
0x01E0 4024	FDBSC1	Free Descriptor/Buffer Starvation Count Register 1
0x01E0 4028	FDBSC2	Free Descriptor/Buffer Starvation Count Register 2
0x01E0 402C	FDBSC3	Free Descriptor/Buffer Starvation Count Register 3
0x01E0 4080	LRAM0BASE	Linking RAM Region 0 Base Address Register
0x01E0 4084	LRAM0SIZE	Linking RAM Region 0 Size Register
0x01E0 4088	LRAM1BASE	Linking RAM Region 1 Base Address Register
0x01E0 4090	PEND0	Queue Pending Register 0
0x01E0 4094	PEND1	Queue Pending Register 1
0x01E0 5000	QMEMRBASE[0]	Memory Region 0 Base Address Register
0x01E0 5004	QMEMRCTRL[0]	Memory Region 0 Control Register
0x01E0 5010	QMEMRBASE[1]	Memory Region 1 Base Address Register
0x01E0 5014	QMEMRCTRL[1]	Memory Region 1 Control Register
. . .	. . .	. . .
0x01E0 5070	QMEMRBASE[7]	Memory Region 7 Base Address Register
0x01E0 5074	QMEMRCTRL[7]	Memory Region 7 Control Register
0x01E0 600C	CTRLD[0]	Queue Manager Queue 0 Control Register D
0x01E0 601C	CTRLD[1]	Queue Manager Queue 1 Control Register D
. . .	. . .	. . .
0x01E0 63FC	CTRLD[63]	Queue Manager Queue 63 Status Register D
0x01E0 6800	QSTATA[0]	Queue Manager Queue 0 Status Register A
0x01E0 6804	QSTATB[0]	Queue Manager Queue 0 Status Register B
0x01E0 6808	QSTATC[0]	Queue Manager Queue 0 Status Register C
0x01E0 6810	QSTATA[1]	Queue Manager Queue 1 Status Register A
0x01E0 6814	QSTATB[1]	Queue Manager Queue 1 Status Register B
0x01E0 6818	QSTATC[1]	Queue Manager Queue 1 Status Register C
. . .	. . .	. . .
0x01E0 6BF0	QSTATA[63]	Queue Manager Queue 63 Status Register A
0x01E0 6BF4	QSTATB[63]	Queue Manager Queue 63 Status Register B
0x01E0 6BF8	QSTATC[63]	Queue Manager Queue 63 Status Register C

6.19.1 USB0 [USB2.0] Electrical Data/Timing

Table 6-82. Switching Characteristics Over Recommended Operating Conditions for USB0 [USB2.0] (see Figure 6-45)

NO.	PARAMETER		1.2V, 1.1V, 1.0V						UNIT
			LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(1)	75	300	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(1)	75	300	4	20	0.5		ns
3	t_{rfM}	Rise/Fall time, matching(2)	80	120	90	111	–	–	%
4	V_{CRS}	Output signal cross-over voltage(1)	1.3	2	1.3	2	–	–	V
5	$t_{jr(source)NT}$	Source (Host) Driver jitter, next transition		2		2			(3)ns
	$t_{jr(FUNC)NT}$	Function Driver jitter, next transition		25		2		(3)	ns
6	$t_{jr(source)PT}$	Source (Host) Driver jitter, paired transition(4)		1		1		(3)	ns
	$t_{jr(FUNC)PT}$	Function Driver jitter, paired transition		10		1		(3)	ns
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver	670		82		–		ns
9	$t_{(DRATE)}$	Data Rate		1.5		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	–	–	40.5	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	100k		100k		-	-	Ω

(1) Low Speed: C_L = 200 pF, Full Speed: C_L = 50 pF, High Speed: C_L = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

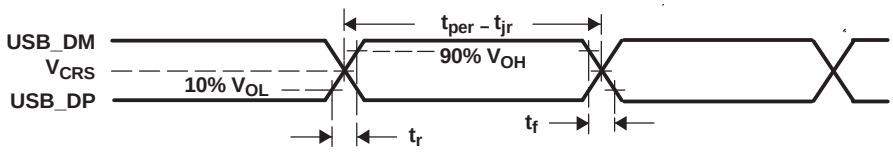

Figure 6-45. USB2.0 Integrated Transceiver Interface Timing

6.20 Universal Serial Bus Host Controller (USB1) [USB1.1 OHCI]

All the USB interfaces for this device are compliant with Universal Serial Bus Specifications, Revision 1.1.

Table 6-83 is the list of USB Host Controller registers.

Table 6-83. USB Host Controller Registers

USB1 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 5000	HCREVISION	OHCI Revision Number Register
0x01E2 5004	HCCONTROL	HC Operating Mode Register
0x01E2 5008	HCCOMMANDSTATUS	HC Command and Status Register
0x01E2 500C	HCINTERRUPTSTATUS	HC Interrupt and Status Register
0x01E2 5010	HCINTERRUPTENABLE	HC Interrupt Enable Register
0x01E2 5014	HCINTERRUPTDISABLE	HC Interrupt Disable Register
0x01E2 5018	HCHCCA	HC HCAA Address Register(1)
0x01E2 501C	HCPERIODCURRENTED	HC Current Periodic Register(1)
0x01E2 5020	HCCONTROLHEADED	HC Head Control Register(1)
0x01E2 5024	HCCONTROLCURRENTED	HC Current Control Register(1)
0x01E2 5028	HCBULKHEADED	HC Head Bulk Register(1)
0x01E2 502C	HCBULKCURRENTED	HC Current Bulk Register(1)
0x01E2 5030	HCDONEHEAD	HC Head Done Register(1)
0x01E2 5034	HCFMINTERVAL	HC Frame Interval Register
0x01E2 5038	HCFMREMAINING	HC Frame Remaining Register
0x01E2 503C	HCFMNUMBER	HC Frame Number Register
0x01E2 5040	HCPERIODICSTART	HC Periodic Start Register
0x01E2 5044	HCLSTHRESHOLD	HC Low-Speed Threshold Register
0x01E2 5048	HCRHDESCRIPTORA	HC Root Hub A Register
0x01E2 504C	HCRHDESCRIPTORB	HC Root Hub B Register
0x01E2 5050	HCRHSTATUS	HC Root Hub Status Register
0x01E2 5054	HCRHPORTSTATUS1	HC Port 1 Status and Control Register(2)
0x01E2 5058	HCRHPORTSTATUS2	HC Port 2 Status and Control Register(3)

(1) Restrictions apply to the physical addresses used in these registers.
(2) Connected to the integrated USB1.1 phy pins (USB1_DM, USB1_DP).
(3) Although the controller implements two ports, the second port cannot be used.

Table 6-84. Switching Characteristics Over Recommended Operating Conditions for USB1 [USB1.1]

NO.	PARAMETER		1.2V, 1.1V, 1.0V				UNIT
			LOW SPEED		FULL SPEED		
			MIN	MAX	MAX	MAX	
U1	t_r	Rise time, USB.DP and USB.DM signals(1)	75(1)	300(1)	4(1)	20(1)	ns
U2	t_f	Fall time, USB.DP and USB.DM signals(1)	75(1)	300(1)	4(1)	20(1)	ns
U3	t_{RFM}	Rise/Fall time matching(2)	80(2)	120(2)	90(2)	110(2)	%
U4	V_{CRS}	Output signal cross-over voltage(1)	1.3(1)	2(1)	1.3(1)	2(1)	V
U5	t_j	Differential propagation jitter(3)	-25(3)	25(3)	-2(3)	2(3)	ns
U6	f_{op}	Operating frequency(4)		1.5		12	MHz

(1) Low Speed: C_L = 200 pF. High Speed: C_L = 50pF
(2) $t_{RFM} = (t_r/t_f) \times 100$
(3) $t_{jr} = t_{px(1)} - t_{px(0)}$
(4) $f_{op} = 1/t_{per}$

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6.21 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between device and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

6.21.1 EMAC Peripheral Register Description(s)

Table 6-85. Ethernet Media Access Controller (EMAC) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 3000	TXREV	Transmit Revision Register
0x01E2 3004	TXCONTROL	Transmit Control Register
0x01E2 3008	TXTEARDOWN	Transmit Teardown Register
0x01E2 3010	RXREV	Receive Revision Register
0x01E2 3014	RXCONTROL	Receive Control Register
0x01E2 3018	RXTEARDOWN	Receive Teardown Register
0x01E2 3080	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
0x01E2 3084	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
0x01E2 3088	TXINTMASKSET	Transmit Interrupt Mask Set Register
0x01E2 308C	TXINTMASKCLEAR	Transmit Interrupt Clear Register
0x01E2 3090	MACINVECTOR	MAC Input Vector Register
0x01E2 3094	MACEOIVECTOR	MAC End Of Interrupt Vector Register
0x01E2 30A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
0x01E2 30A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
0x01E2 30A8	RXINTMASKSET	Receive Interrupt Mask Set Register
0x01E2 30AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
0x01E2 30B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register
0x01E2 30B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
0x01E2 30B8	MACINTMASKSET	MAC Interrupt Mask Set Register
0x01E2 30BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
0x01E2 3100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
0x01E2 3104	RXUNICASTSET	Receive Unicast Enable Set Register
0x01E2 3108	RXUNICASTCLEAR	Receive Unicast Clear Register
0x01E2 310C	RXMAXLEN	Receive Maximum Length Register
0x01E2 3110	RXBUFFEROFFSET	Receive Buffer Offset Register
0x01E2 3114	RXFILTERLOWTHRESH	Receive Filter Low Priority Frame Threshold Register
0x01E2 3120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
0x01E2 3124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
0x01E2 3128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
0x01E2 312C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
0x01E2 3130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
0x01E2 3134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
0x01E2 3138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
0x01E2 313C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register

Table 6-85. Ethernet Media Access Controller (EMAC) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 3140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
0x01E2 3144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
0x01E2 3148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
0x01E2 314C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
0x01E2 3150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register
0x01E2 3154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
0x01E2 3158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register
0x01E2 315C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
0x01E2 3160	MACCONTROL	MAC Control Register
0x01E2 3164	MACSTATUS	MAC Status Register
0x01E2 3168	EMCONTROL	Emulation Control Register
0x01E2 316C	FIFOCONTROL	FIFO Control Register
0x01E2 3170	MACCONFIG	MAC Configuration Register
0x01E2 3174	SOFTRESET	Soft Reset Register
0x01E2 31D0	MACSRCADDRLO	MAC Source Address Low Bytes Register
0x01E2 31D4	MACSRCADDRHI	MAC Source Address High Bytes Register
0x01E2 31D8	MACHASH1	MAC Hash Address Register 1
0x01E2 31DC	MACHASH2	MAC Hash Address Register 2
0x01E2 31E0	BOFFTEST	Back Off Test Register
0x01E2 31E4	TPACETEST	Transmit Pacing Algorithm Test Register
0x01E2 31E8	RXPAUSE	Receive Pause Timer Register
0x01E2 31EC	TXPAUSE	Transmit Pause Timer Register
0x01E2 3200 - 0x01E2 32FC	(see Table 6-86)	EMAC Statistics Registers
0x01E2 3500	MACADDRLO	MAC Address Low Bytes Register, Used in Receive Address Matching
0x01E2 3504	MACADDRHI	MAC Address High Bytes Register, Used in Receive Address Matching
0x01E2 3508	MACINDEX	MAC Index Register
0x01E2 3600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
0x01E2 3604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
0x01E2 3608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
0x01E2 360C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
0x01E2 3610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
0x01E2 3614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
0x01E2 3618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
0x01E2 361C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register
0x01E2 3620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
0x01E2 3624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
0x01E2 3628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register
0x01E2 362C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
0x01E2 3630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
0x01E2 3634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
0x01E2 3638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
0x01E2 363C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
0x01E2 3640	TX0CP	Transmit Channel 0 Completion Pointer Register
0x01E2 3644	TX1CP	Transmit Channel 1 Completion Pointer Register
0x01E2 3648	TX2CP	Transmit Channel 2 Completion Pointer Register
0x01E2 364C	TX3CP	Transmit Channel 3 Completion Pointer Register
0x01E2 3650	TX4CP	Transmit Channel 4 Completion Pointer Register

Table 6-85. Ethernet Media Access Controller (EMAC) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 3654	TX5CP	Transmit Channel 5 Completion Pointer Register
0x01E2 3658	TX6CP	Transmit Channel 6 Completion Pointer Register
0x01E2 365C	TX7CP	Transmit Channel 7 Completion Pointer Register
0x01E2 3660	RX0CP	Receive Channel 0 Completion Pointer Register
0x01E2 3664	RX1CP	Receive Channel 1 Completion Pointer Register
0x01E2 3668	RX2CP	Receive Channel 2 Completion Pointer Register
0x01E2 366C	RX3CP	Receive Channel 3 Completion Pointer Register
0x01E2 3670	RX4CP	Receive Channel 4 Completion Pointer Register
0x01E2 3674	RX5CP	Receive Channel 5 Completion Pointer Register
0x01E2 3678	RX6CP	Receive Channel 6 Completion Pointer Register
0x01E2 367C	RX7CP	Receive Channel 7 Completion Pointer Register

Table 6-86. EMAC Statistics Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 3200	RXGOODFRAMES	Good Receive Frames Register
0x01E2 3204	RXBCASTFRAMES	Broadcast Receive Frames Register (Total number of good broadcast frames received)
0x01E2 3208	RXMCASTFRAMES	Multicast Receive Frames Register (Total number of good multicast frames received)
0x01E2 320C	RXPAUSEFRAMES	Pause Receive Frames Register
0x01E2 3210	RXCRCERRORS	Receive CRC Errors Register (Total number of frames received with CRC errors)
0x01E2 3214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors)
0x01E2 3218	RXOVERSIZED	Receive Oversized Frames Register (Total number of oversized frames received)
0x01E2 321C	RXJABBER	Receive Jabber Frames Register (Total number of jabber frames received)
0x01E2 3220	RXUNDERSIZED	Receive Undersized Frames Register (Total number of undersized frames received)
0x01E2 3224	RXFRAGMENTS	Receive Frame Fragments Register
0x01E2 3228	RXFILTERED	Filtered Receive Frames Register
0x01E2 322C	RXQOSFILTERED	Received QOS Filtered Frames Register
0x01E2 3230	RXOCTETS	Receive Octet Frames Register (Total number of received bytes in good frames)
0x01E2 3234	TXGOODFRAMES	Good Transmit Frames Register (Total number of good frames transmitted)
0x01E2 3238	TXBCASTFRAMES	Broadcast Transmit Frames Register
0x01E2 323C	TXMCASTFRAMES	Multicast Transmit Frames Register
0x01E2 3240	TXPAUSEFRAMES	Pause Transmit Frames Register
0x01E2 3244	TXDEFERRED	Deferred Transmit Frames Register
0x01E2 3248	TXCOLLISION	Transmit Collision Frames Register
0x01E2 324C	TXSINGLECOLL	Transmit Single Collision Frames Register
0x01E2 3250	TXMULTICOLL	Transmit Multiple Collision Frames Register
0x01E2 3254	TXEXCESSIVECOLL	Transmit Excessive Collision Frames Register
0x01E2 3258	TXLATECOLL	Transmit Late Collision Frames Register
0x01E2 325C	TXUNDERRUN	Transmit Underrun Error Register
0x01E2 3260	TXCARRIERSENSE	Transmit Carrier Sense Errors Register
0x01E2 3264	TXOCTETS	Transmit Octet Frames Register
0x01E2 3268	FRAME64	Transmit and Receive 64 Octet Frames Register

Table 6-86. EMAC Statistics Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 326C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
0x01E2 3270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
0x01E2 3274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
0x01E2 3278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
0x01E2 327C	FRAME1024TUP	Transmit and Receive 1024 to 1518 Octet Frames Register
0x01E2 3280	NETOCTETS	Network Octet Frames Register
0x01E2 3284	RXSOFOVERRUNS	Receive FIFO or DMA Start of Frame Overruns Register
0x01E2 3288	RXMOFOVERRUNS	Receive FIFO or DMA Middle of Frame Overruns Register
0x01E2 328C	RXDMAOVERRUNS	Receive DMA Start of Frame and Middle of Frame Overruns Register

Table 6-87. EMAC Control Module Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 2000	REV	EMAC Control Module Revision Register
0x01E2 2004	SOFTRESET	EMAC Control Module Software Reset Register
0x01E2 200C	INTCONTROL	EMAC Control Module Interrupt Control Register
0x01E2 2010	C0RXTHRESHEN	EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Enable Register
0x01E2 2014	C0RXEN	EMAC Control Module Interrupt Core 0 Receive Interrupt Enable Register
0x01E2 2018	C0TXEN	EMAC Control Module Interrupt Core 0 Transmit Interrupt Enable Register
0x01E2 201C	C0MISCEN	EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Enable Register
0x01E2 2020	C1RXTHRESHEN	EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Enable Register
0x01E2 2024	C1RXEN	EMAC Control Module Interrupt Core 1 Receive Interrupt Enable Register
0x01E2 2028	C1TXEN	EMAC Control Module Interrupt Core 1 Transmit Interrupt Enable Register
0x01E2 202C	C1MISCEN	EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Enable Register
0x01E2 2030	C2RXTHRESHEN	EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Enable Register
0x01E2 2034	C2RXEN	EMAC Control Module Interrupt Core 2 Receive Interrupt Enable Register
0x01E2 2038	C2TXEN	EMAC Control Module Interrupt Core 2 Transmit Interrupt Enable Register
0x01E2 203C	C2MISCEN	EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Enable Register
0x01E2 2040	C0RXTHRESHSTAT	EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Status Register
0x01E2 2044	C0RXSTAT	EMAC Control Module Interrupt Core 0 Receive Interrupt Status Register
0x01E2 2048	C0TXSTAT	EMAC Control Module Interrupt Core 0 Transmit Interrupt Status Register
0x01E2 204C	C0MISCSTAT	EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Status Register
0x01E2 2050	C1RXTHRESHSTAT	EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Status Register
0x01E2 2054	C1RXSTAT	EMAC Control Module Interrupt Core 1 Receive Interrupt Status Register
0x01E2 2058	C1TXSTAT	EMAC Control Module Interrupt Core 1 Transmit Interrupt Status Register
0x01E2 205C	C1MISCSTAT	EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Status Register
0x01E2 2060	C2RXTHRESHSTAT	EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Status Register
0x01E2 2064	C2RXSTAT	EMAC Control Module Interrupt Core 2 Receive Interrupt Status Register
0x01E2 2068	C2TXSTAT	EMAC Control Module Interrupt Core 2 Transmit Interrupt Status Register
0x01E2 206C	C2MISCSTAT	EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Status Register
0x01E2 2070	C0RXIMAX	EMAC Control Module Interrupt Core 0 Receive Interrupts Per Millisecond Register
0x01E2 2074	C0TXIMAX	EMAC Control Module Interrupt Core 0 Transmit Interrupts Per Millisecond Register
0x01E2 2078	C1RXIMAX	EMAC Control Module Interrupt Core 1 Receive Interrupts Per Millisecond Register
0x01E2 207C	C1TXIMAX	EMAC Control Module Interrupt Core 1 Transmit Interrupts Per Millisecond Register
0x01E2 2080	C2RXIMAX	EMAC Control Module Interrupt Core 2 Receive Interrupts Per Millisecond Register
0x01E2 2084	C2TXIMAX	EMAC Control Module Interrupt Core 2 Transmit Interrupts Per Millisecond Register

Table 6-88. EMAC Control Module RAM

BYTE ADDRESS	DESCRIPTION
0x01E2 0000 - 0x01E2 1FFF	EMAC Local Buffer Descriptor Memory

6.21.1.1 EMAC Electrical Data/Timing

Table 6-89. Timing Requirements for MII_RXCLK (see Figure 6-46)

NO.			1.2V, 1.1V				1.0V		UNIT
			10 Mbps		100 Mbps		10 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(MII\_RXCLK)}$	Cycle time, MII_RXCLK	400		40		400		ns
2	$t_{w(MII\_RXCLKH)}$	Pulse duration, MII_RXCLK high	140		14		140		ns
3	$t_{w(MII\_RXCLKL)}$	Pulse duration, MII_RXCLK low	140		14		140		ns

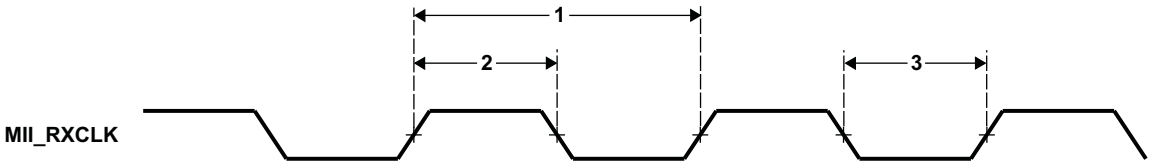

Figure 6-46. MII_RXCLK Timing (EMAC - Receive)

Table 6-90. Timing Requirements for MII_TXCLK (see Figure 6-46)

NO.	PARAMETER		1.2V, 1.1V				1.0V		UNIT
			10 Mbps		100 Mbps		10 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(MII\_TXCLK)}$	Cycle time, MII_TXCLK	400		40		400		ns
2	$t_{w(MII\_TXCLKH)}$	Pulse duration, MII_TXCLK high	140		14		140		ns
3	$t_{w(MII\_TXCLKL)}$	Pulse duration, MII_TXCLK low	140		14		140		ns

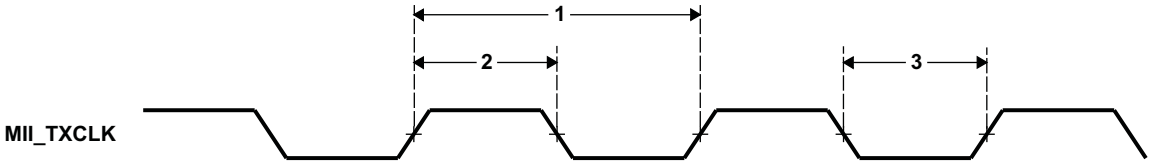

Figure 6-47. MII_TXCLK Timing (EMAC - Transmit)

Table 6-91. Timing Requirements for EMAC MII Receive 10/100 Mbit/s(1) (see Figure 6-48)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{su(MRXD-MII\_RXCLKH)}$	Setup time, receive selected signals valid before MII_RXCLK high	8		ns
2	$t_{h(MII\_RXCLKH-MRXD)}$	Hold time, receive selected signals valid after MII_RXCLK high	8		ns

(1) Receive selected signals include: MII_RXD[3]-MII_RXD[0], MII_RXDV, and MII_RXER.

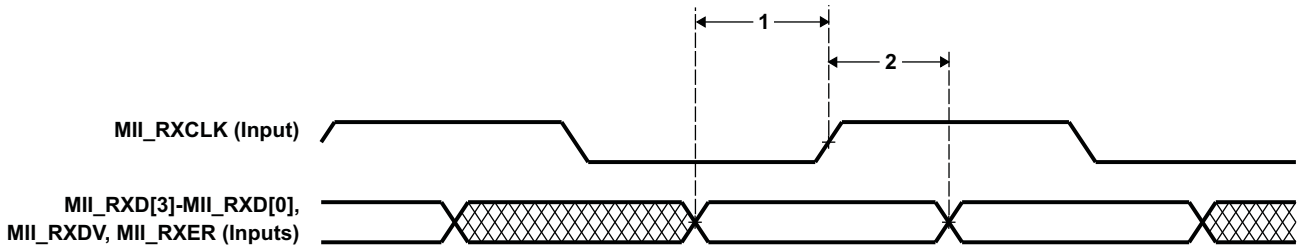

Figure 6-48. EMAC Receive Interface Timing

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Table 6-92. Switching Characteristics Over Recommended Operating Conditions for EMAC MII Transmit 10/100 Mbit/s(1) (see Figure 6-49)

NO.	PARAMETER		1.2V, 1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(MII\_TXCLKH-MTXD)}$	Delay time, MII_TXCLK high to transmit selected signals valid	2	25	2	32	ns

(1) Transmit selected signals include: MTXD3-MTXD0, and MII_TXEN.

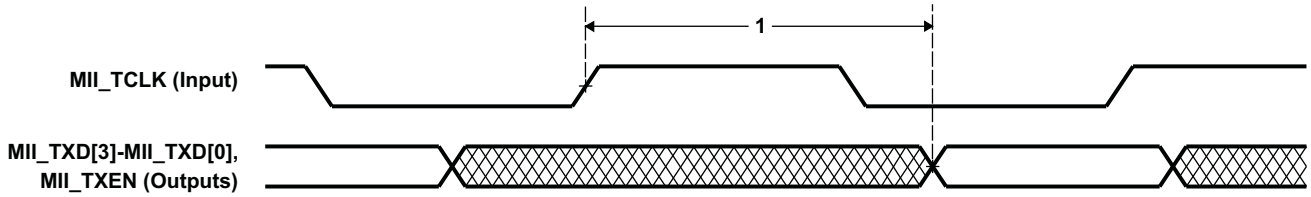

Figure 6-49. EMAC Transmit Interface Timing

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Table 6-93. Timing Requirements for EMAC RMII

NO.	PARAMETER		1.2V, 1.1V[1]			UNIT
			MIN	TYP	MAX	
1	tc(REFCLK)	Cycle Time, REF_CLK		20		ns
2	tw(REFCLKH)	Pulse Width, REF_CLK High	7		13	ns
3	tw(REFCLKL)	Pulse Width, REF_CLK Low	7		13	ns
6	tsu(RXD-REFCLK)	Input Setup Time, RXD Valid before REF_CLK High	4			ns
7	th(REFCLK-RXD)	Input Hold Time, RXD Valid after REF_CLK High	2			ns
8	tsu(CRSDV-REFCLK)	Input Setup Time, CRSDV Valid before REF_CLK High	4			ns
9	th(REFCLK-CRSDV)	Input Hold Time, CRSDV Valid after REF_CLK High	2			ns
10	tsu(RXER-REFCLK)	Input Setup Time, RXER Valid before REF_CLK High	4			ns
11	th(REFCLKR-RXER)	Input Hold Time, RXER Valid after REF_CLK High	2			ns

(1) RMII is not supported at operating points below 1.1V nominal.

Table 6-94. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII

NO.	PARAMETER		1.2V, 1.1V[1]			UNIT
			MIN	TYP	MAX	
4	td(REFCLK-TXD)	Output Delay Time, REF_CLK High to TXD Valid	2.5		13	ns
5	td(REFCLK-TXEN)	Output Delay Time, REF_CLK High to TXEN Valid	2.5		13	ns

(1) RMII is not supported at operating points below 1.1V nominal.

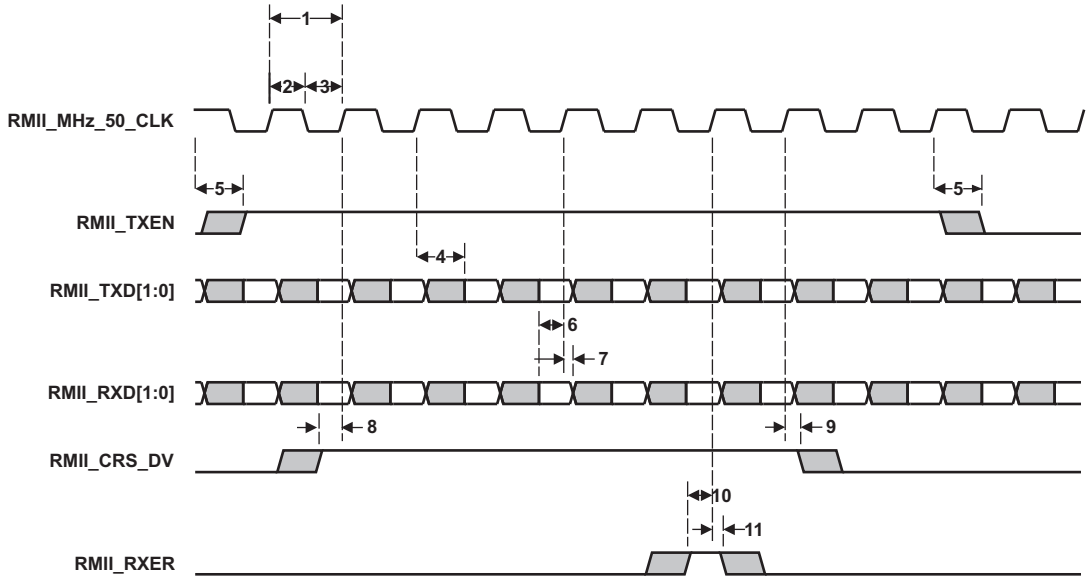

Figure 6-50. RMII Timing Diagram

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6.22 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time.

6.22.1 MDIO Registers

For a list of supported MDIO registers see Table 6-95 [MDIO Registers].

Table 6-95. MDIO Register Memory Map

BYTE ADDRESS	ACRONYM	REGISTER NAME
0x01E2 4000	REV	Revision Identification Register
0x01E2 4004	CONTROL	MDIO Control Register
0x01E2 4008	ALIVE	MDIO PHY Alive Status Register
0x01E2 400C	LINK	MDIO PHY Link Status Register
0x01E2 4010	LINKINTRAW	MDIO Link Status Change Interrupt (Unmasked) Register
0x01E2 4014	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register
0x01E2 4018	–	Reserved
0x01E2 4020	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register
0x01E2 4024	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register
0x01E2 4028	USERINTMASKSET	MDIO User Command Complete Interrupt Mask Set Register
0x01E2 402C	USERINTMASKCLEAR	MDIO User Command Complete Interrupt Mask Clear Register
0x01E2 4030 - 0x01E2 407C	–	Reserved
0x01E2 4080	USERACCESS0	MDIO User Access Register 0
0x01E2 4084	USERPHYSEL0	MDIO User PHY Select Register 0
0x01E2 4088	USERACCESS1	MDIO User Access Register 1
0x01E2 408C	USERPHYSEL1	MDIO User PHY Select Register 1
0x01E2 4090 - 0x01E2 47FF	–	Reserved

6.22.2 Management Data Input/Output (MDIO) Electrical Data/Timing

Table 6-96. Timing Requirements for MDIO Input (see Figure 6-51 and Figure 6-52)

NO.			1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{c(MDCLK)}$	Cycle time, MDCLK	400		ns
2	$t_{w(MDCLK)}$	Pulse duration, MDCLK high/low	180		ns
3	$t_{t(MDCLK)}$	Transition time, MDCLK		5	ns
4	$t_{su(MDIO-MDCLKH)}$	Setup time, MDIO data input valid before MDCLK high	10		ns
5	$t_{h(MDCLKH-MDIO)}$	Hold time, MDIO data input valid after MDCLK high	10		ns

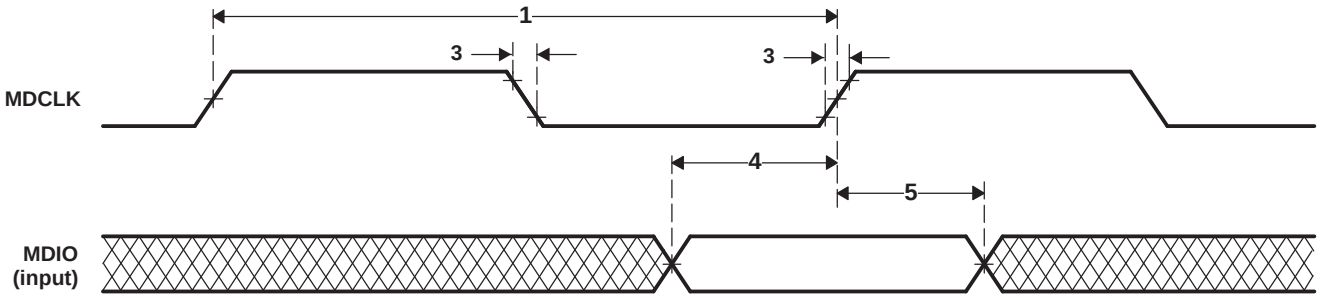

Figure 6-51. MDIO Input Timing

Table 6-97. Switching Characteristics Over Recommended Operating Conditions for MDIO Output (see Figure 6-52)

NO.			MIN	MAX	UNIT
7	$t_{d(MDCLKL-MDIO)}$	Delay time, MDCLK low to MDIO data output valid	0	100	ns

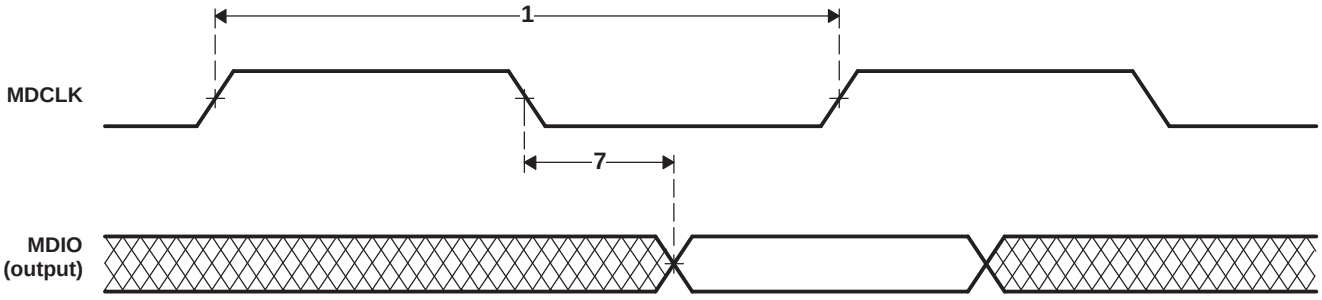

Figure 6-52. MDIO Output Timing

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6.23 LCD Controller (LCDC)

Table 6-98 lists the LCD Controller registers.

Table 6-98. LCD Controller Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 3000	REVID	LCD Revision Identification Register
0x01E1 3004	LCD_CTRL	LCD Control Register
0x01E1 3008	LCD_STAT	LCD Status Register
0x01E1 300C	LIDD_CTRL	LCD LIDD Control Register
0x01E1 3010	LIDD_CS0_CONF	LCD LIDD CS0 Configuration Register
0x01E1 3014	LIDD_CS0_ADDR	LCD LIDD CS0 Address Read/Write Register
0x01E1 3018	LIDD_CS0_DATA	LCD LIDD CS0 Data Read/Write Register
0x01E1 301C	LIDD_CS1_CONF	LCD LIDD CS1 Configuration Register
0x01E1 3020	LIDD_CS1_ADDR	LCD LIDD CS1 Address Read/Write Register
0x01E1 3024	LIDD_CS1_DATA	LCD LIDD CS1 Data Read/Write Register
0x01E1 3028	RASTER_CTRL	LCD Raster Control Register
0x01E1 302C	RASTER_TIMING_0	LCD Raster Timing 0 Register
0x01E1 3030	RASTER_TIMING_1	LCD Raster Timing 1 Register
0x01E1 3034	RASTER_TIMING_2	LCD Raster Timing 2 Register
0x01E1 3038	RASTER_SUBPANEL	LCD Raster Subpanel Display Register
0x01E1 3040	LCDDMA_CTRL	LCD DMA Control Register
0x01E1 3044	LCDDMA_FB0_BASE	LCD DMA Frame Buffer 0 Base Address Register
0x01E1 3048	LCDDMA_FB0_CEILING	LCD DMA Frame Buffer 0 Ceiling Address Register
0x01E1 304C	LCDDMA_FB1_BASE	LCD DMA Frame Buffer 1 Base Address Register
0x01E1 3050	LCDDMA_FB1_CEILING	LCD DMA Frame Buffer 1 Ceiling Address Register

6.23.1 LCD Interface Display Driver (LIDD Mode)

Table 6-99. Timing Requirements for LCD LIDD Mode (1)

NO.	PARAMETER		1.2V, 1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	
16	$t_{su(LCD\_D)}$	Setup time, LCD_D[15:0] valid before LCD_CLK (SYSCLK2) high	7		8		ns
17	$t_{h(LCD\_D)}$	Hold time, LCD_D[15:0] valid after LCD_CLK (SYSCLK2) high	0		0		ns

(1) Over operating free-air temperature range (unless otherwise noted)

Table 6-100. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode

NO.	PARAMETER		1.2V, 1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] valid (write)	0	7	0	9	ns
5	$t_{d(LCD\_D\_I)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] invalid (write)	0	7	0	9	ns
6	$t_{d(LCD\_E\_A)}$	Delay time, LCD_CLK (SYSCLK2) high to $\overline{\text{LCD\_AC\_ENB\_CS}}$ low	0	7	0	9	ns
7	$t_{d(LCD\_E\_I)}$	Delay time, LCD_CLK (SYSCLK2) high to $\overline{\text{LCD\_AC\_ENB\_CS}}$ high	0	7	0	9	ns
8	$t_{d(LCD\_A\_A)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC low	0	7	0	9	ns
9	$t_{d(LCD\_A\_I)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC high	0	7	0	9	ns
10	$t_{d(LCD\_W\_A)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC low	0	7	0	9	ns
11	$t_{d(LCD\_W\_I)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC high	0	7	0	9	ns
12	$t_{d(LCD\_STRB\_A)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_PCLK high	0	7	0	9	ns
13	$t_{d(LCD\_STRB\_I)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_PCLK low	0	7	0	9	ns
14	$t_{d(LCD\_D\_Z)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] in 3-state	0	7	0	9	ns
15	$t_{d(Z\_LCD\_D)}$	Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] (valid from 3-state)	0	7	0	9	ns

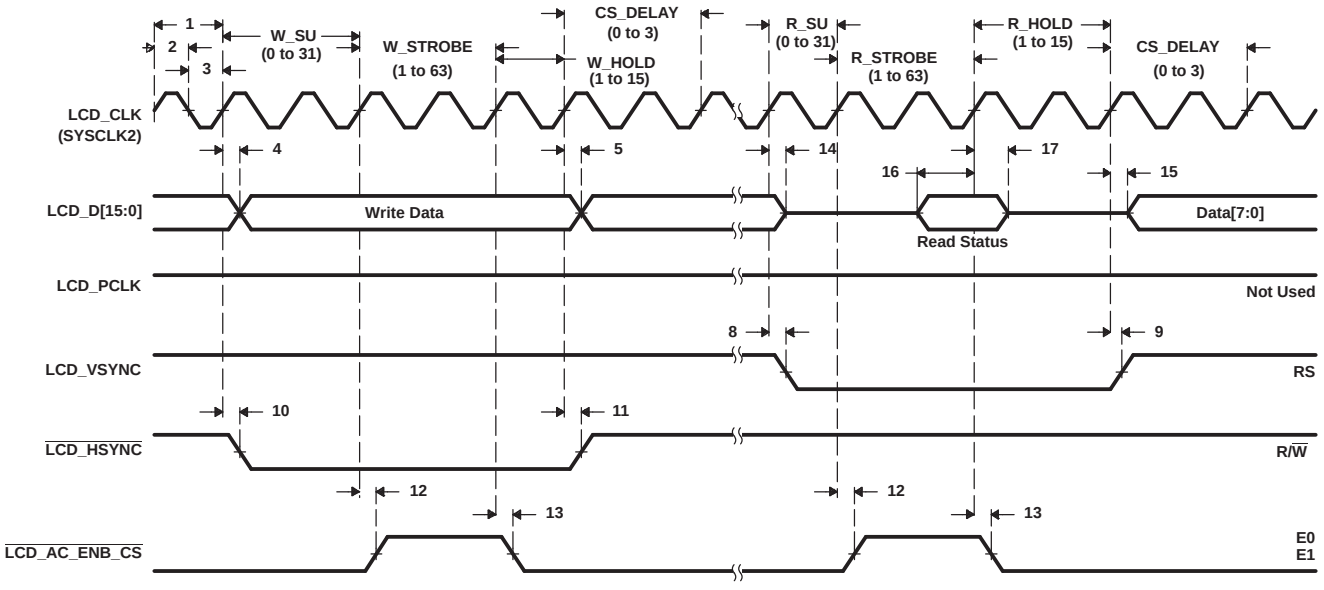

Figure 6-53. Character Display HD44780 Write

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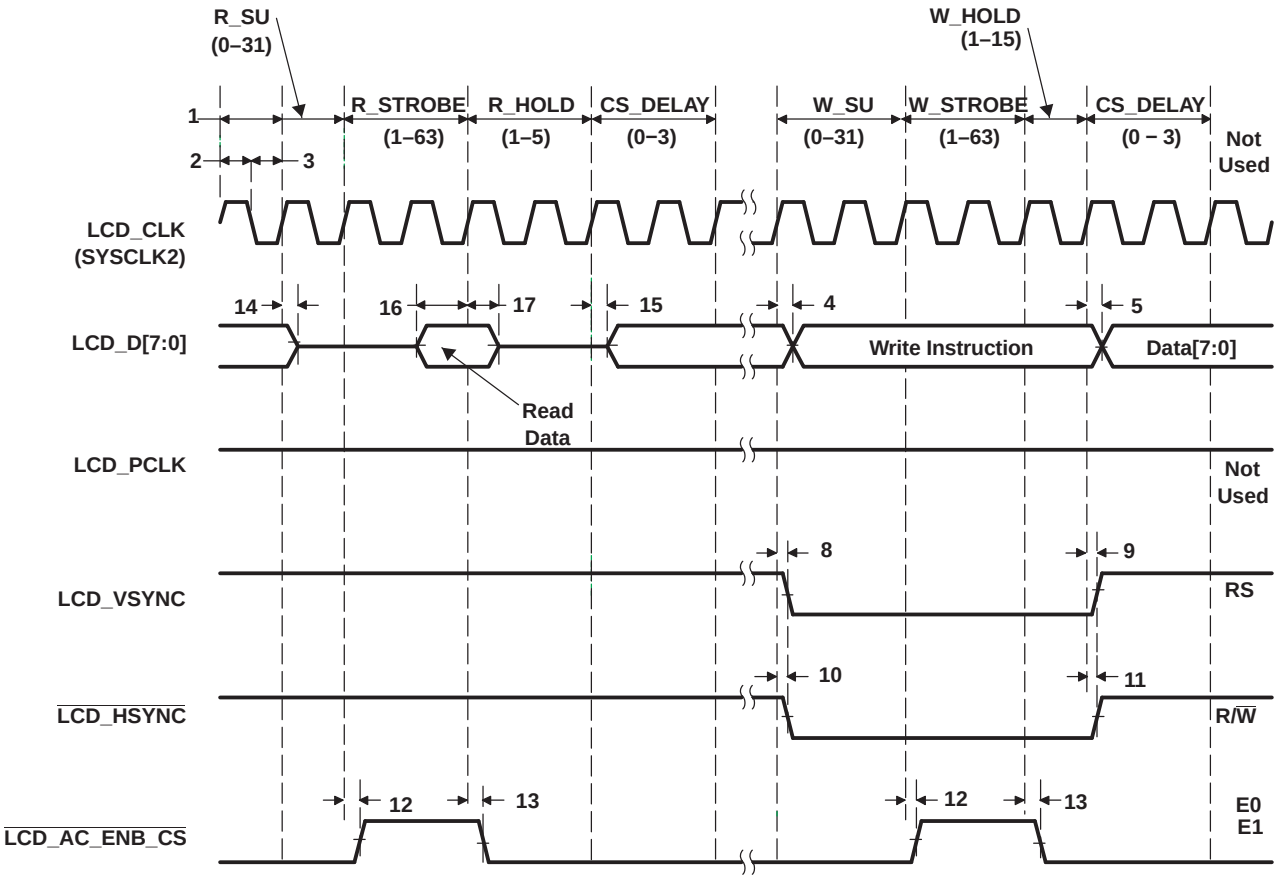

Figure 6-54. Character Display HD44780 Read

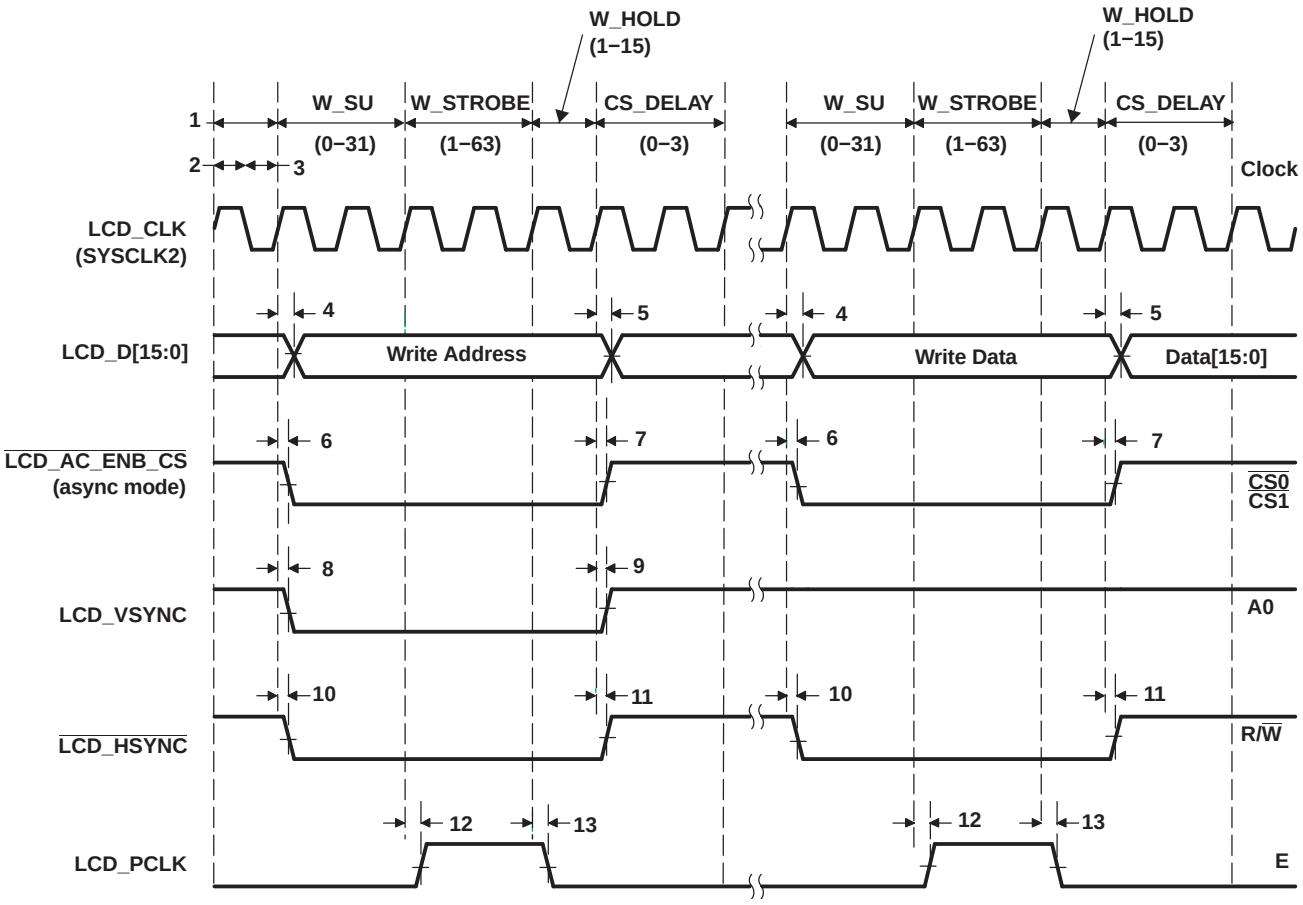

Figure 6-55. Micro-Interface Graphic Display 6800 Write

PRODUCT PREVIEW

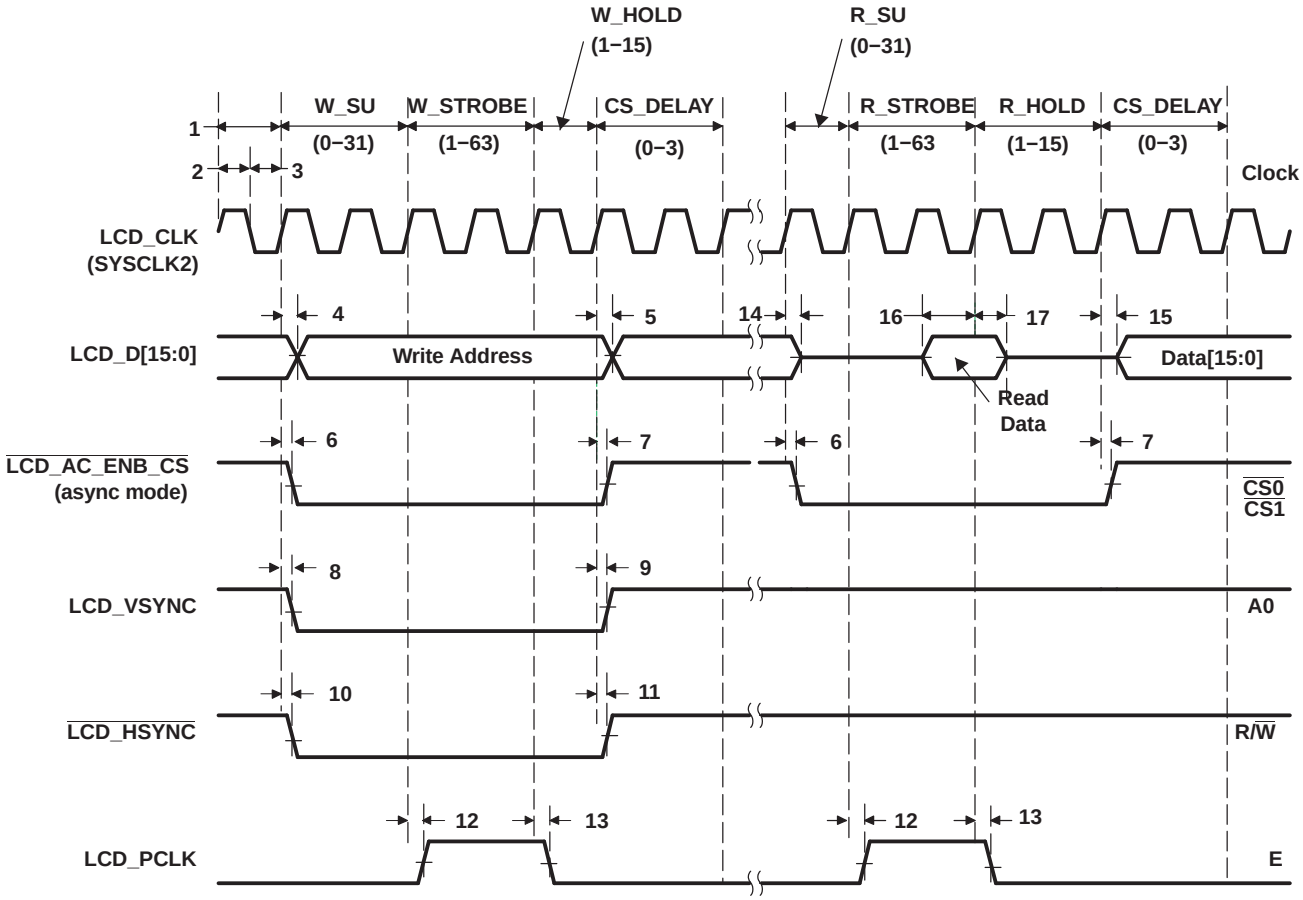

Figure 6-56. Micro-Interface Graphic Display 6800 Read

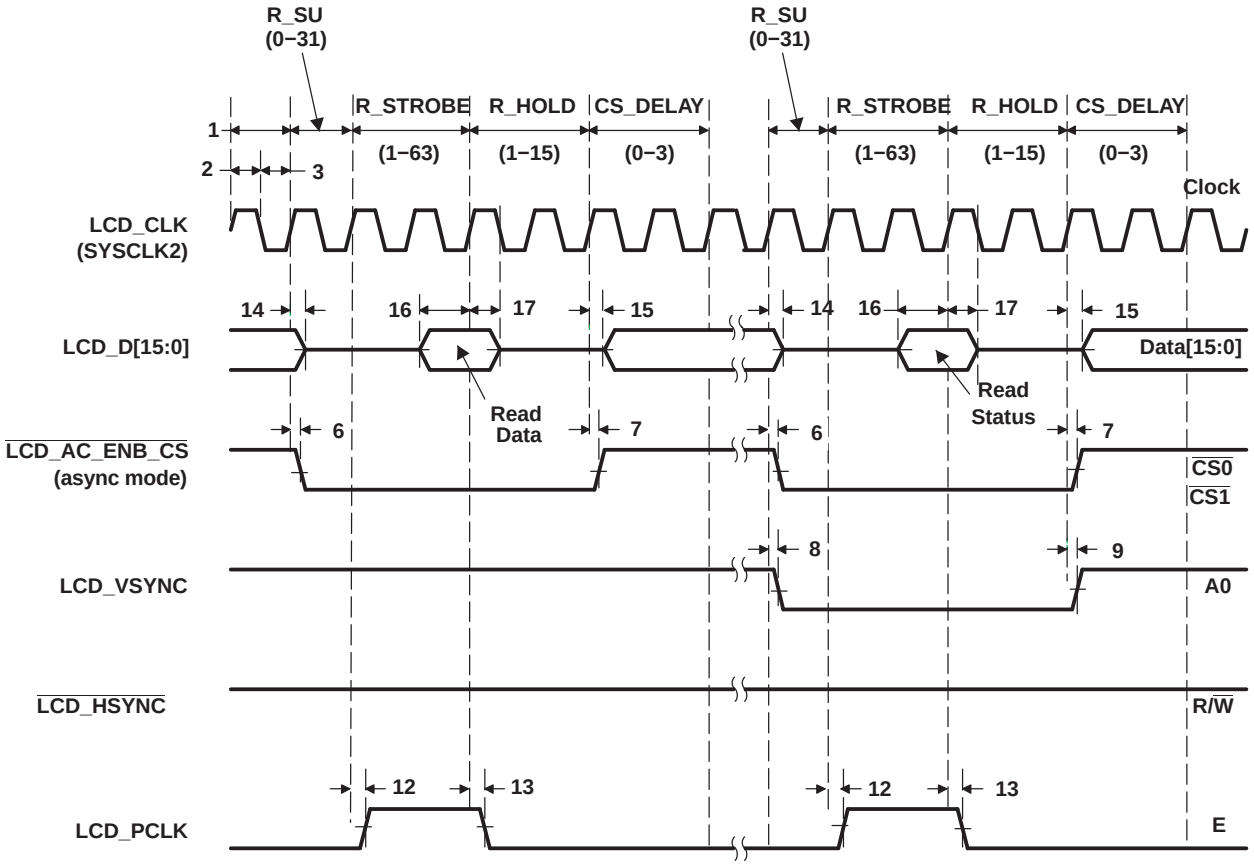

Figure 6-57. Micro-Interface Graphic Display 6800 Status

PRODUCT PREVIEW

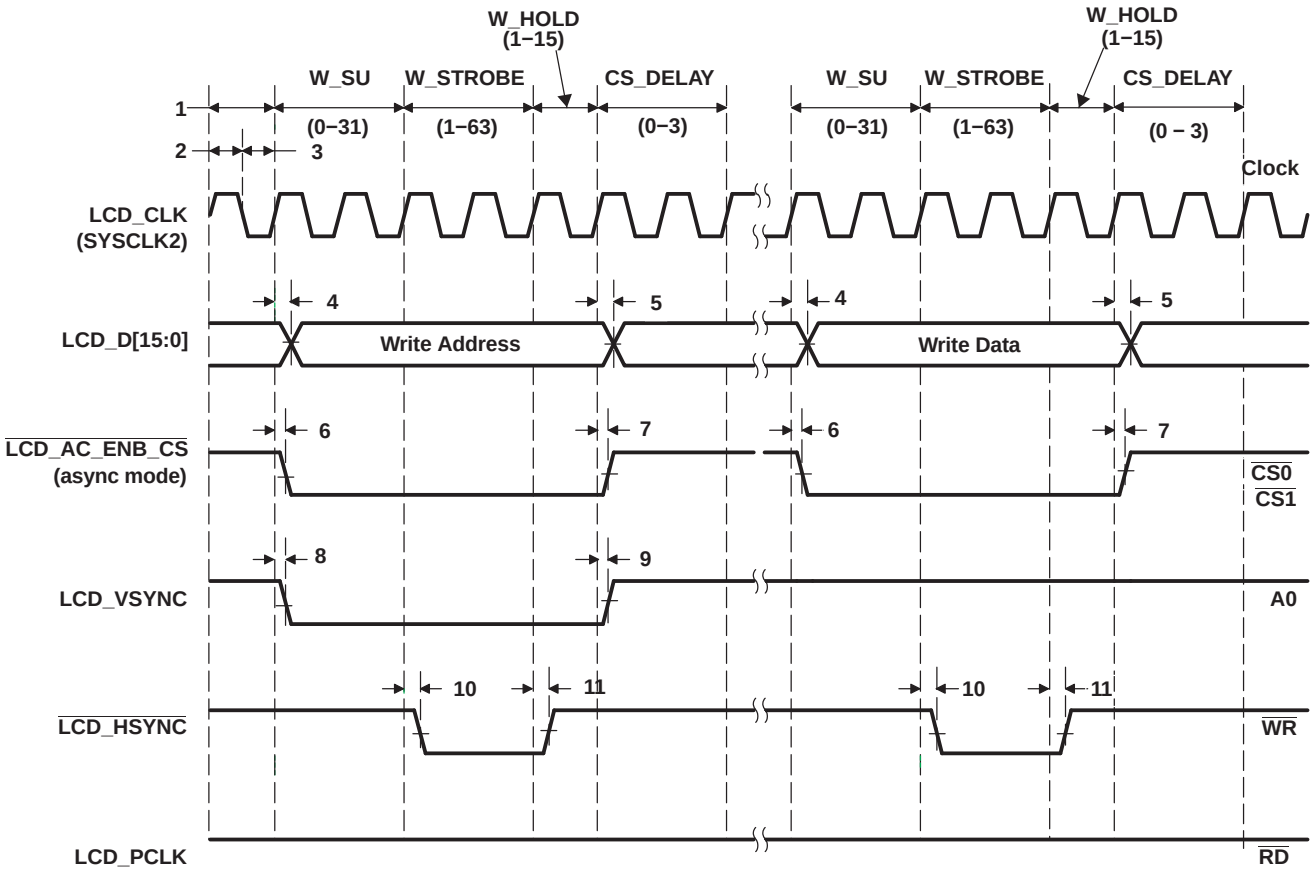

Figure 6-58. Micro-Interface Graphic Display 8080 Write

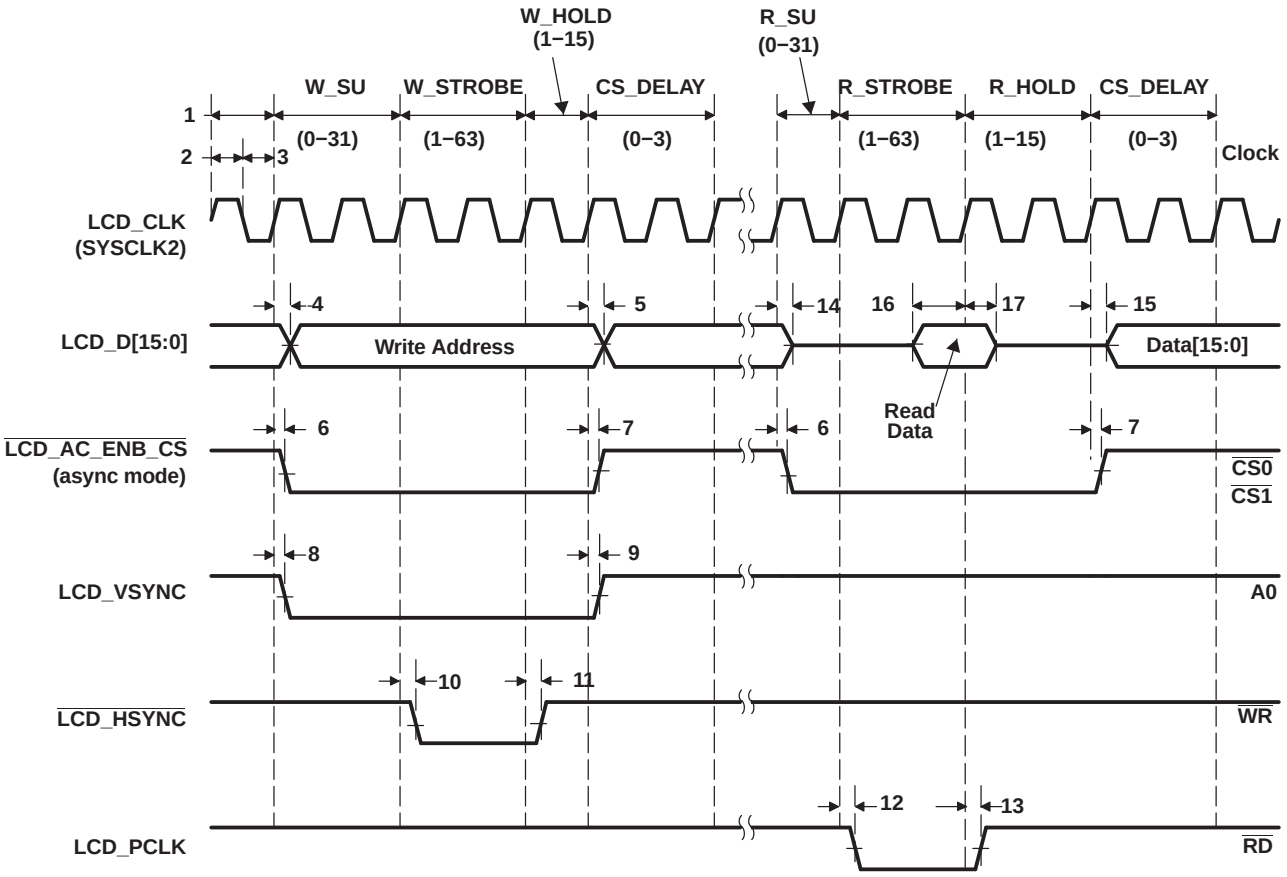

Figure 6-59. Micro-Interface Graphic Display 8080 Read

PRODUCT PREVIEW

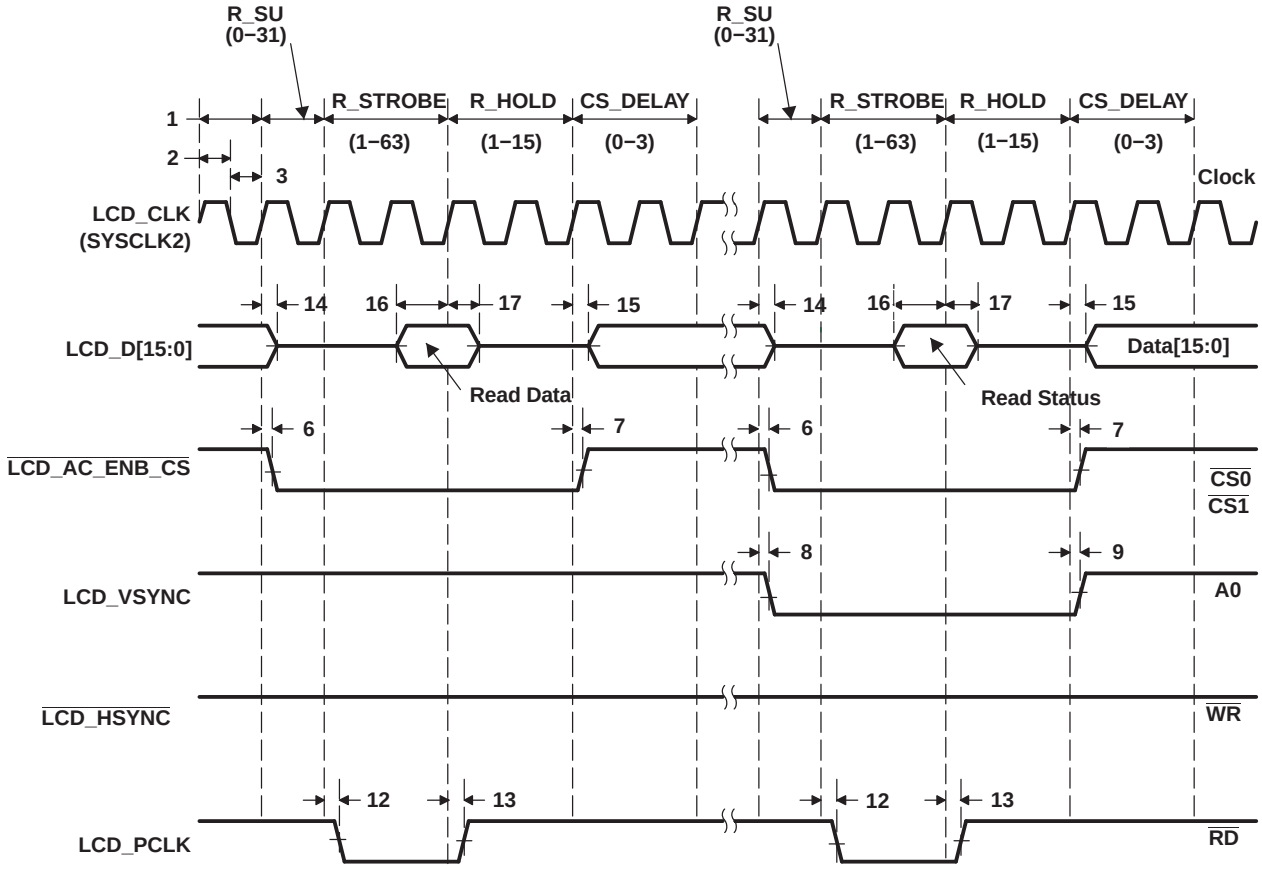

Figure 6-60. Micro-Interface Graphic Display 8080 Status

6.23.2 LCD Raster Mode

Table 6-101. Switching Characteristics Over Recommended Operating Conditions for LCD Raster Mode

See Figure 6-61 through Figure 6-65

NO.	PARAMETER		1.2V, 1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	
	$f_{clock(PIXEL\_CLK)}$	Clock frequency, pixel clock		F/2 (1)		F/2 (1)	MHz
1	$t_{c(PIXEL\_CLK)}$	Cycle time, pixel clock	26.66		33.33		ns
2	$t_{w(PIXEL\_CLK\_H)}$	Pulse duration, pixel clock high	10		10		ns
3	$t_{w(PIXEL\_CLK\_L)}$	Pulse duration, pixel clock low	10		10		ns
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_PCLK high to LCD_D[15:0] valid (write)	0	7	0	9	ns
5	$t_{d(LCD\_D\_IV)}$	Delay time, LCD_PCLK high to LCD_D[15:0] invalid (write)	0	7	0	9	ns
6	$t_{d(\overline{LCD\_AC\_ENB\_CS\_A})}$	Delay time, LCD_PCLK low to $\overline{LCD\_AC\_ENB\_CS}$ high	0	7	0	9	ns
7	$t_{d(\overline{LCD\_AC\_ENB\_CS\_I})}$	Delay time, LCD_PCLK low to $\overline{LCD\_AC\_ENB\_CS}$ high	0	7	0	9	ns
8	$t_{d(LCD\_VSYNC\_A)}$	Delay time, LCD_PCLK low to LCD_VSYNC high	0	7	0	9	ns
9	$t_{d(LCD\_VSYNC\_I)}$	Delay time, LCD_PCLK low to LCD_VSYNC low	0	7	0	9	ns
10	$t_{d(LCD\_HSYNC\_A)}$	Delay time, LCD_PCLK high to LCD_HSYNC high	0	7	0	9	ns
11	$t_{d(LCD\_HSYNC\_I)}$	Delay time, LCD_PCLK high to LCD_HSYNC low	0	7	0	9	ns

(1) F = frequency of LCD_PCLK in ns

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPL)

$\overline{LCD\_AC\_ENB\_CS}$ timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

The display format produced in raster mode is shown in Figure 6-61. An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC. The beginning of each new line is denoted by the activation of I/O signal LCD_HSYNC.

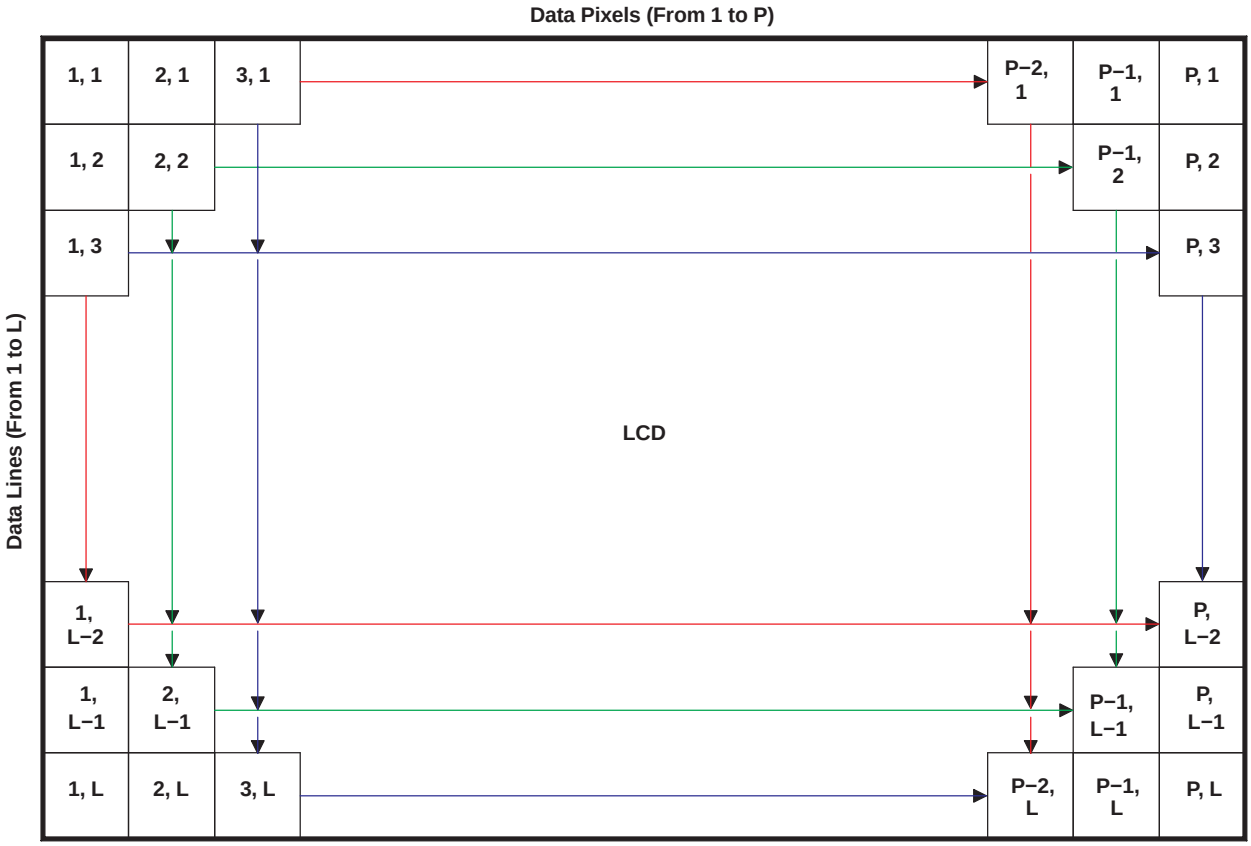

Figure 6-61. LCD Raster-Mode Display Format

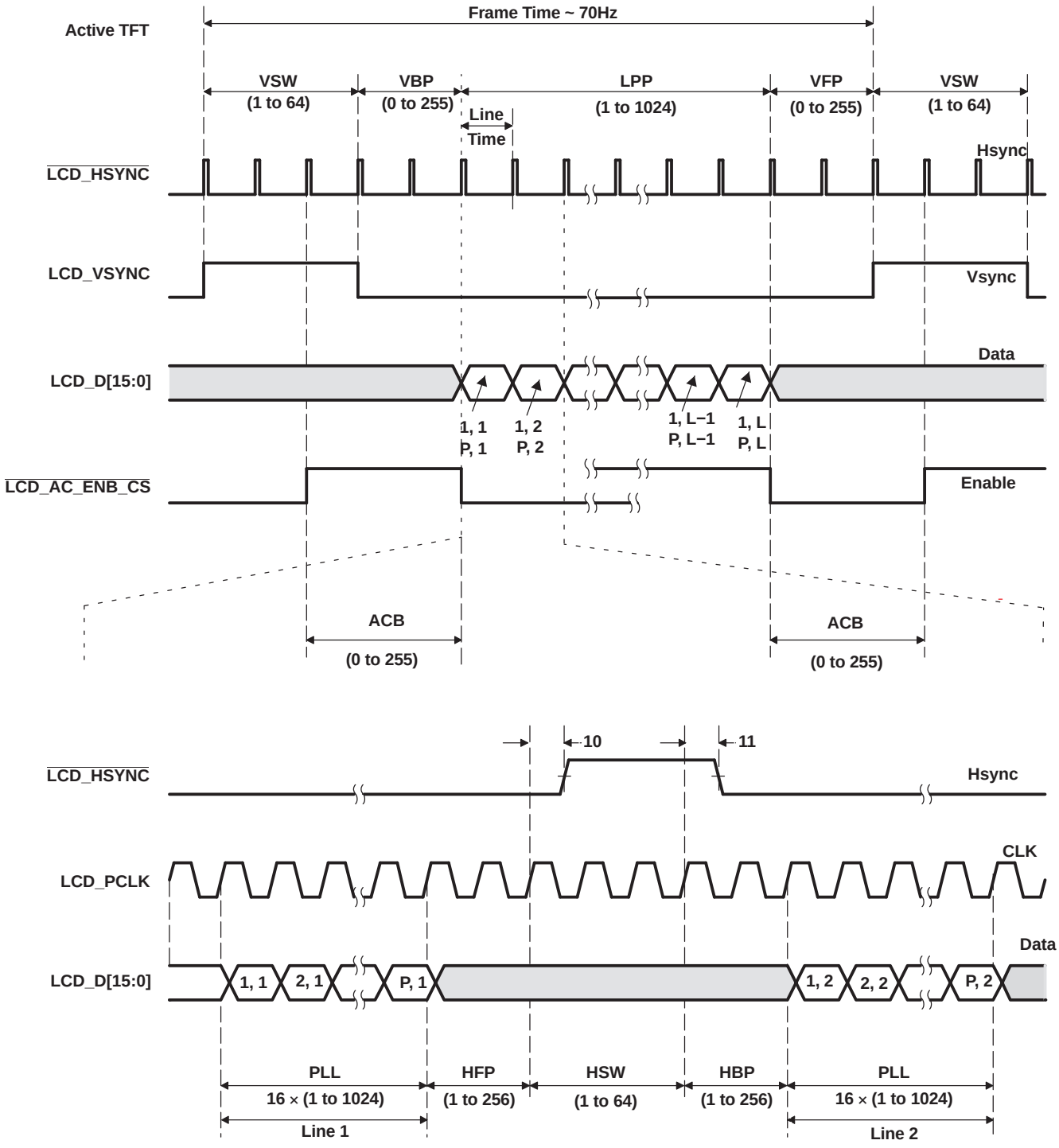

Figure 6-62. LCD Raster-Mode Active

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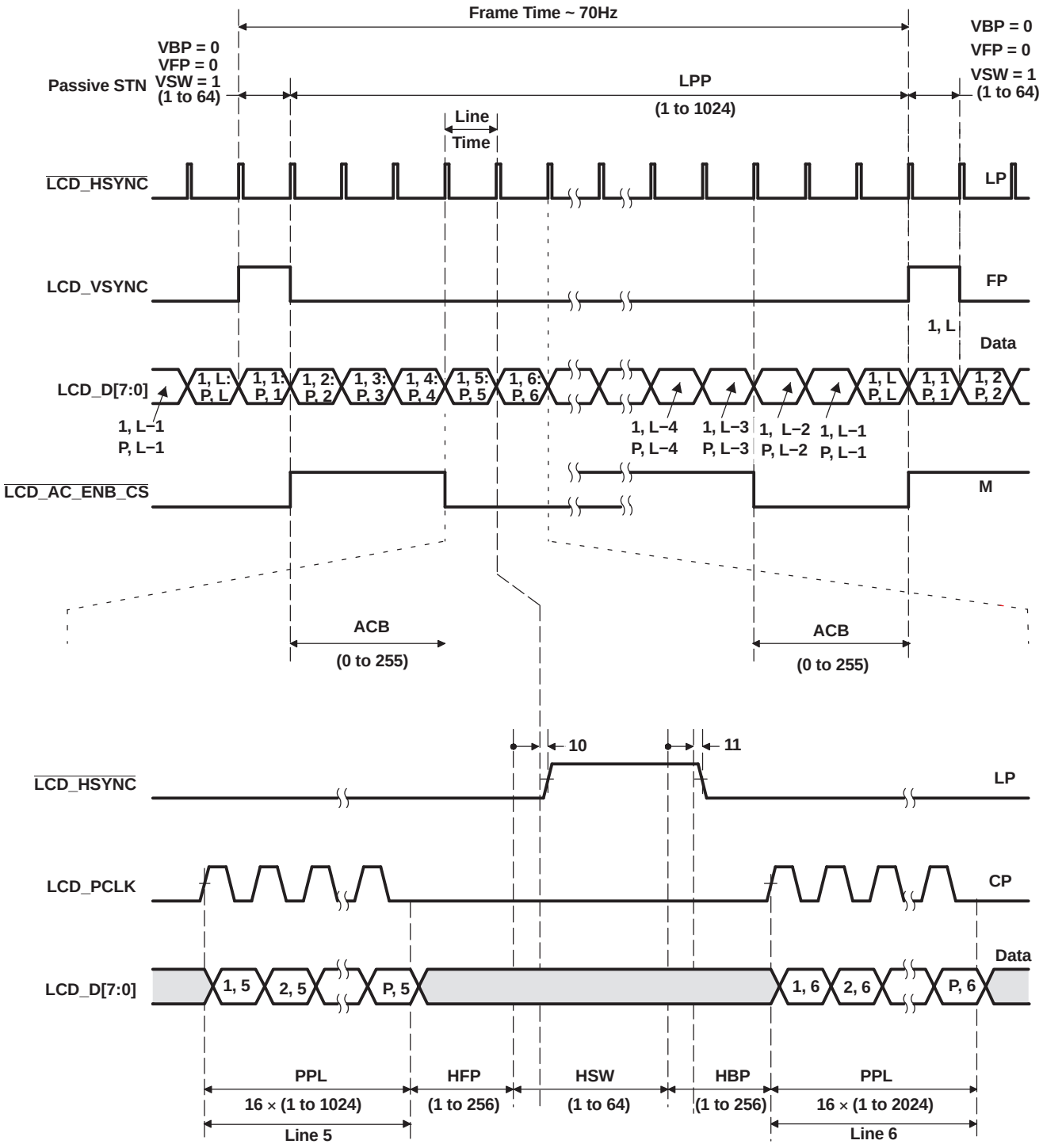

Figure 6-63. LCD Raster-Mode Passive

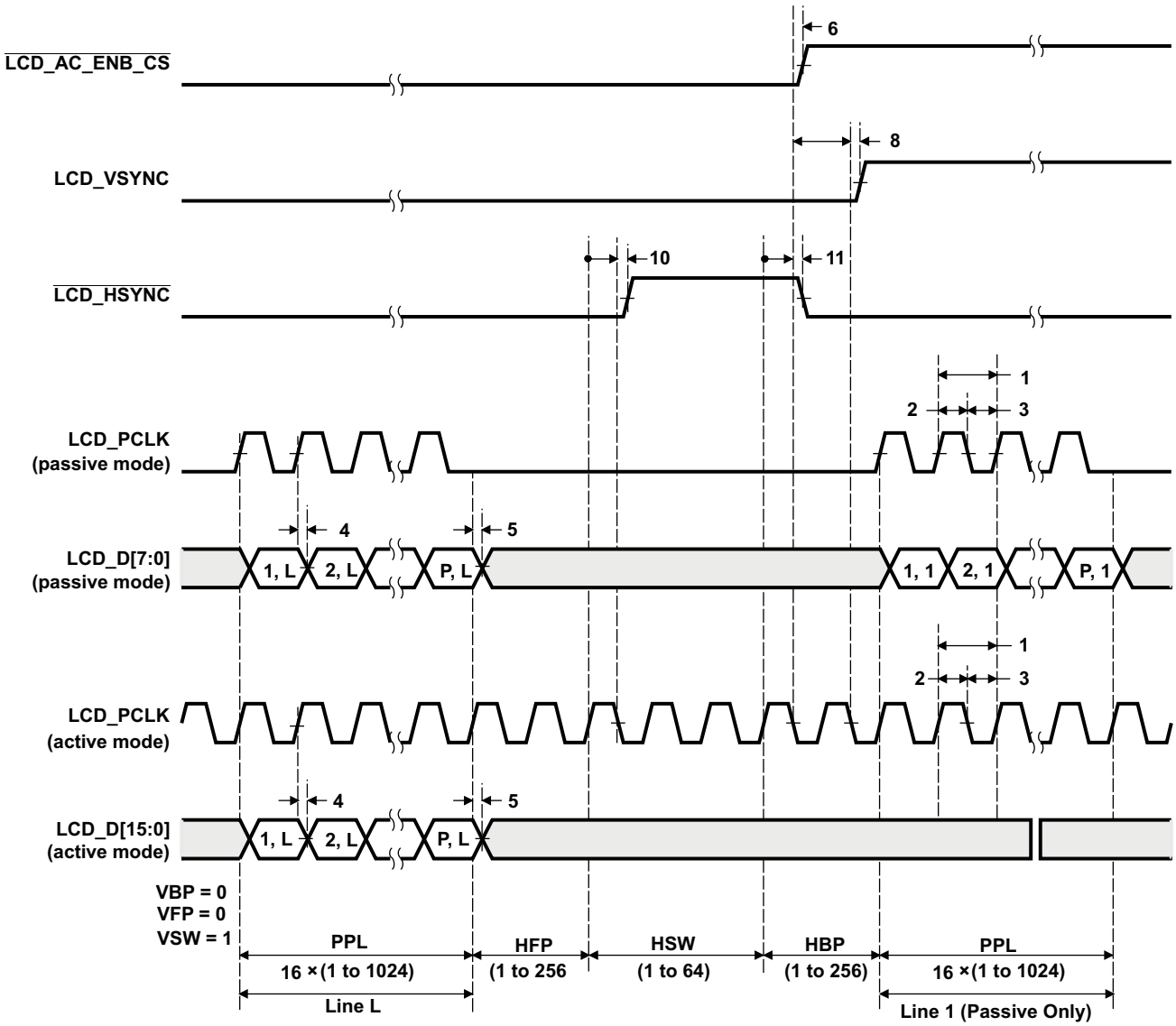

Figure 6-64. LCD Raster-Mode Control Signal Activation

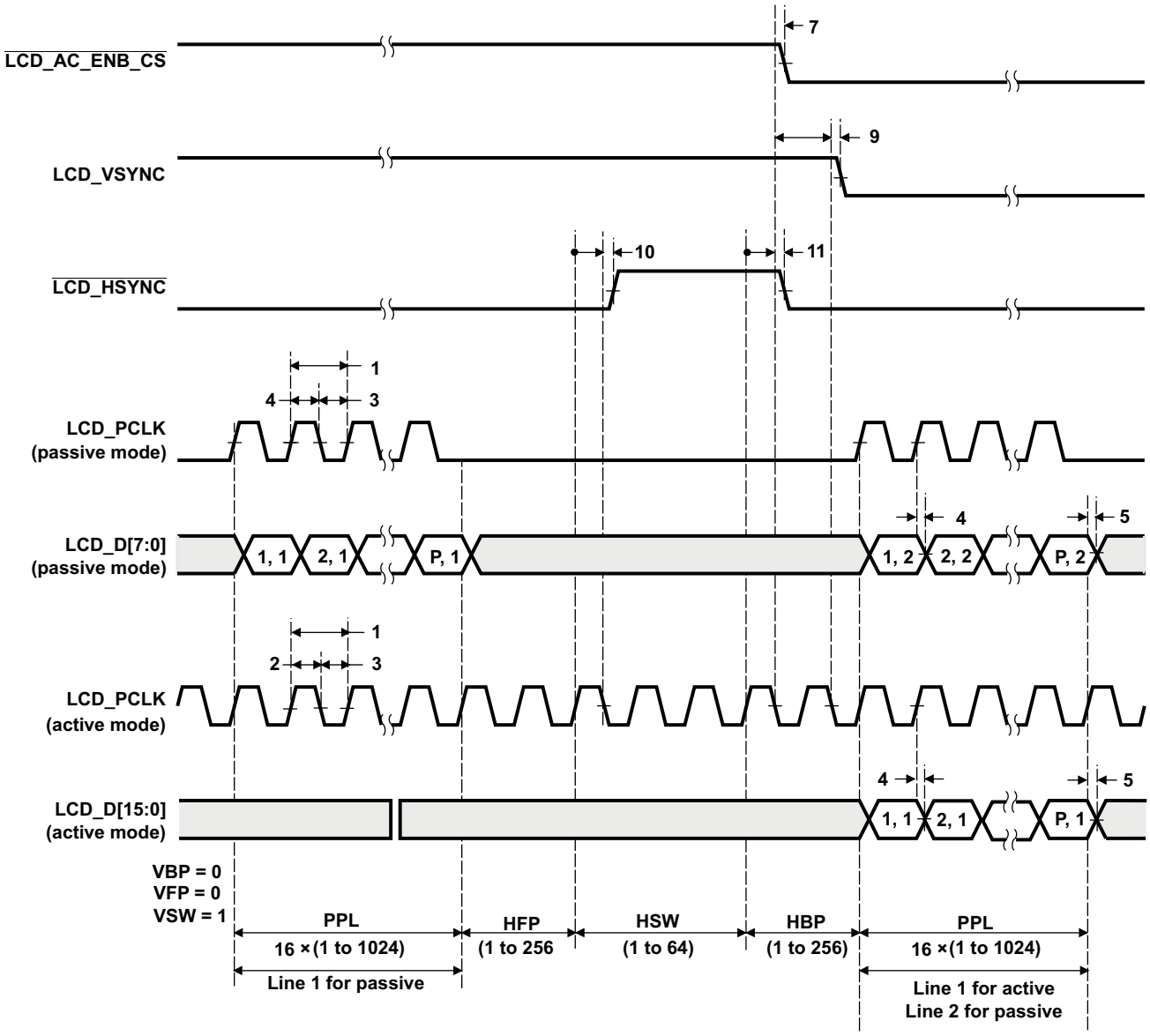

Figure 6-65. LCD Raster-Mode Control Signal Deactivation

6.24 Host-Port Interface (UHPI)

6.24.1 HPI Device-Specific Information

The device includes a user-configurable 16-bit Host-port interface (HPI16).

6.24.2 HPI Peripheral Register Description(s)

Table 6-102. HPI Control Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION	COMMENTS
0x01E1 0000	PID	Peripheral Identification Register	
0x01E1 0004	PWREMU_MGMT	HPI power and emulation management register	The CPU has read/write access to the PWREMU_MGMT register.
0x01E1 0008	-	Reserved	
0x01E1 000C	GPIO_EN	General Purpose IO Enable Register	
0x01E1 0010	GPIO_DIR1	General Purpose IO Direction Register 1	
0x01E1 0014	GPIO_DAT1	General Purpose IO Data Register 1	
0x01E1 0018	GPIO_DIR2	General Purpose IO Direction Register 2	
0x01E1 001C	GPIO_DAT2	General Purpose IO Data Register 2	
0x01E1 0020	GPIO_DIR3	General Purpose IO Direction Register 3	
0x01E1 0024	GPIO_DAT3	General Purpose IO Data Register 3	
01E1 0028	-	Reserved	
01E1 002C	-	Reserved	
01E1 0030	HPIC	HPI control register	The Host and the CPU both have read/write access to the HPIC register.
01E1 0034	HPIA (HPIAW)(1)	HPI address register (Write)	The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers.
01E1 0038	HPIA (HPIAR)(1)	HPI address register (Read)	
01E1 000C - 01E1 07FF	-	Reserved	

(1) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the Host. The CPU can access HPIAW and HPIAR independently.

6.24.3 HPI Electrical Data/Timing

Table 6-103. Timing Requirements for Host-Port Interface [1.2V, 1.1V][(1)(2)]

NO.			1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals[(3)] valid before $\overline{\text{UHPI\_HSTROBE}}$ low	5		ns
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals[(3)] valid after $\overline{\text{UHPI\_HSTROBE}}$ low	2		ns
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{\text{UHPI\_HSTROBE}}$ active low	15		ns
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{\text{UHPI\_HSTROBE}}$ inactive high between consecutive accesses	2M		ns
9	$t_{su(SELV-HASL)}$	Setup time, selects signals valid before $\overline{\text{UHPI\_HAS}}$ low	5		
10	$t_{h(HASL-SELV)}$	Hold time, select signals valid after $\overline{\text{UHPI\_HAS}}$ low	2		
11	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{\text{UHPI\_HSTROBE}}$ high	5		ns
12	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{\text{UHPI\_HSTROBE}}$ high	2		ns
13	$t_{h(HRDYL-HSTBH)}$	Hold time, $\overline{\text{UHPI\_HSTROBE}}$ high after $\overline{\text{UHPI\_HRDY}}$ low. $\overline{\text{UHPI\_HSTROBE}}$ should not be inactivated until $\overline{\text{UHPI\_HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	2		ns
16	$t_{su(HASL-HSTBL)}$	Setup time, $\overline{\text{UHPI\_HAS}}$ low before $\overline{\text{UHPI\_HSTROBE}}$ low	5		
17	$t_{h(HSTBL-HASH)}$	Hold time, $\overline{\text{UHPI\_HAS}}$ low after $\overline{\text{UHPI\_HSTROBE}}$ low	2		

(1) $\overline{\text{UHPI\_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI\_HCS}}$, $\overline{\text{UHPI\_HDS1}}$, and $\overline{\text{UHPI\_HDS2}}$: [NOT($\overline{\text{UHPI\_HDS1}}$ XOR $\overline{\text{UHPI\_HDS2}}$)] OR $\overline{\text{UHPI\_HCS}}$.
(2) M=SYSCLK2 period (CPU clock frequency)/2 in ns. For example, when running parts at 300 MHz, use M=6.67 ns.
(3) Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$ and HHWIL.

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Table 6-104. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.2V, 1.1V](1)(2)(3)

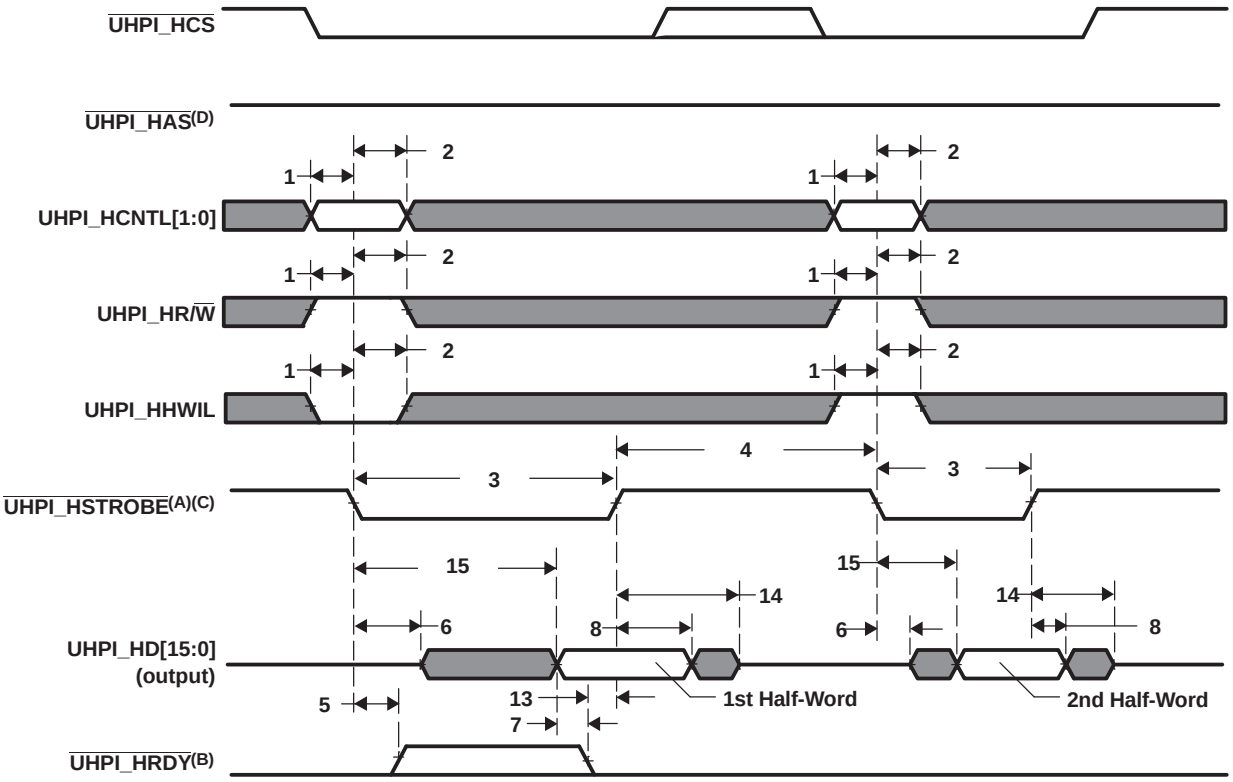
NO.	PARAMETER			1.2V		1.1V		UNIT
				MIN	MAX	MIN	MAX	
5	$t_{d(HSTBL-HRDYV)}$	Delay time, HSTROBE low to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: Back-to-back HPIA writes (can be either first or second half-word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word) *Case 4*: HPIA write and Write FIFO not empty For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions: *Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access) *Case 2*: First half-word access of HPID Read without auto-increment For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions: *Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access) *Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half-word access)		15		17	ns
5a	$t_{d(HASL-HRDYV)}$	Delay time, HAS low to HRDY valid			15		17	
6	$t_{en(HSTBL-HDLZ)}$	Enable time, HD driven from HSTROBE low		1.5		1.5		ns
7	$t_{d(HRDYL-HDV)}$	Delay time, HRDY low to HD valid			0		0	ns
8	$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE high		1.5		1.5		ns
14	$t_{dis(HSTBH-HDHZ)}$	Disable time, HD high-impedance from HSTROBE high			15		17	ns
15	$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid	For HPI Read. Applies to conditions where data is already residing in HPID/FIFO: *Case 1*: HPIC or HPIA read *Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO *Case 3*: Second half-word of HPID read with or without auto-increment		15		17	ns
18	$t_{d(HSTBH-HRDYV)}$	Delay time, HSTROBE high to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: HPID write when Write FIFO is full (can happen to either half-word) *Case 2*: HPIA write (can happen to either half-word) *Case 3*: HPID write without auto-increment (only happens to second half-word)		15		17	ns

(1) M=SYSCLK2 period (CPU clock frequency)/2 in ns. For example, when running parts at 300 MHz, use M=6.67 ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).

Table 6-105. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.0V](1)(2)(3)

NO.	PARAMETER			1.0V MIN	1.0V MAX	UNIT
5	$t_{d(HSTBL-HRDYV)}$	Delay time, HSTROBE low to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: Back-to-back HPIA writes (can be either first or second half-word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word) *Case 4*: HPIA write and Write FIFO not empty For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions: *Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access) *Case 2*: First half-word access of HPID Read without auto-increment For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions: *Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access) *Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half-word access)		22	ns
5a	$t_{d(HASL-HRDYV)}$	Delay time, HAS low to HRDY valid			22	
6	$t_{en(HSTBL-HDLZ)}$	Enable time, HD driven from HSTROBE low		1.5		ns
7	$t_{d(HRDYL-HDV)}$	Delay time, HRDY low to HD valid			0	ns
8	$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE high		1.5		ns
14	$t_{dis(HSTBH-HDHZ)}$	Disable time, HD high-impedance from HSTROBE high			22	ns
15	$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid	For HPI Read. Applies to conditions where data is already residing in HPID/FIFO: *Case 1*: HPIC or HPIA read *Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO *Case 3*: Second half-word of HPID read with or without auto-increment		22	ns
18	$t_{d(HSTBH-HRDYV)}$	Delay time, HSTROBE high to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: HPID write when Write FIFO is full (can happen to either half-word) *Case 2*: HPIA write (can happen to either half-word) *Case 3*: HPID write without auto-increment (only happens to second half-word)		22	ns

(1) M=SYSCLK2 period (CPU clock frequency)/2 in ns. For example, when running parts at 300 MHz, use M=6.67 ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).



A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing)and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

Figure 6-66. UHPI Read Timing (HAS Not Used, Tied High)

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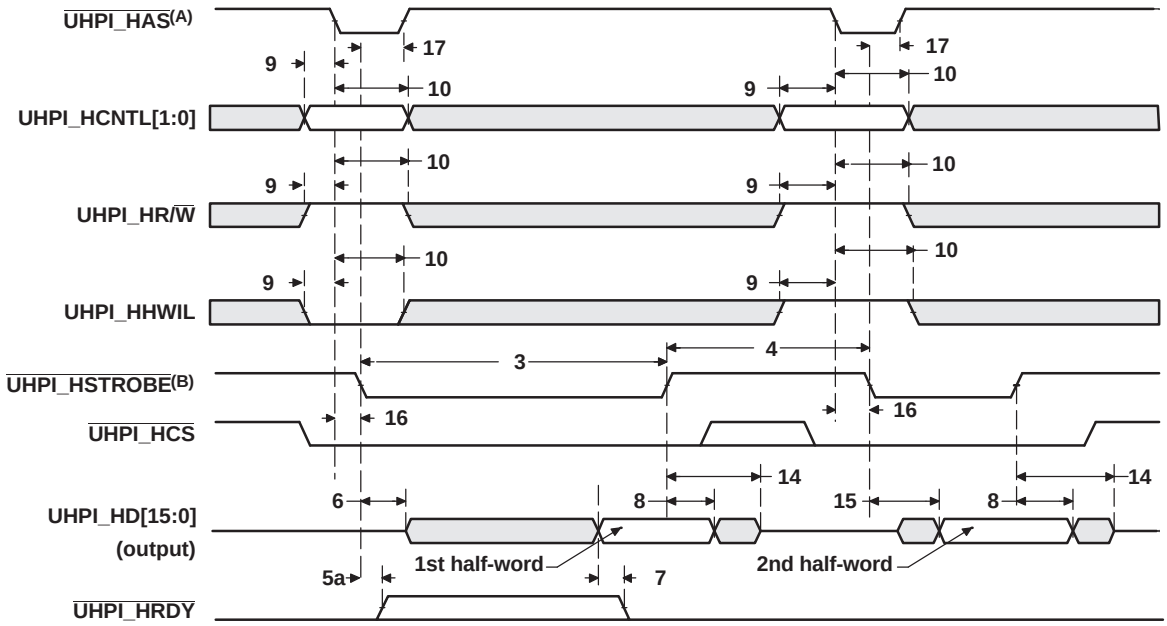
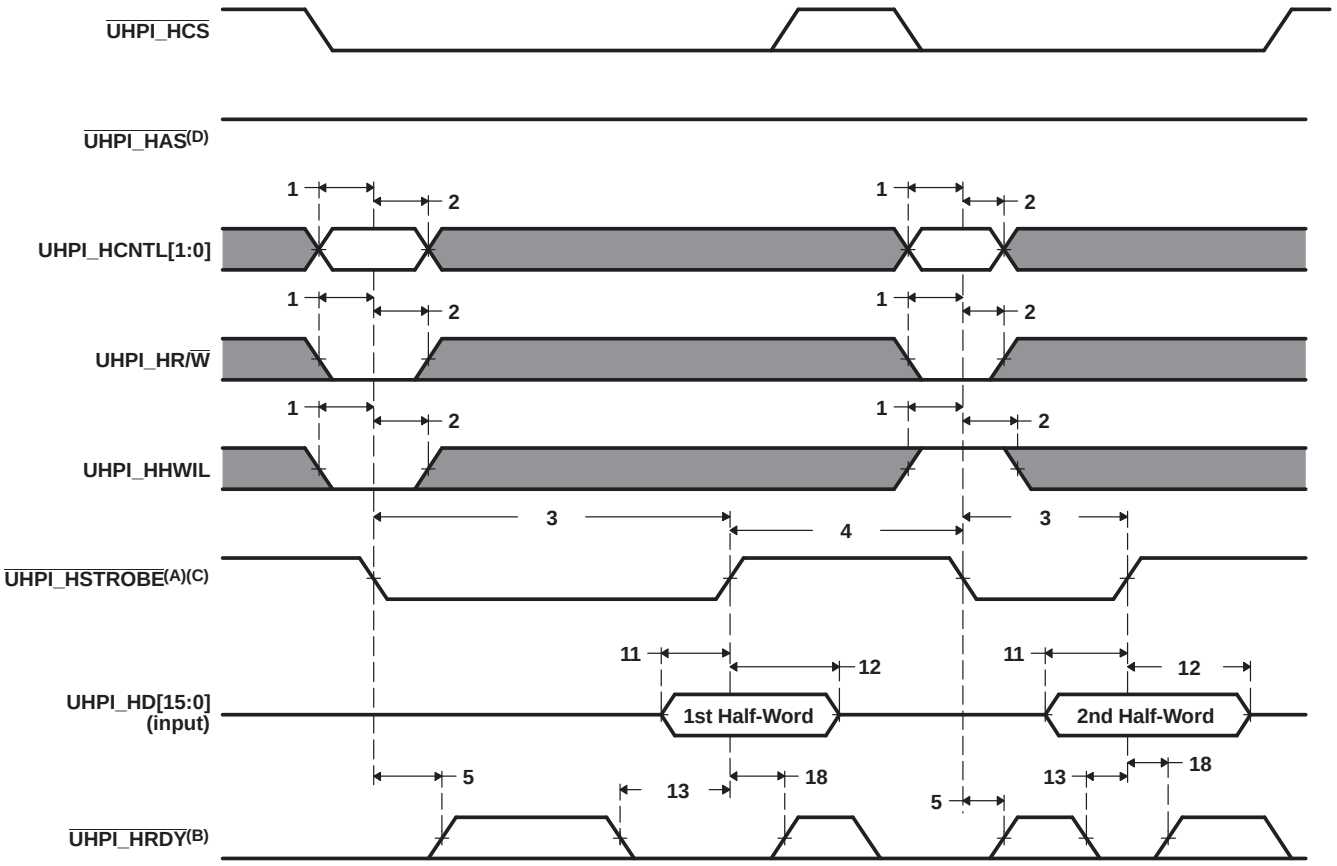


A. For correct operation, strobe the UHPI_HAS signal only once per UHPI_HSTROBE active cycle.

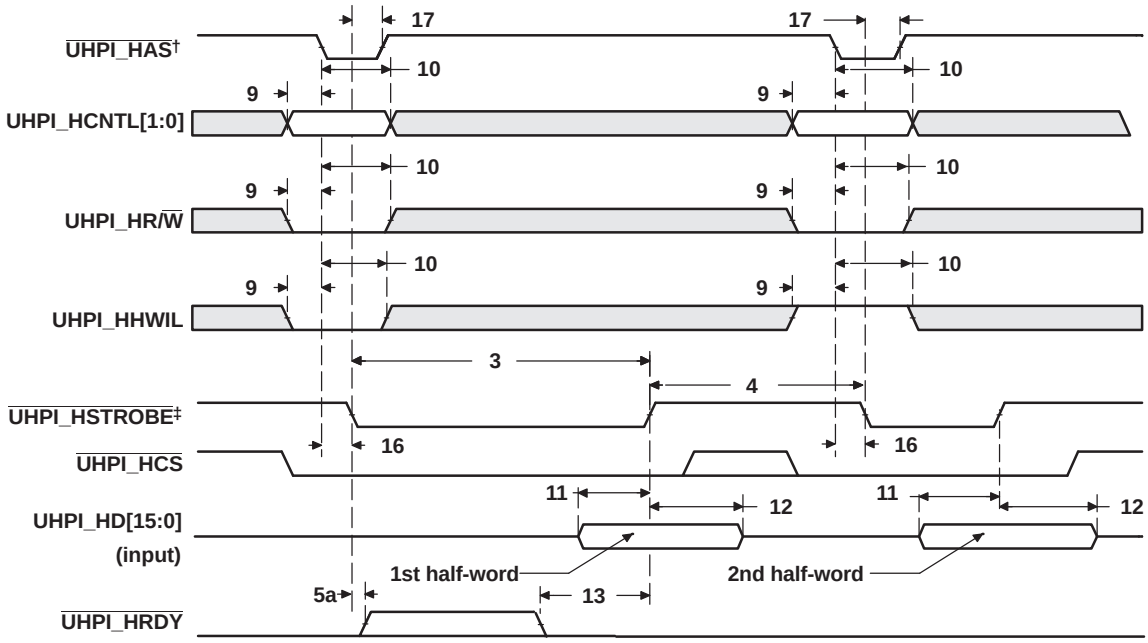
B. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

Figure 6-67. UHPI Read Timing (HAS Used)



A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

Figure 6-68. UHPI Write Timing (HAS Not Used, Tied High)



A. For correct operation, strobe the UHPI_HAS signal only once per UHPI_HSTROBE active cycle.

B. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

Figure 6-69. UHPI Write Timing (HAS Used)

6.25 Universal Parallel Port (uPP)

The Universal Parallel Port (uPP) peripheral is a multichannel, high-speed parallel interface with dedicated data lines and minimal control signals. It is designed to interface cleanly with high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) with up to 16-bit data width (per channel). It may also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode, transmit mode, or duplex mode, in which its individual channels operate in opposite directions.

The uPP peripheral includes an internal DMA controller to maximize throughput and minimize CPU overhead during high-speed data transmission. All uPP transactions use the internal DMA to provide data to or retrieve data from the I/O channels. The DMA controller includes two DMA channels, which typically service separate I/O channels. The uPP peripheral also supports data interleave mode, in which all DMA resources service a single I/O channel. In this mode, only one I/O channel may be used.

The features of the uPP include:

- Programmable data width per channel (from 8 to 16 bits inclusive)
- Programmable data justification
  - Right-justify with zero extend
  - Right-justify with sign extend
  - Left-justify with zero fill
- Supports multiplexing of interleaved data during SDR transmit
- Optional frame START signal with programmable polarity
- Optional data ENABLE signal with programmable polarity
- Optional synchronization WAIT signal with programmable polarity
- Single Data Rate (SDR) or Double data Rate (DDR, interleaved) interface
  - Supports multiplexing of interleaved data during SDR transmit
  - Supports demultiplexing and multiplexing of interleaved data during DDR transfers

6.25.1 uPP Register Descriptions

Table 6-106 shows the uPP registers.

Table 6-106. Universal Parallel Port (uPP) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 6000	UPPID	uPP Peripheral Identification Register
0x01E1 6004	UPPCR	uPP Peripheral Control Register
0x01E1 6008	UPDLB	uPP Digital Loopback Register
0x01E1 6010	UPCTL	uPP Channel Control Register
0x01E1 6014	UPICR	uPP Interface Configuration Register
0x01E1 6018	UPIVR	uPP Interface Idle Value Register
0x01E1 601C	UPTCR	uPP Threshold Configuration Register
0x01E1 6020	UPISR	uPP Interrupt Raw Status Register
0x01E1 6024	UPIER	uPP Interrupt Enabled Status Register
0x01E1 6028	UPIES	uPP Interrupt Enable Set Register
0x01E1 602C	UPIEC	uPP Interrupt Enable Clear Register
0x01E1 6030	UPEOI	uPP End-of-Interrupt Register
0x01E1 6040	UPID0	uPP DMA Channel I Descriptor 0 Register
0x01E1 6044	UPID1	uPP DMA Channel I Descriptor 1 Register
0x01E1 6048	UPID2	uPP DMA Channel I Descriptor 2 Register
0x01E1 6050	UPIS0	uPP DMA Channel I Status 0 Register
0x01E1 6054	UPIS1	uPP DMA Channel I Status 1 Register
0x01E1 6058	UPIS2	uPP DMA Channel I Status 2 Register
0x01E1 6060	UPQD0	uPP DMA Channel Q Descriptor 0 Register
0x01E1 6064	UPQD1	uPP DMA Channel Q Descriptor 1 Register
0x01E1 6068	UPQD2	uPP DMA Channel Q Descriptor 2 Register
0x01E1 6070	UPQS0	uPP DMA Channel Q Status 0 Register
0x01E1 6074	UPQS1	uPP DMA Channel Q Status 1 Register
0x01E1 6078	UPQS2	uPP DMA Channel Q Status 2 Register

6.25.2 uPP Electrical Data/Timing

Table 6-107. Timing Requirements for uPP (see Figure TBD)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(INCLK)}$	Cycle time, CH*n*_CLK	SDR mode	13.33		20		26.66		ns
			DDR mode	26.66		40		53.33		
2	$t_{w(INCLKH)}$	Pulse width, CH*n*_CLK high	SDR mode	5		8		10		ns
			DDR mode	10		16		20		
3	$t_{w(INCLKL)}$	Pulse width, CH*n*_CLK low	SDR mode	5		8		10		ns
			DDR mode	10		16		20		
4	$t_{su(STV-INCLKH)}$	Setup time, CH*n*_START valid before CH*n*_CLK high		4		5.5		6.5		ns
5	$t_{h(INCLKH-STV)}$	Hold time, CH*n*_START valid after CH*n*_CLK high		0.8		0.8		0.8		ns
6	$t_{su(ENV-INCLKH)}$	Setup time, CH*n*_ENABLE valid before CH*n*_CLK high		4		5.5		6.5		ns
7	$t_{h(INCLKH-ENV)}$	Hold time, CH*n*_ENABLE valid after CH*n*_CLK high		0.8		0.8		0.8		ns
8	$t_{su(DV-INCLKH)}$	Setup time, CH*n*_DATA/XDATA valid before CH*n*_CLK high		4		5.5		6.5		ns
9	$t_{h(INCLKH-DV)}$	Hold time, CH*n*_DATA/XDATA valid after CH*n*_CLK high		0.8		0.8		0.8		ns
10	$t_{su(DV-INCLKL)}$	Setup time, CH*n*_DATA/XDATA valid before CH*n*_CLK low		4		5.5		6.5		ns
11	$t_{h(INCLKL-DV)}$	Hold time, CH*n*_DATA/XDATA valid after CH*n*_CLK low		0.8		0.8		0.8		ns
19	$t_{su(WTV-INCLKL)}$	Setup time, CH*n*_WAIT valid before CH*n*_CLK high		4		5.5		6.5		ns
20	$t_{h(INCLKL-WTV)}$	Hold time, CH*n*_WAIT valid after CH*n*_CLK high		0.8		0.8		0.8		ns
21	$t_{c(2xTXCLK)}$	Cycle time, 2xTXCLK input clock(1)		6.66		10		13.33		ns

(1) 2xTXCLK is an alternate transmit clock source that must be at least 2 times the required uPP transmit clock rate (as it is is divided down by 2 inside the uPP). 2xTXCLK has no specified skew relationship to the CH*n*_CLOCK and therefore is not shown in the timing diagram.

Table 6-108. Switching Characteristics Over Recommended Operating Conditions for uPP (see Figure TBD)

NO.	PARAMETER			1.2V		1.1V		1.0V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{c(OUTCLK)}$	Cycle time, CH*n*_CLK	SDR mode	13.33		20		26.66		ns
			DDR mode	26.66		40		53.33		
13	$t_{w(OUTCLKH)}$	Pulse width, CH*n*_CLK high	SDR mode	5		8		10		ns
			DDR mode	10		16		20		
14	$t_{w(OUTCLKL)}$	Pulse width, CH*n*_CLK low	SDR mode	5		8		10		ns
			DDR mode	10		16		20		
15	$t_{d(OUTCLKH-STV)}$	Delay time, CH*n*_START valid after CH*n*_CLK high		2	11	2	15	2	21	ns
16	$t_{d(OUTCLKH-ENV)}$	Delay time, CH*n*_ENABLE valid after CH*n*_CLK high		2	11	2	15	2	21	ns
17	$t_{d(OUTCLKH-DV)}$	Delay time, CH*n*_DATA/XDATA valid after CH*n*_CLK high		2	11	2	15	2	21	ns
18	$t_{d(OUTCLKL-DV)}$	Delay time, CH*n*_DATA/XDATA valid after CH*n*_CLK low		2	11	2	15	2	21	ns

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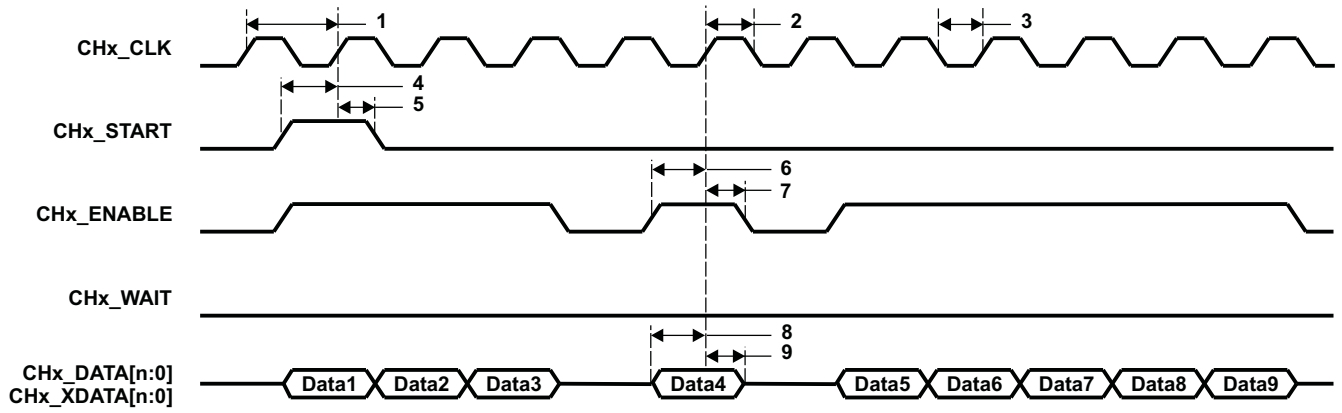

Figure 6-70. uPP Single Data Rate (SDR) Receive Timing

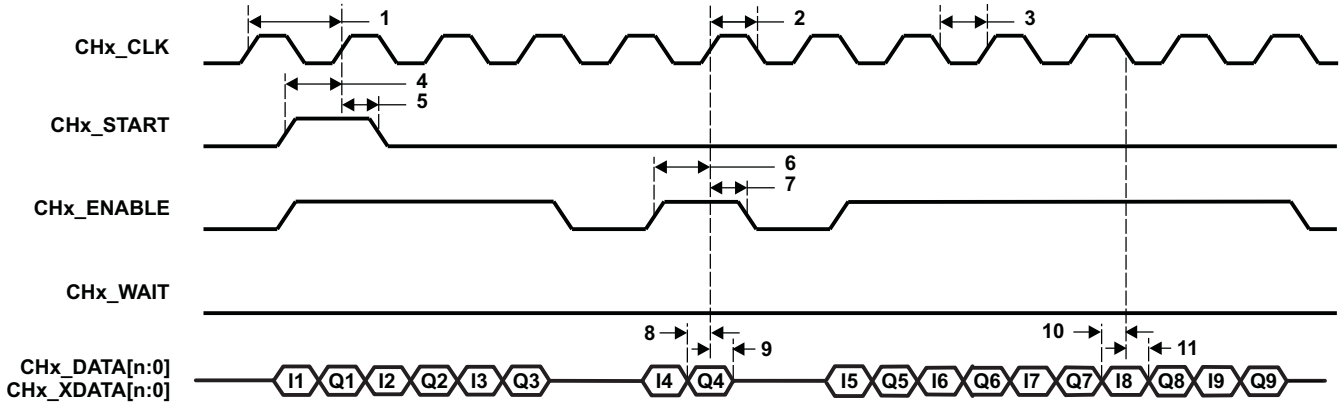

Figure 6-71. uPP Double Data Rate (DDR) Receive Timing

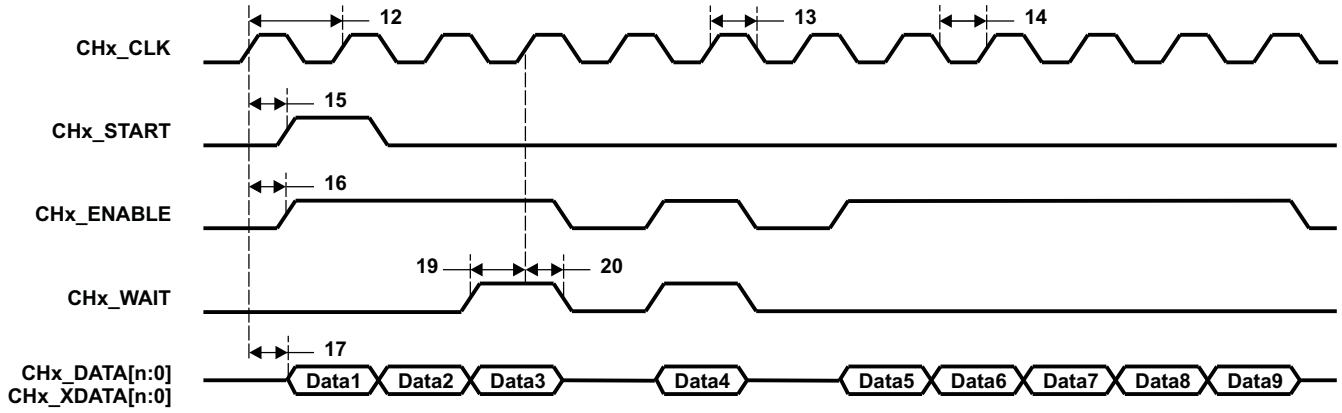

Figure 6-72. uPP Single Data Rate (SDR) Transmit Timing

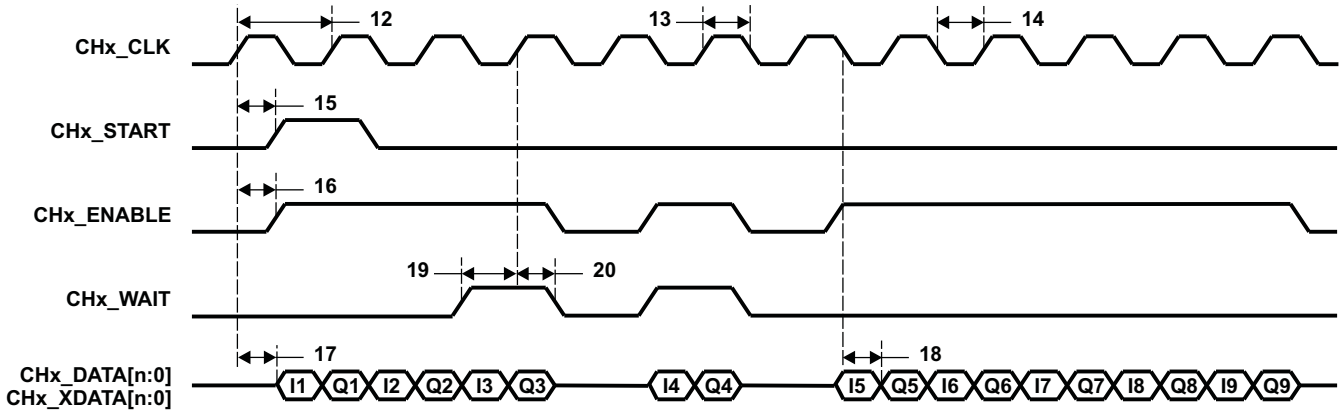

Figure 6-73. uPP Double Data Rate (DDR) Transmit Timing

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6.26 Video Port Interface (VPIF)

The Video Port Interface (VPIF) allows the capture and display of digital video streams. Features include:

- Up to 2 Video Capture Channels (Channel 0 and Channel 1)
  - Two 8-bit Standard-Definition (SD) Video with embedded timing codes (BT.656)
  - Single 16-bit High-Definition (HD) Video with embedded timing codes (BT.1120)
  - Single Raw Video (8-/10-/12-bit)
- Up to 2 Video Display Channels (Channel 2 and Channel 3)
  - Two 8-bit SD Video Display with embedded timing codes (BT.656)
  - Single 16-bit HD Video Display with embedded timing codes (BT.1120)

The VPIF capture channel input data format is selectable based on the settings of the specific Channel Control Register (Channels 0–3). The VPIF Raw Video data-bus width is selectable based on the settings of the Channel 0 Control Register.

6.26.1 VPIF Register Descriptions

Table 6-109 shows the VPIF registers.

Table 6-109. Video Port Interface (VPIF) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 7000	PID	Peripheral identification register
0x01E1 7004	CH0_CTRL	Channel 0 control register
0x01E1 7008	CH1_CTRL	Channel 1 control register
0x01E1 700C	CH2_CTRL	Channel 2 control register
0x01E1 7010	CH3_CTRL	Channel 3 control register
0x01E1 7014 - 0x01E1 701F	-	Reserved
0x01E1 7020	INTEN	Interrupt enable
0x01E1 7024	INTENSET	Interrupt enable set
0x01E1 7028	INTENCLR	Interrupt enable clear
0x01E1 702C	INTSTAT	Interrupt status
0x01E1 7030	INTSTATCLR	Interrupt status clear
0x01E1 7034	EMU_CTRL	Emulation control
0x01E1 7038	DMA_SIZE	DMA size control
0x01E1 703C - 0x01E1 703F	-	Reserved
CAPTURE CHANNEL 0 REGISTERS		
0x01E1 7040	CH0_TY_STRTADR	Channel 0 Top Field luma buffer start address
0x01E1 7044	CH0_BY_STRTADR	Channel 0 Bottom Field luma buffer start address
0x01E1 7048	CH0_TC_STRTADR	Channel 0 Top Field chroma buffer start address
0x01E1 704C	CH0_BC_STRTADR	Channel 0 Bottom Field chroma buffer start address
0x01E1 7050	CH0_THA_STRTADR	Channel 0 Top Field horizontal ancillary data buffer start address
0x01E1 7054	CH0_BHA_STRTADR	Channel 0 Bottom Field horizontal ancillary data buffer start address
0x01E1 7058	CH0_TVA_STRTADR	Channel 0 Top Field vertical ancillary data buffer start address
0x01E1 705C	CH0_BVA_STRTADR	Channel 0 Bottom Field vertical ancillary data buffer start address
0x01E1 7060	CH0_SUBPIC_CFG	Channel 0 sub-picture configuration
0x01E1 7064	CH0_IMG_ADD_OFST	Channel 0 image data address offset
0x01E1 7068	CH0_HA_ADD_OFST	Channel 0 horizontal ancillary data address offset
0x01E1 706C	CH0_HSIZE_CFG	Channel 0 horizontal data size configuration
0x01E1 7070	CH0_VSIZE_CFG0	Channel 0 vertical data size configuration (0)
0x01E1 7074	CH0_VSIZE_CFG1	Channel 0 vertical data size configuration (1)
0x01E1 7078	CH0_VSIZE_CFG2	Channel 0 vertical data size configuration (2)
0x01E1 707C	CH0_VSIZE	Channel 0 vertical image size
CAPTURE CHANNEL 1 REGISTERS		
0x01E1 7080	CH1_TY_STRTADR	Channel 1 Top Field luma buffer start address
0x01E1 7084	CH1_BY_STRTADR	Channel 1 Bottom Field luma buffer start address
0x01E1 7088	CH1_TC_STRTADR	Channel 1 Top Field chroma buffer start address
0x01E1 708C	CH1_BC_STRTADR	Channel 1 Bottom Field chroma buffer start address
0x01E1 7090	CH1_THA_STRTADR	Channel 1 Top Field horizontal ancillary data buffer start address
0x01E1 7094	CH1_BHA_STRTADR	Channel 1 Bottom Field horizontal ancillary data buffer start address
0x01E1 7098	CH1_TVA_STRTADR	Channel 1 Top Field vertical ancillary data buffer start address
0x01E1 709C	CH1_BVA_STRTADR	Channel 1 Bottom Field vertical ancillary data buffer start address
0x01E1 70A0	CH1_SUBPIC_CFG	Channel 1 sub-picture configuration
0x01E1 70A4	CH1_IMG_ADD_OFST	Channel 1 image data address offset
0x01E1 70A8	CH1_HA_ADD_OFST	Channel 1 horizontal ancillary data address offset
0x01E1 70AC	CH1_HSIZE_CFG	Channel 1 horizontal data size configuration

Table 6-109. Video Port Interface (VPIF) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 70B0	CH1_VSIZE_CFG0	Channel 1 vertical data size configuration (0)
0x01E1 70B4	CH1_VSIZE_CFG1	Channel 1 vertical data size configuration (1)
0x01E1 70B8	CH1_VSIZE_CFG2	Channel 1 vertical data size configuration (2)
0x01E1 70BC	CH1_VSIZE	Channel 1 vertical image size
DISPLAY CHANNEL 2 REGISTERS		
0x01E1 70C0	CH2_TY_STRTADR	Channel 2 Top Field luma buffer start address
0x01E1 70C4	CH2_BY_STRTADR	Channel 2 Bottom Field luma buffer start address
0x01E1 70C8	CH2_TC_STRTADR	Channel 2 Top Field chroma buffer start address
0x01E1 70CC	CH2_BC_STRTADR	Channel 2 Bottom Field chroma buffer start address
0x01E1 70D0	CH2_THA_STRTADR	Channel 2 Top Field horizontal ancillary data buffer start address
0x01E1 70D4	CH2_BHA_STRTADR	Channel 2 Bottom Field horizontal ancillary data buffer start address
0x01E1 70D8	CH2_TVA_STRTADR	Channel 2 Top Field vertical ancillary data buffer start address
0x01E1 70DC	CH2_BVA_STRTADR	Channel 2 Bottom Field vertical ancillary data buffer start address
0x01E1 70E0	CH2_SUBPIC_CFG	Channel 2 sub-picture configuration
0x01E1 70E4	CH2_IMG_ADD_OFST	Channel 2 image data address offset
0x01E1 70E8	CH2_HA_ADD_OFST	Channel 2 horizontal ancillary data address offset
0x01E1 70EC	CH2_HSIZE_CFG	Channel 2 horizontal data size configuration
0x01E1 70F0	CH2_VSIZE_CFG0	Channel 2 vertical data size configuration (0)
0x01E1 70F4	CH2_VSIZE_CFG1	Channel 2 vertical data size configuration (1)
0x01E1 70F8	CH2_VSIZE_CFG2	Channel 2 vertical data size configuration (2)
0x01E1 70FC	CH2_VSIZE	Channel 2 vertical image size
0x01E1 7100	CH2_THA_STRTPOS	Channel 2 Top Field horizontal ancillary data insertion start position
0x01E1 7104	CH2_THA_SIZE	Channel 2 Top Field horizontal ancillary data size
0x01E1 7108	CH2_BHA_STRTPOS	Channel 2 Bottom Field horizontal ancillary data insertion start position
0x01E1 710C	CH2_BHA_SIZE	Channel 2 Bottom Field horizontal ancillary data size
0x01E1 7110	CH2_TVA_STRTPOS	Channel 2 Top Field vertical ancillary data insertion start position
0x01E1 7114	CH2_TVA_SIZE	Channel 2 Top Field vertical ancillary data size
0x01E1 7118	CH2_BVA_STRTPOS	Channel 2 Bottom Field vertical ancillary data insertion start position
0x01E1 711C	CH2_BVA_SIZE	Channel 2 Bottom Field vertical ancillary data size
0x01E1 7120 - 0x01E1 713F	-	Reserved
DISPLAY CHANNEL 3 REGISTERS		
0x01E1 7140	CH3_TY_STRTADR	Channel 3 Field 0 luma buffer start address
0x01E1 7144	CH3_BY_STRTADR	Channel 3 Field 1 luma buffer start address
0x01E1 7148	CH3_TC_STRTADR	Channel 3 Field 0 chroma buffer start address
0x01E1 714C	CH3_BC_STRTADR	Channel 3 Field 1 chroma buffer start address
0x01E1 7150	CH3_THA_STRTADR	Channel 3 Field 0 horizontal ancillary data buffer start address
0x01E1 7154	CH3_BHA_STRTADR	Channel 3 Field 1 horizontal ancillary data buffer start address
0x01E1 7158	CH3_TVA_STRTADR	Channel 3 Field 0 vertical ancillary data buffer start address
0x01E1 715C	CH3_BVA_STRTADR	Channel 3 Field 1 vertical ancillary data buffer start address
0x01E1 7160	CH3_SUBPIC_CFG	Channel 3 sub-picture configuration
0x01E1 7164	CH3_IMG_ADD_OFST	Channel 3 image data address offset
0x01E1 7168	CH3_HA_ADD_OFST	Channel 3 horizontal ancillary data address offset
0x01E1 716C	CH3_HSIZE_CFG	Channel 3 horizontal data size configuration
0x01E1 7170	CH3_VSIZE_CFG0	Channel 3 vertical data size configuration (0)
0x01E1 7174	CH3_VSIZE_CFG1	Channel 3 vertical data size configuration (1)
0x01E1 7178	CH3_VSIZE_CFG2	Channel 3 vertical data size configuration (2)
0x01E1 717C	CH3_VSIZE	Channel 3 vertical image size

Table 6-109. Video Port Interface (VPIF) Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E1 7180	CH3_THA_STRTPOS	Channel 3 Top Field horizontal ancillary data insertion start position
0x01E1 7184	CH3_THA_SIZE	Channel 3 Top Field horizontal ancillary data size
0x01E1 7188	CH3_BHA_STRTPOS	Channel 3 Bottom Field horizontal ancillary data insertion start position
0x01E1 718C	CH3_BHA_SIZE	Channel 3 Bottom Field horizontal ancillary data size
0x01E1 7190	CH3_TVA_STRTPOS	Channel 3 Top Field vertical ancillary data insertion start position
0x01E1 7194	CH3_TVA_SIZE	Channel 3 Top Field vertical ancillary data size
0x01E1 7198	CH3_BVA_STRTPOS	Channel 3 Bottom Field vertical ancillary data insertion start position
0x01E1 719C	CH3_BVA_SIZE	Channel 3 Bottom Field vertical ancillary data size
0x01E1 71A0 - 0x01E1 71FF	-	Reserved

6.26.2 VPIF Electrical Data/Timing

Table 6-110. Timing Requirements for VPIF VP_CLKINx Inputs(1) (see Figure 6-74)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(VKI)}$	Cycle time, VP_CLKIN0	13.3		20		26.6		ns
		Cycle time, VP_CLKIN1/2/3	13.3		20		26.6		ns
2	$t_{w(VKIH)}$	Pulse duration, VP_CLKINx high	0.4C		0.4C		0.4C		ns
3	$t_{w(VKIL)}$	Pulse duration, VP_CLKINx low	0.4C		0.4C		0.4C		ns
4	$t_{t(VKI)}$	Transition time, VP_CLKINx		5		5		5	ns

(1) C = VP_CLKINx period in ns.

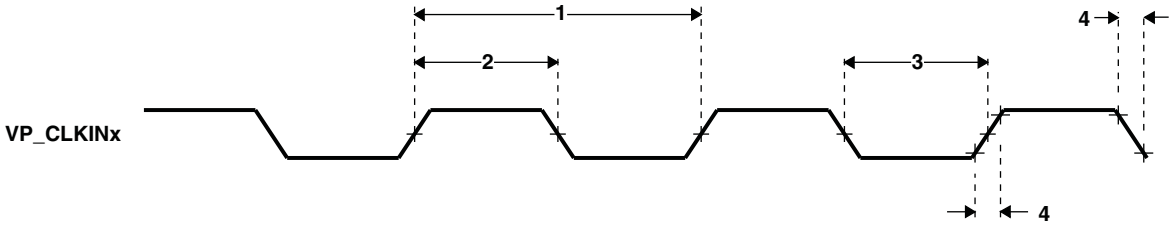

Figure 6-74. Video Port Capture VP_CLKINx Timing

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Table 6-111. Timing Requirements for VPIF Channels 0/1 Video Capture Data and Control Inputs (see Figure 6-75)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(VDINV-VKIH)}$	Setup time, VP_DINx valid before VP_CLKIN0/1 high	4		6		7		ns
2	$t_{h(VKIH-VDINV)}$	Hold time, VP_DINx valid after VP_CLKIN0/1 high	0		0		0		ns

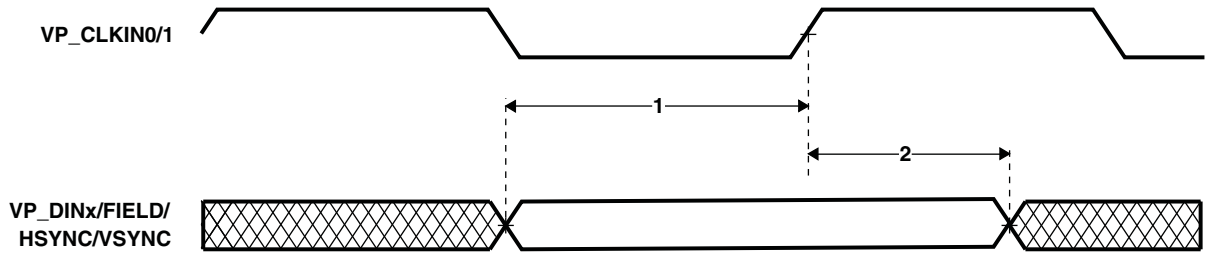

Figure 6-75. VPIF Channels 0/1 Video Capture Data and Control Input Timing

Table 6-112. Switching Characteristics Over Recommended Operating Conditions for Video Data Shown With Respect to VP_CLKOUT2/3[(1)] (see Figure 6-76)

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(VKO)}$	Cycle time, VP_CLKOUT2/3	13.3		20		26.6		ns
2	$t_{w(VKOH)}$	Pulse duration, VP_CLKOUT2/3 high	0.4C		0.4C		0.4C		ns
3	$t_{w(VKOL)}$	Pulse duration, VP_CLKOUT2/3 low	0.4C		0.4C		0.4C		ns
4	$t_{t(VKO)}$	Transition time, VP_CLKOUT2/3		5		5		5	ns
11	$t_{d(VKOH-VPDOUTV)}$	Delay time, VP_CLKOUT2/3 high to VP_DOUTx valid		8.5		12		17	ns
12	$t_{d(VCLKOH-VPDOUTIV)}$	Delay time, VP_CLKOUT2/3 high to VP_DOUTx invalid	1.5		1.5		1.5		ns

(1) C = VP_CLKO2/3 period in ns.

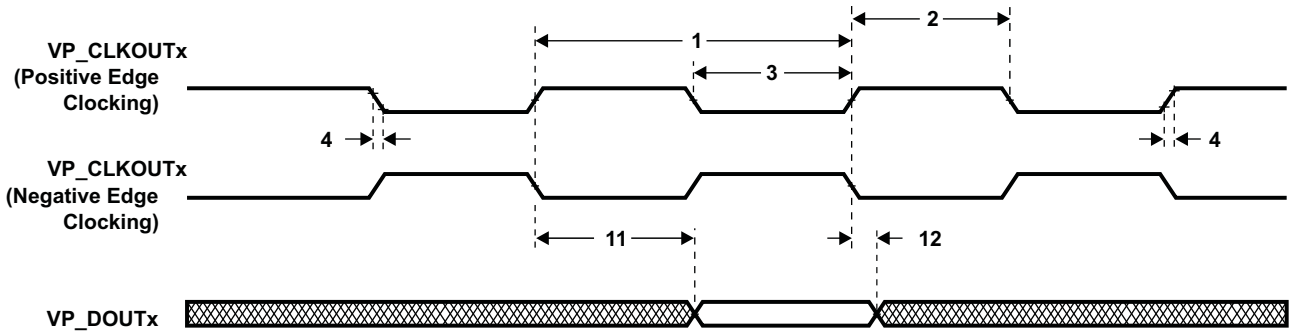

Figure 6-76. VPIF Channels 2/3 Video Display Data Output Timing With Respect to VP_CLKOUT2/3

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6.27 Enhanced Capture (eCAP) Peripheral

The device contains up to three enhanced capture (eCAP) modules. Figure 6-77 shows a functional block diagram of a module.

Uses for ECAP include:

- Speed measurements of rotating machinery (e.g. toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor triggers
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The ECAP module described in this specification includes the following features:

- 32 bit time base
- 4 event time-stamp registers (each 32 bits)
- Edge polarity selection for up to 4 sequenced time-stamp capture events
- Interrupt on either of the 4 events
- Single shot capture of up to 4 event time-stamps
- Continuous mode capture of time-stamps in a 4 deep circular buffer
- Absolute time-stamp capture
- Difference mode time-stamp capture
- All the above resources are dedicated to a single input pin

The eCAP modules are clocked at the ASYNC3 clock domain rate.

The clock enable bits (ECAP1/2/3/4ENCLK) in the PCLKCR1 register are used to turn off the eCAP modules individually (for low power operation). Upon reset, ECAP1ENCLK, ECAP2ENCLK, ECAP3ENCLK, and ECAP4EN CLK are set to low, indicating that the peripheral clock is off.

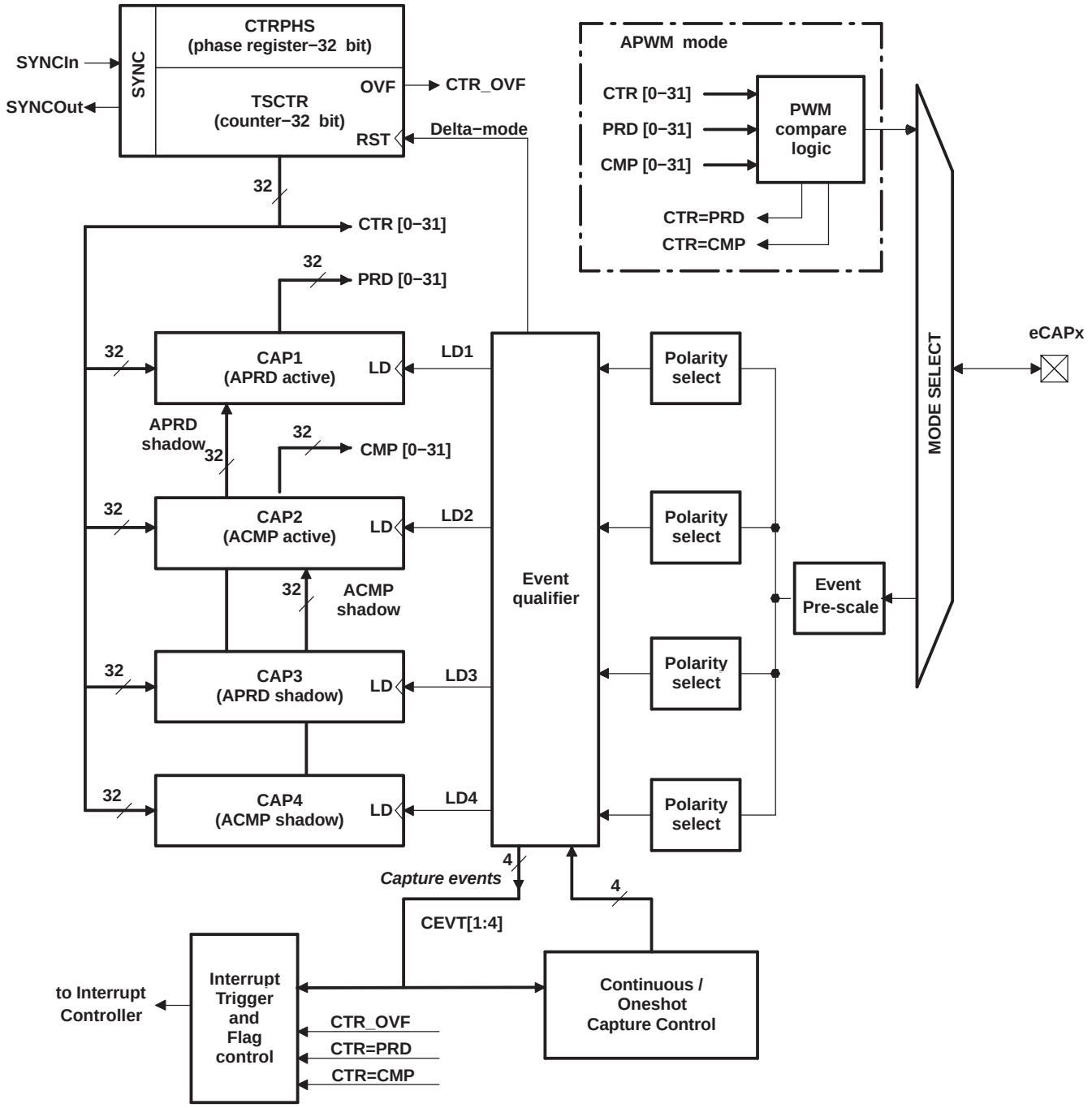

Figure 6-77. eCAP Functional Block Diagram

Table 6-113 is the list of the ECAP registers.

Table 6-113. ECAPx Configuration Registers

ECAP0 BYTE ADDRESS	ECAP1 BYTE ADDRESS	ECAP2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01F0 6000	0x01F0 7000	0x01F0 8000	TSCTR	Time-Stamp Counter
0x01F0 6004	0x01F0 7004	0x01F0 8004	CTRPHS	Counter Phase Offset Value Register
0x01F0 6008	0x01F0 7008	0x01F0 8008	CAP1	Capture 1 Register
0x01F0 600C	0x01F0 700C	0x01F0 800C	CAP2	Capture 2 Register
0x01F0 6010	0x01F0 7010	0x01F0 8010	CAP3	Capture 3 Register
0x01F0 6014	0x01F0 7014	0x01F0 8014	CAP4	Capture 4 Register
0x01F0 6028	0x01F0 7028	0x01F0 8028	ECCTL1	Capture Control Register 1
0x01F0 602A	0x01F0 702A	0x01F0 802A	ECCTL2	Capture Control Register 2
0x01F0 602C	0x01F0 702C	0x01F0 802C	ECEINT	Capture Interrupt Enable Register
0x01F0 602E	0x01F0 702E	0x01F0 802E	ECFLG	Capture Interrupt Flag Register
0x01F0 6030	0x01F0 7030	0x01F0 8030	ECCLR	Capture Interrupt Clear Register
0x01F0 6032	0x01F0 7032	0x01F0 8032	ECFRC	Capture Interrupt Force Register
0x01F0 605C	0x01F0 705C	0x01F0 805C	REVID	Revision ID

Table 6-114 shows the eCAP timing requirement and Table 6-115 shows the eCAP switching characteristics.

Table 6-114. Timing Requirements for Enhanced Capture (eCAP)

PARAMETER		TEST CONDITIONS	1.2V, 1.1V, 1.0V		
			MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

Table 6-115. Switching Characteristics Over Recommended Operating Conditions for eCAP

PARAMETER		1.2V		1.1V		1.0V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20		20		20		ns

6.28 Enhanced High-Resolution Pulse-Width Modulator (eHRPWM)

The device contains two enhanced PWM Modules (eHRPWM). Figure 6-78 shows a block diagram of multiple eHRPWM modules. Figure 4-4 shows the signal interconnections with the eHRPWM.

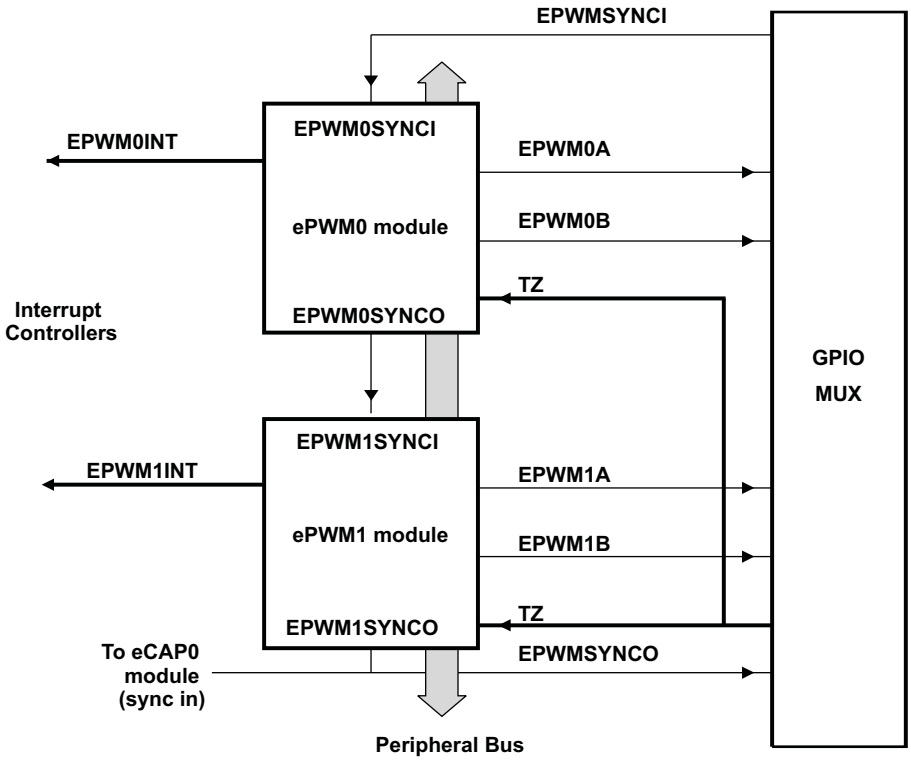

Figure 6-78. Multiple PWM Modules in a C6748 System

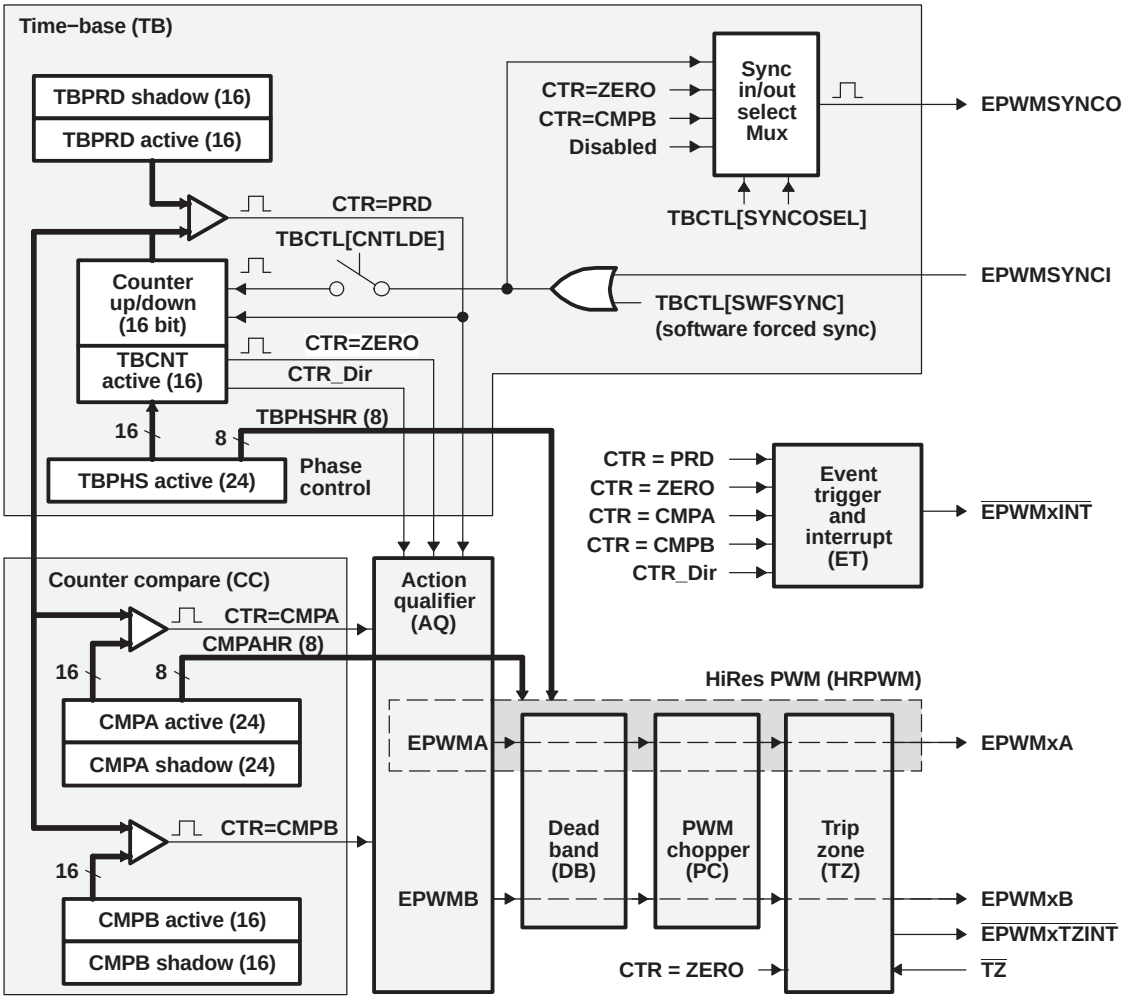

Figure 6-79. eHRPWM Sub-Modules Showing Critical Internal Signal Interconnections

Table 6-116. eHRPWM Module Control and Status Registers Grouped by Submodule

eHRPWM0 BYTE ADDRESS	eHRPWM1 BYTE ADDRESS	Acronym	Shadow	Register Description
Time-Base Submodule Registers				
0x01F0 0000	0x01F0 2000	TBCTL	No	Time-Base Control Register
0x01F0 0002	0x01F0 2002	TBSTS	No	Time-Base Status Register
0x01F0 0004	0x01F0 2004	TBPHSHR	No	Extension for HRPWM Phase Register (1)
0x01F0 0006	0x01F0 2006	TBPHS	No	Time-Base Phase Register
0x01F0 0008	0x01F0 2008	TBCNT	No	Time-Base Counter Register
0x01F0 000A	0x01F0 200A	TBPRD	Yes	Time-Base Period Register
Counter-Compare Submodule Registers				
0x01F0 000E	0x01F0 200E	CMPCTL	No	Counter-Compare Control Register
0x01F0 0010	0x01F0 2010	CMPAHR	No	Extension for HRPWM Counter-Compare A Register (1)
0x01F0 0012	0x01F0 2012	CMPA	Yes	Counter-Compare A Register
0x01F0 0014	0x01F0 2014	CMPB	Yes	Counter-Compare B Register
Action-Qualifier Submodule Registers				
0x01F0 0016	0x01F0 2016	AQCTLA	No	Action-Qualifier Control Register for Output A (eHRPWMxA)
0x01F0 0018	0x01F0 2018	AQCTLB	No	Action-Qualifier Control Register for Output B (eHRPWMxB)
0x01F0 001A	0x01F0 201A	AQSFRC	No	Action-Qualifier Software Force Register
0x01F0 001C	0x01F0 201C	AQCSFRC	Yes	Action-Qualifier Continuous S/W Force Register Set
Dead-Band Generator Submodule Registers				
0x01F0 001E	0x01F0 201E	DBCTL	No	Dead-Band Generator Control Register
0x01F0 0020	0x01F0 2020	DBRED	No	Dead-Band Generator Rising Edge Delay Count Register
0x01F0 0022	0x01F0 2022	DBFED	No	Dead-Band Generator Falling Edge Delay Count Register
PWM-Chopper Submodule Registers				
0x01F0 003C	0x01F0 203C	PCCTL	No	PWM-Chopper Control Register
Trip-Zone Submodule Registers				
0x01F0 0024	0x01F0 2024	TZSEL	No	Trip-Zone Select Register
0x01F0 0028	0x01F0 2028	TZCTL	No	Trip-Zone Control Register
0x01F0 002A	0x01F0 202A	TZEINT	No	Trip-Zone Enable Interrupt Register
0x01F0 002C	0x01F0 202C	TZFLG	No	Trip-Zone Flag Register
0x01F0 002E	0x01F0 202E	TZCLR	No	Trip-Zone Clear Register
0x01F0 0030	0x01F0 2030	TZFRC	No	Trip-Zone Force Register
Event-Trigger Submodule Registers				
0x01F0 0032	0x01F0 2032	ETSEL	No	Event-Trigger Selection Register
0x01F0 0034	0x01F0 2034	ETPS	No	Event-Trigger Pre-Scale Register
0x01F0 0036	0x01F0 2036	ETFLG	No	Event-Trigger Flag Register
0x01F0 0038	0x01F0 2038	ETCLR	No	Event-Trigger Clear Register
0x01F0 003A	0x01F0 203A	ETFRC	No	Event-Trigger Force Register
High-Resolution PWM (HRPWM) Submodule Registers				
0x01F0 1020	0x01F0 3020	HRCNFG	No	HRPWM Configuration Register (1)

(1) These registers are only available on eHRPWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, these locations are reserved.

6.28.1 Enhanced Pulse Width Modulator (eHRPWM) Timing

PWM refers to PWM outputs on eHRPWM1-6. Table 6-117 shows the PWM timing requirements and Table 6-118, switching characteristics.

Table 6-117. Timing Requirements for eHRPWM

PARAMETER		TEST CONDITIONS	1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

Table 6-118. Switching Characteristics Over Recommended Operating Conditions for eHRPWM

PARAMETER		TEST CONDITIONS	1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		TBD		TBD		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		$8t_{c(SCO)}$		$8t_{c(SCO)}$		cycles
$t_{d(PWM)TZA}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25		TBD		TBD	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20		TBD		TBD	ns

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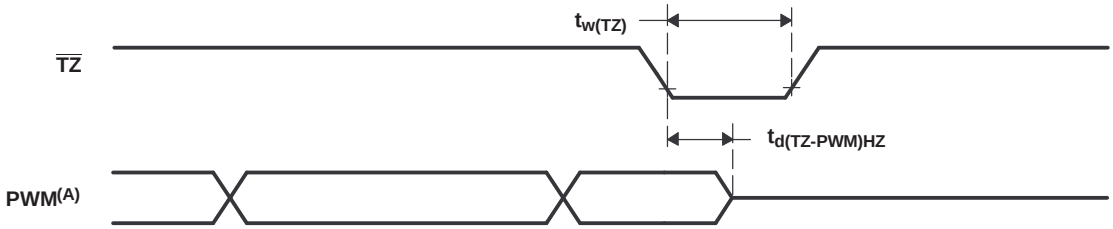
6.28.2 Trip-Zone Input Timing



A. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-80. PWM Hi-Z Characteristics

Table 6-119. Trip-Zone input Timing Requirements

PARAMETER		TEST CONDITIONS	1.2V, 1.1V, 1.0V		
			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}$x input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

Table 6-120 shows the high-resolution PWM switching characteristics.

Table 6-120. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)

PARAMETER	1.2V			1.1V			1.0V			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		200			TBD			TBD		ps

(1) Maximum MEP step size is based on worst-case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

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6.29 Timers

The timers support the following features:

- Configurable as single 64-bit timer or two 32-bit timers
- Period timeouts generate interrupts, DMA events or external pin events
- 8 32-bit compare registers
- Compare matches generate interrupt events
- Capture capability
- 64-bit Watchdog capability (Timer64P1 only)

Table 6-121 lists the timer registers.

Table 6-121. Timer Registers

TIMER64P 0 BYTE ADDRESS	TIMER64P 1 BYTE ADDRESS	TIMER64P 2 BYTE ADDRESS	TIMER64P 3 BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C2 0000	0x01C2 1000	0x01F0 C000	0x01F0 D000	REV	Revision Register
0x01C2 0004	0x01C2 1004	0x01F0 C004	0x01F0 D004	EMUMGT	Emulation Management Register
0x01C2 0008	0x01C2 1008	0x01F0 C008	0x01F0 D008	GPINTGPEN	GPIO Interrupt and GPIO Enable Register
0x01C2 000C	0x01C2 100C	0x01F0 C00C	0x01F0 D00C	GPDATGPDIR	GPIO Data and GPIO Direction Register
0x01C2 0010	0x01C2 1010	0x01F0 C010	0x01F0 D010	TIM12	Timer Counter Register 12
0x01C2 0014	0x01C2 1014	0x01F0 C014	0x01F0 D014	TIM34	Timer Counter Register 34
0x01C2 0018	0x01C2 1018	0x01F0 C018	0x01F0 D018	PRD12	Timer Period Register 12
0x01C2 001C	0x01C2 101C	0x01F0 C01C	0x01F0 D01C	PRD34	Timer Period Register 34
0x01C2 0020	0x01C2 1020	0x01F0 C020	0x01F0 D020	TCR	Timer Control Register
0x01C2 0024	0x01C2 1024	0x01F0 C024	0x01F0 D024	TGCR	Timer Global Control Register
0x01C2 0028	0x01C2 1028	0x01F0 C028	0x01F0 D028	WDTCR	Watchdog Timer Control Register
0x01C2 0034	0x01C2 1034	0x01F0 C034	0x01F0 D034	REL12	Timer Reload Register 12
0x01C2 0038	0x01C2 1038	0x01F0 C038	0x01F0 D038	REL34	Timer Reload Register 34
0x01C2 003C	0x01C2 103C	0x01F0 C03C	0x01F0 D03C	CAP12	Timer Capture Register 12
0x01C2 0040	0x01C2 1040	0x01F0 C040	0x01F0 D040	CAP34	Timer Capture Register 34
0x01C2 0044	0x01C2 1044	0x01F0 C044	0x01F0 D044	INTCTLSTAT	Timer Interrupt Control and Status Register
0x01C2 0060	0x01C2 1060	0x01F0 C060	0x01F0 D060	CMP0	Compare Register 0
0x01C2 0064	0x01C2 1064	0x01F0 C064	0x01F0 D064	CMP1	Compare Register 1
0x01C2 0068	0x01C2 1068	0x01F0 C068	0x01F0 D068	CMP2	Compare Register 2
0x01C2 006C	0x01C2 106C	0x01F0 C06C	0x01F0 D06C	CMP3	Compare Register 3
0x01C2 0070	0x01C2 1070	0x01F0 C070	0x01F0 D070	CMP4	Compare Register 4
0x01C2 0074	0x01C2 1074	0x01F0 C074	0x01F0 D074	CMP5	Compare Register 5
0x01C2 0078	0x01C2 1078	0x01F0 C078	0x01F0 D078	CMP6	Compare Register 6
0x01C2 007C	0x01C2 107C	0x01F0 C07C	0x01F0 D07C	CMP7	Compare Register 7

6.29.1 Timer Electrical Data/Timing

Table 6-122. Timing Requirements for Timer Input(1)(2) (see Figure 6-81)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{c(TM64Px\_IN12)}$	Cycle time, TM64Px_IN12	4P		ns
2	$t_{w(TINPH)}$	Pulse duration, TM64Px_IN12 high	0.45C	0.55C	ns
3	$t_{w(TINPL)}$	Pulse duration, TM64Px_IN12 low	0.45C	0.55C	ns
4	$t_{t(TM64Px\_IN12)}$	Transition time, TM64Px_IN12		0.05C	ns

(1) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.
(2) C = TM64P0_IN12 cycle time in ns. For example, when TM64Px_IN12 frequency is 27 MHz, use C = 37.0$\overline{37}$ ns

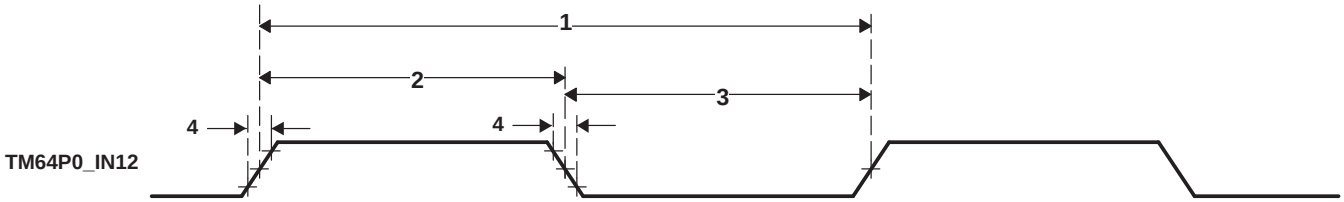

Figure 6-81. Timer Timing

Table 6-123. Switching Characteristics Over Recommended Operating Conditions for Timer Output (1)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
5	$t_{w(TOUTH)}$	Pulse duration, TM64P0_OUT12 high	4P		ns
6	$t_{w(TOUTL)}$	Pulse duration, TM64P0_OUT12 low	4P		ns

(1) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.

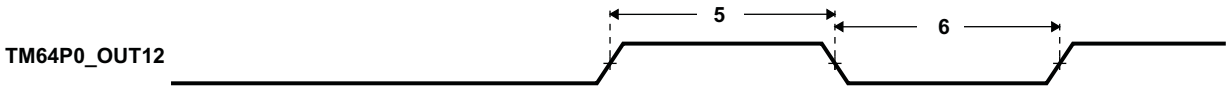

Figure 6-82. Timer Timing

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6.30 Real Time Clock (RTC)

The RTC provides a time reference to an application running on the device. The current date and time is tracked in a set of counter registers that update once per second. The time can be represented in 12-hour or 24-hour mode. The calendar and time registers are buffered during reads and writes so that updates do not interfere with the accuracy of the time and date.

Alarms are available to interrupt the CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. In addition, the RTC can interrupt the CPU every time the calendar and time registers are updated, or at programmable periodic intervals.

The real-time clock (RTC) provides the following features:

- 100-year calendar (xx00 to xx99)
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 12-hour clock mode (with AM and PM) or 24-hour clock mode
- Alarm interrupt
- Periodic interrupt
- Single interrupt to the CPU
- Supports external 32.768-kHz crystal or external clock source of the same frequency
- Separate isolated power supply

Figure 6-83 shows a block diagram of the RTC.

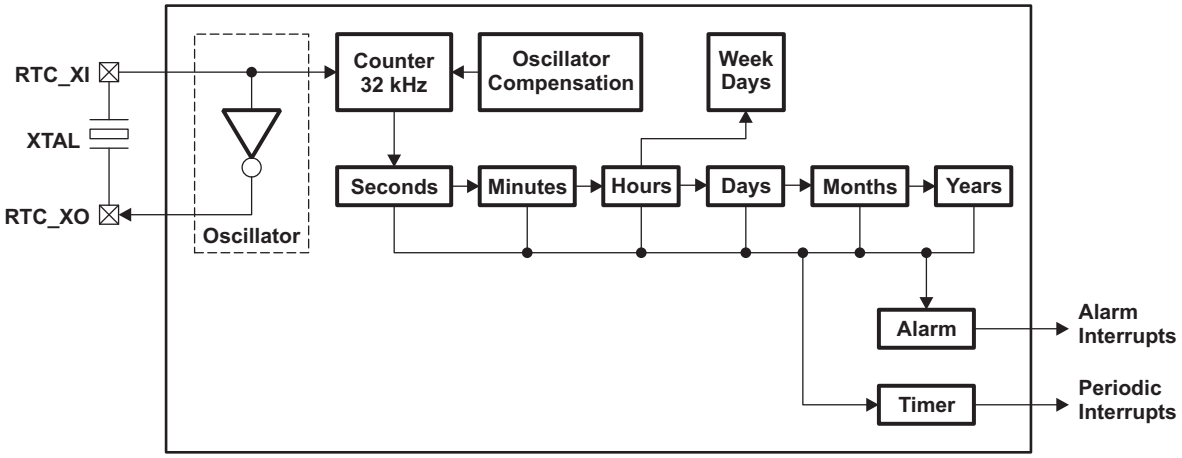

Figure 6-83. Real-Time Clock Block Diagram

6.30.1 Clock Source

The clock reference for the RTC is an external 32.768-kHz crystal or an external clock source of the same frequency. The RTC also has a separate power supply that is isolated from the rest of the system. When the CPU and other peripherals are without power, the RTC can remain powered to preserve the current time and calendar information. Even if the RTC is not used, it must remain powered when the rest of the device is powered.

The source for the RTC reference clock may be provided by a crystal or by an external clock source. The RTC has an internal oscillator buffer to support direct operation with a crystal. The crystal is connected between pins RTC_XI and RTC_XO. RTC_XI is the input to the on-chip oscillator and RTC_XO is the output from the oscillator back to the crystal.

An external 32.768-kHz clock source may be used instead of a crystal. In such a case, the clock source is connected to RTC_XI, and RTC_XO is left unconnected.

If the RTC is not used, the RTC_XI pin should be held either low or high, RTC_XO should be left unconnected, RTC_CVDD should be connected to the device CVDD and RTC_VSS should remain grounded.

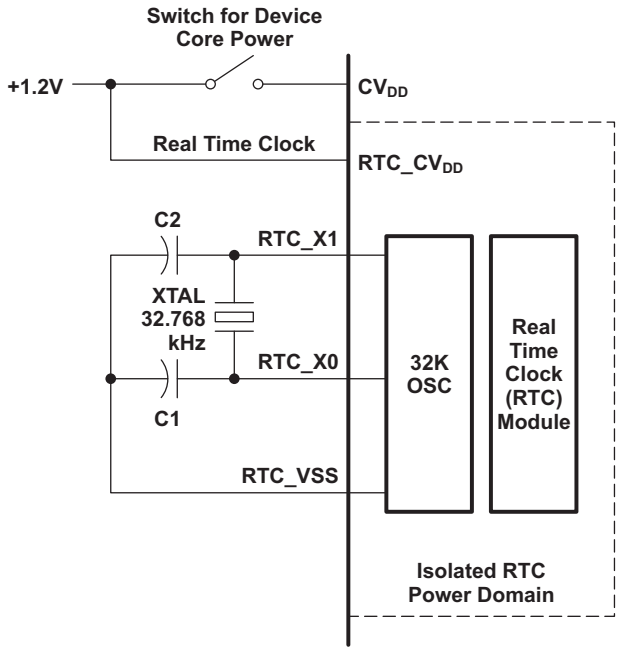

Figure 6-84. Clock Source

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6.30.2 Registers

Table 6-124 lists the memory-mapped registers for the RTC. See the device-specific data manual for the memory address of these registers.

Table 6-124. Real-Time Clock (RTC) Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C2 3000	SECOND	Seconds Register
0x01C2 3004	MINUTE	Minutes Register
0x01C2 3008	HOUR	Hours Register
0x01C2 300C	DAY	Day of the Month Register
0x01C2 3010	MONTH	Month Register
0x01C2 3014	YEAR	Year Register
0x01C2 3018	DOTW	Day of the Week Register
0x01C2 3020	ALARMSECOND	Alarm Seconds Register
0x01C2 3024	ALARMMINUTE	Alarm Minutes Register
0x01C2 3028	ALARMHOUR	Alarm Hours Register
0x01C2 302C	ALARMDAY	Alarm Days Register
0x01C2 3030	ALARMMONTH	Alarm Months Register
0x01C2 3034	ALARMYEAR	Alarm Years Register
0x01C2 3040	CTRL	Control Register
0x01C2 3044	STATUS	Status Register
0x01C2 3048	INTERRUPT	Interrupt Enable Register
0x01C2 304C	COMPLSB	Compensation (LSB) Register
0x01C2 3050	COMPMSB	Compensation (MSB) Register
0x01C2 3054	OSC	Oscillator Register
0x01C2 3060	SCRATCH0	Scratch 0 (General-Purpose) Register
0x01C2 3064	SCRATCH1	Scratch 1 (General-Purpose) Register
0x01C2 3068	SCRATCH2	Scratch 2 (General-Purpose) Register
0x01C2 306C	KICK0	Kick 0 (Write Protect) Register
0x01C2 3070	KICK1	Kick 1 (Write Protect) Register

6.31 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]).

The device GPIO peripheral supports the following:

- Up to 144 Pins configurable as GPIO
- External Interrupt and DMA request Capability
  - Every GPIO pin may be configured to generate an interrupt request on detection of rising and/or falling edges on the pin.
  - The interrupt requests within each bank are combined (logical or) to create eight unique bank level interrupt requests.
  - The bank level interrupt service routine may poll the INTSTATx register for its bank to determine which pin(s) have triggered the interrupt.
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, 7 and 8 Interrupts assigned to DSP Events 65, 41, 49, 52, 54, 59, 62, 72 and 75 respectively
  - GPIO Banks 0, 1, 2, 3, 4, and 5 are assigned to EDMA events 6, 7, 22, 23, 28, 29, and 29 respectively on Channel Controller 0 and GPIO Banks 6, 7, and 8 are assigned to EDMA events 16, 17, and 18 respectively on Channel Controller 1.
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

The memory map for the GPIO registers is shown in Table 6-125.

6.31.1 GPIO Register Description(s)

Table 6-125. GPIO Registers

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 6000	REV	Peripheral Revision Register
0x01E2 6004	RESERVED	Reserved
0x01E2 6008	BINTEN	GPIO Interrupt Per-Bank Enable Register
GPIO Banks 0 and 1		
0x01E2 6010	DIR01	GPIO Banks 0 and 1 Direction Register
0x01E2 6014	OUT_DATA01	GPIO Banks 0 and 1 Output Data Register
0x01E2 6018	SET_DATA01	GPIO Banks 0 and 1 Set Data Register
0x01E2 601C	CLR_DATA01	GPIO Banks 0 and 1 Clear Data Register
0x01E2 6020	IN_DATA01	GPIO Banks 0 and 1 Input Data Register
0x01E2 6024	SET_RIS_TRIG01	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register
0x01E2 6028	CLR_RIS_TRIG01	GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register
0x01E2 602C	SET_FAL_TRIG01	GPIO Banks 0 and 1 Set Falling Edge Interrupt Register
0x01E2 6030	CLR_FAL_TRIG01	GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register
0x01E2 6034	INTSTAT01	GPIO Banks 0 and 1 Interrupt Status Register
GPIO Banks 2 and 3		
0x01E2 6038	DIR23	GPIO Banks 2 and 3 Direction Register
0x01E2 603C	OUT_DATA23	GPIO Banks 2 and 3 Output Data Register
0x01E2 6040	SET_DATA23	GPIO Banks 2 and 3 Set Data Register
0x01E2 6044	CLR_DATA23	GPIO Banks 2 and 3 Clear Data Register
0x01E2 6048	IN_DATA23	GPIO Banks 2 and 3 Input Data Register
0x01E2 604C	SET_RIS_TRIG23	GPIO Banks 2 and 3 Set Rising Edge Interrupt Register
0x01E2 6050	CLR_RIS_TRIG23	GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register
0x01E2 6054	SET_FAL_TRIG23	GPIO Banks 2 and 3 Set Falling Edge Interrupt Register
0x01E2 6058	CLR_FAL_TRIG23	GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register
0x01E2 605C	INTSTAT23	GPIO Banks 2 and 3 Interrupt Status Register
GPIO Banks 4 and 5		
0x01E2 6060	DIR45	GPIO Banks 4 and 5 Direction Register
0x01E2 6064	OUT_DATA45	GPIO Banks 4 and 5 Output Data Register
0x01E2 6068	SET_DATA45	GPIO Banks 4 and 5 Set Data Register
0x01E2 606C	CLR_DATA45	GPIO Banks 4 and 5 Clear Data Register
0x01E2 6070	IN_DATA45	GPIO Banks 4 and 5 Input Data Register
0x01E2 6074	SET_RIS_TRIG45	GPIO Banks 4 and 5 Set Rising Edge Interrupt Register
0x01E2 6078	CLR_RIS_TRIG45	GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register
0x01E2 607C	SET_FAL_TRIG45	GPIO Banks 4 and 5 Set Falling Edge Interrupt Register
0x01E2 6080	CLR_FAL_TRIG45	GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register
0x01E2 6084	INTSTAT45	GPIO Banks 4 and 5 Interrupt Status Register
GPIO Banks 6 and 7		
0x01E2 6088	DIR67	GPIO Banks 6 and 7 Direction Register
0x01E2 608C	OUT_DATA67	GPIO Banks 6 and 7 Output Data Register
0x01E2 6090	SET_DATA67	GPIO Banks 6 and 7 Set Data Register
0x01E2 6094	CLR_DATA67	GPIO Banks 6 and 7 Clear Data Register
0x01E2 6098	IN_DATA67	GPIO Banks 6 and 7 Input Data Register
0x01E2 609C	SET_RIS_TRIG67	GPIO Banks 6 and 7 Set Rising Edge Interrupt Register
0x01E2 60A0	CLR_RIS_TRIG67	GPIO Banks 6 and 7 Clear Rising Edge Interrupt Register
0x01E2 60A4	SET_FAL_TRIG67	GPIO Banks 6 and 7 Set Falling Edge Interrupt Register

Table 6-125. GPIO Registers (continued)

BYTE ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01E2 60A8	CLR_FAL_TRIG67	GPIO Banks 6 and 7 Clear Falling Edge Interrupt Register
0x01E2 60AC	INTSTAT67	GPIO Banks 6 and 7 Interrupt Status Register
GPIO Bank 8		
0x01E2 60B0	DIR8	GPIO Bank 8 Direction Register
0x01E2 60B4	OUT_DATA8	GPIO Bank 8 Output Data Register
0x01E2 60B8	SET_DATA8	GPIO Bank 8 Set Data Register
0x01E2 60BC	CLR_DATA8	GPIO Bank 8 Clear Data Register
0x01E2 60C0	IN_DATA8	GPIO Bank 8 Input Data Register
0x01E2 60C4	SET_RIS_TRIG8	GPIO Bank 8 Set Rising Edge Interrupt Register
0x01E2 60C8	CLR_RIS_TRIG8	GPIO Bank 8 Clear Rising Edge Interrupt Register
0x01E2 60CC	SET_FAL_TRIG8	GPIO Bank 8 Set Falling Edge Interrupt Register
0x01E2 60D0	CLR_FAL_TRIG8	GPIO Bank 8 Clear Falling Edge Interrupt Register
0x01E2 60D4	INTSTAT8	GPIO Bank 8 Interrupt Status Register

6.31.2 GPIO Peripheral Input/Output Electrical Data/Timing

Table 6-126. Timing Requirements for GPIO Inputs[1] (see Figure 6-85)

NO.			1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GP*n*[*m*] as input high	2C[1][2]		ns
2	$t_{w(GPIL)}$	Pulse duration, GP*n*[*m*] as input low	2C[1][2]		ns

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns

Table 6-127. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 6-85)

NO.	PARAMETER		1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GP*n*[*m*] as output high	2C[1] [2]		ns
4	$t_{w(GPOL)}$	Pulse duration, GP*n*[*m*] as output low	2C[1][2]		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns

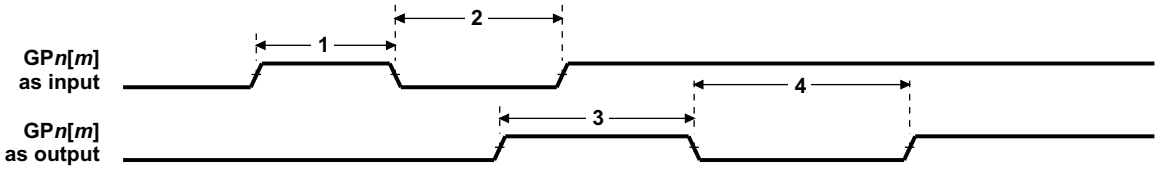


Figure 6-85. GPIO Port Timing

6.31.3 GPIO Peripheral External Interrupts Electrical Data/Timing

Table 6-128. Timing Requirements for External Interrupts[1] (see Figure 6-86)

NO.			1.2V, 1.1V, 1.0V		UNIT
			MIN	MAX	
1	$t_{w(ILOW)}$	Width of the external interrupt pulse low	2C[1][2]		ns
2	$t_{w(IHIGH)}$	Width of the external interrupt pulse high	2C[1][2]		ns

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns

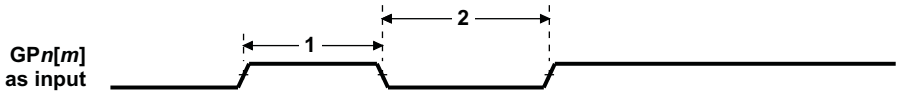


Figure 6-86. GPIO External Interrupt Timing

6.32 Emulation Logic

The debug capabilities and features for DSP are as shown below.

DSP:

- Basic Debug
  - Execution Control
  - System Visibility
- Real-Time Debug
  - Interrupts serviced while halted
  - Low/non-intrusive system visibility while running
- Advanced Debug
  - Global Start
  - Global Stop
  - Specify targeted memory level(s) during memory accesses
  - HSRTDX (High Speed Real Time Data eXchange)
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses
- Analysis Actions
  - Stop program execution
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access

Table 6-129. DSP Debug Features

Category	Hardware Feature	Availability
Basic Debug	Software breakpoint	Unlimited
	Hardware breakpoint	Up to 10 HWBPs, including: 4 precise(1) HWBPs inside DSP core and one of them is associated with a counter. 2 imprecise(1) HWBPs from AET. 4 imprecise(1) HWBPs from AET which are shared for watch point.

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.

Table 6-129. DSP Debug Features (continued)

Category	Hardware Feature	Availability
Analysis	Watch point	Up to 4 watch points, which are shared with HWBPs, and can also be used as 2 watch points with data (32 bits)
	Watch point with Data	Up to 2, Which can also be used as 4 watch points.
	Counters/timers	1x64-bits (cycle only) + 2x32-bits (water mark counters)
	External Event Trigger In	1
	External Event Trigger Out	1

6.32.1 JTAG Port Description

The device target debug interface uses the five standard IEEE 1149.1(JTAG) signals ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO).

TRST holds the debug and boundary scan logic in reset (normal DSP operation) when pulled low (its default state). Since TRST has an internal pull-down resistor, this ensures that at power up the device functions in its normal (non-test) operation mode if TRST is not connected. Otherwise, TRST should be driven inactive by the emulator or boundary scan controller. Boundary scan test cannot be performed while the TRST pin is pulled low.

Table 6-130. JTAG Port Description

PIN	TYPE	NAME	DESCRIPTION
$\overline{\text{TRST}}$	I	Test Logic Reset	When asserted (active low) causes all test and debug logic in the device to be reset along with the IEEE 1149.1 interface
TCK	I	Test Clock	This is the test clock used to drive an IEEE 1149.1 TAP state machine and logic.
TMS	I	Test Mode Select	Directs the next state of the IEEE 1149.1 test access port state machine
TDI	I	Test Data Input	Scan data input to the device
TDO	O	Test Data Output	Scan data output of the device
EMU0	I/O	Emulation 0	Channel 0 trigger + HSRTDX
EMU1	I/O	Emulation 1	Channel 1 trigger + HSRTDX

6.32.2 Scan Chain Configuration Parameters

Table 6-131 shows the TAP configuration details required to configure the router/emulator for this device.

Table 6-131. JTAG Port Description

Router Port ID	Default TAP	TAP Name	Tap IR Length
17	No	C674x	38
19	No	ETB	4

The router is revision C and has a 6-bit IR length.

6.32.3 Initial Scan Chain Configuration

The first level of debug interface that sees the scan controller is the TAP router module. The debugger can configure the TAP router for serially linking up to 16 TAP controllers or individually scanning one of the TAP controllers without disrupting the IR state of the other TAPs.

7 Mechanical Packaging and Orderable Information

This section describes the device orderable part numbers, packaging options, materials, thermal and mechanical parameters.

7.1 Device Support

7.1.1 Development Support

TI offers an extensive line of development tools for the device platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the device applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the device, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C6745). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

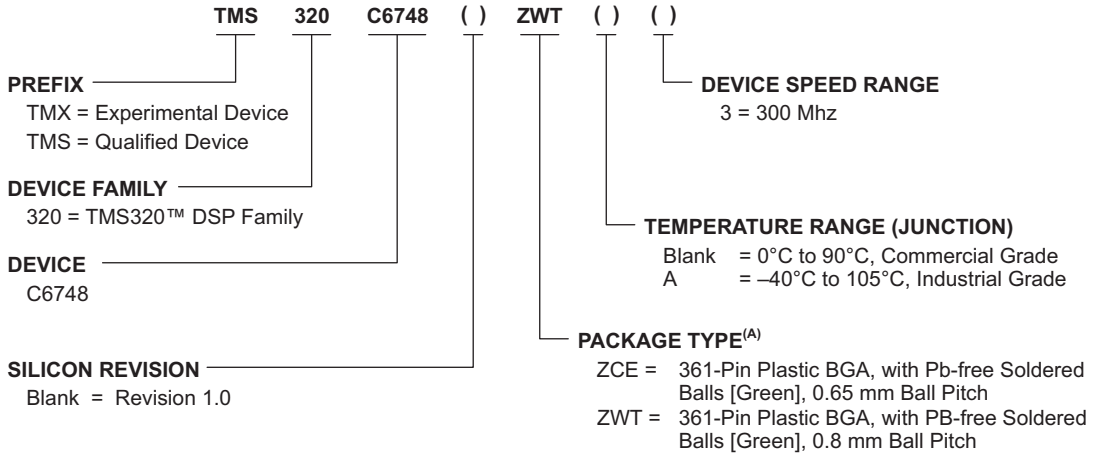
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

PRODUCT PREVIEW

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZWT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default).

Figure 7-1 provides a legend for reading the complete device.



A. BGA = Ball Grid Array

B. The device speed range symbolization indicates the maximum CPU frequency when the core voltage CV_{DD} is set to 1.2 V.

Figure 7-1. Device Nomenclature

7.2 Thermal Data for ZCE Package

The following table(s) show the thermal resistance characteristics for the PBGA–ZCE mechanical package.

Table 7-1. Thermal Resistance Characteristics (PBGA Package) [ZCE]

NO.			°C/W(1)	AIR FLOW (m/s)(2)
1	$R\Theta_{JC}$	Junction-to-case	7.6	N/A
2	$R\Theta_{JB}$	Junction-to-board	11.3	N /A
3	$R\Theta_{JA}$	Junction-to-free air	23.9	0.00
4	$R\Theta_{JMA}$	Junction-to-moving air	21.2	0.50
5			20.3	1.00
6			19.5	2.00
7			18.6	4.00
8	Psi_{JT}	Junction-to-package top	0.2	0.00
9			0.3	0.50
10			0.3	1.00
11			0.4	2.00
12			0.5	4.00
13	Psi_{JB}	Junction-to-board	11.2	0.00
14			11.1	0.50
15			11.1	1.00
16			11.0	2.00
17			10.9	4.00

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 500 mW and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second

7.3 Thermal Data for ZWT Package

The following table(s) show the thermal resistance characteristics for the PBGA–ZWT mechanical package.

Table 7-2. Thermal Resistance Characteristics (PBGA Package) [ZWT]

NO.			°C/W(1)	AIR FLOW (m/s)(2)
1	$R\Theta_{JC}$	Junction-to-case	7.3	N/A
2	$R\Theta_{JB}$	Junction-to-board	12.4	N /A
3	$R\Theta_{JA}$	Junction-to-free air	23.7	0.00
4	$R\Theta_{JMA}$	Junction-to-moving air	21.0	0.50
5			20.1	1.00
6			19.3	2.00
7			18.4	4.00
8	Psi_{JT}	Junction-to-package top	0.2	0.00
9			0.3	0.50
10			0.3	1.00
11			0.4	2.00
12			0.5	4.00
13	Psi_{JB}	Junction-to-board	12.3	0.00
14			12.2	0.50
15			12.1	1.00
16			12.0	2.00
17			11.9	4.00

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 1W and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second

PACKAGING INFORMATION

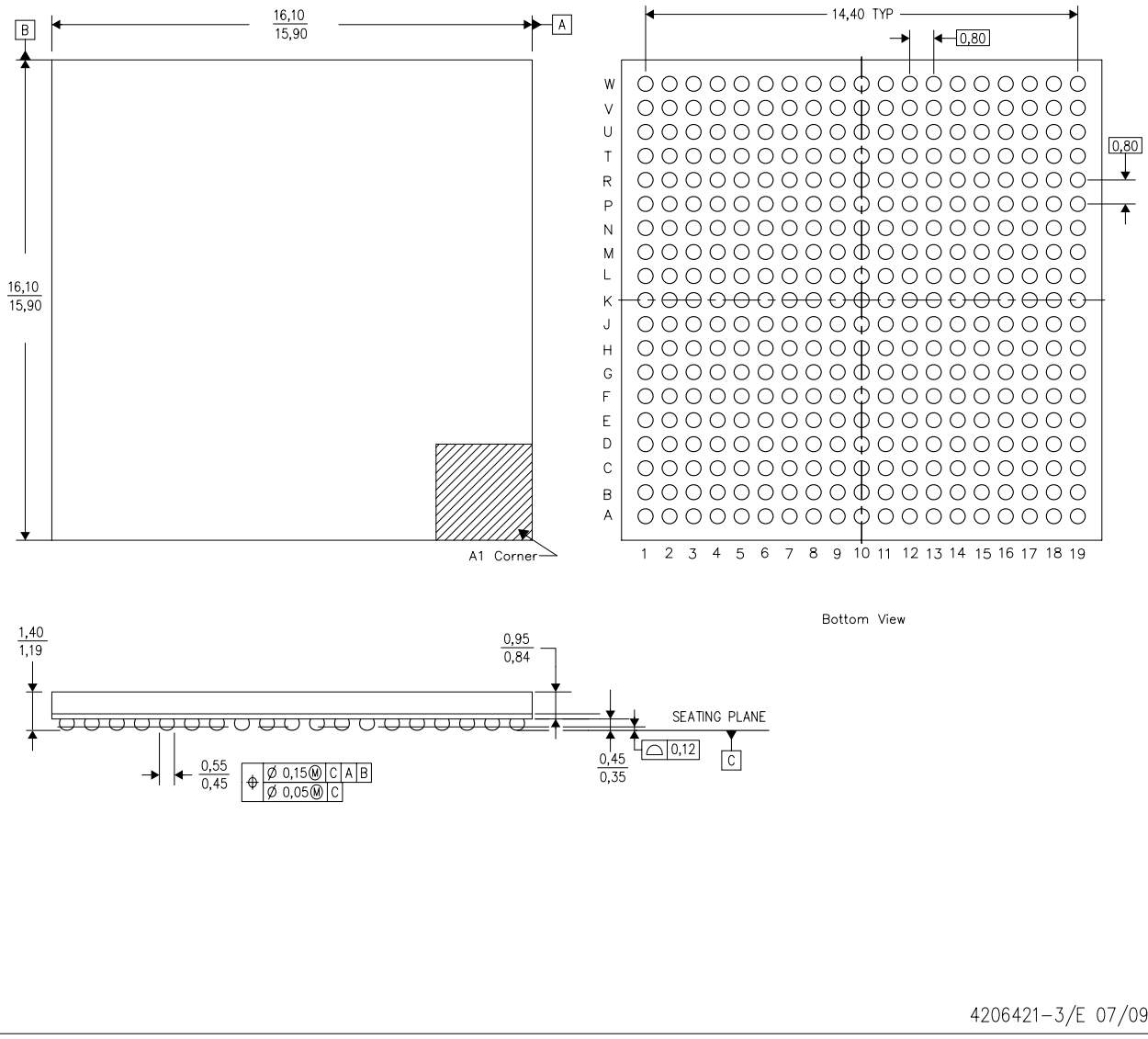
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMX320C6748ZCE	ACTIVE	NFBGA	ZCE	361	160	TBD	Call TI	Call TI
TMX320C6748ZWT	ACTIVE	NFBGA	ZWT	361	90	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

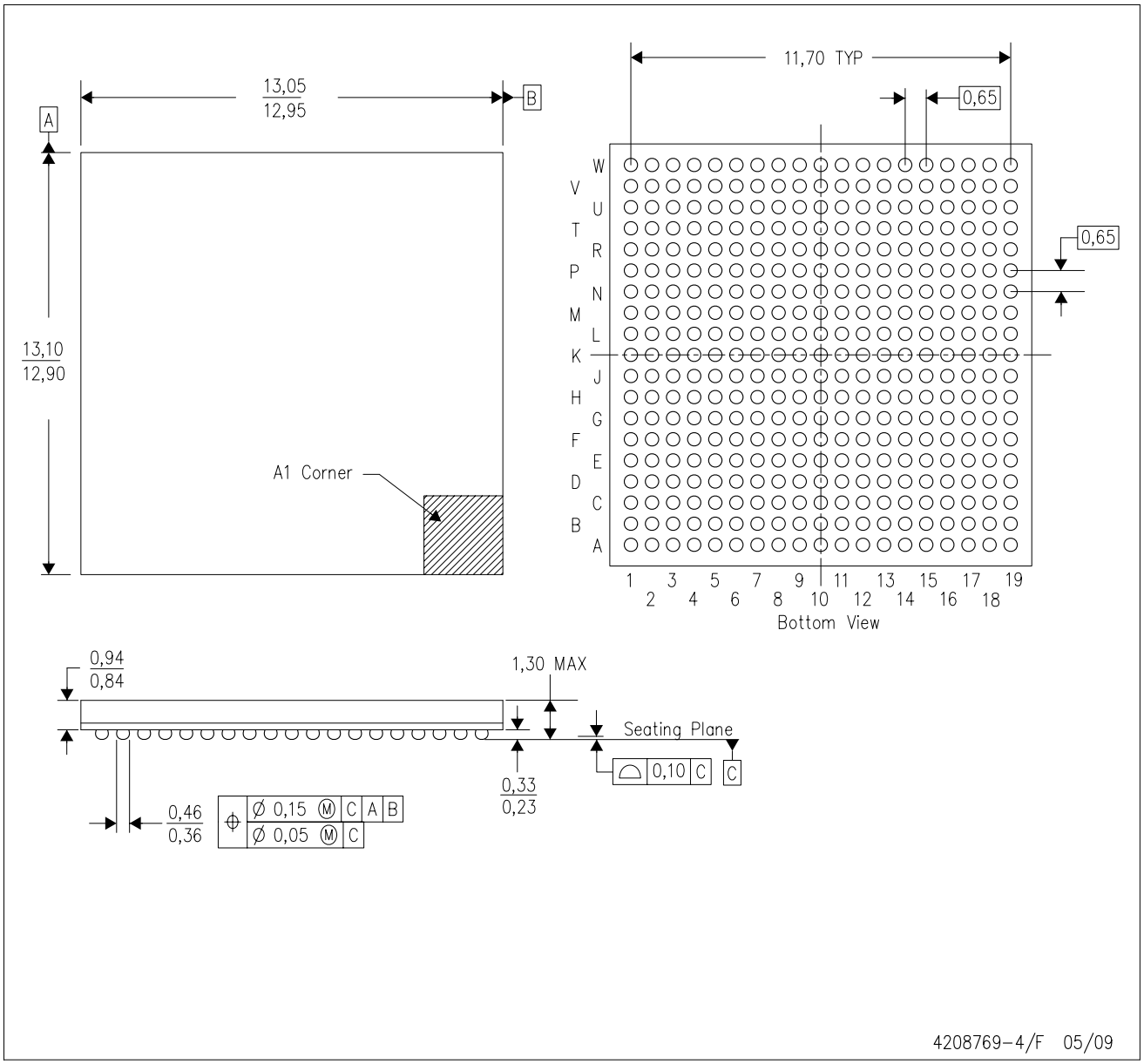
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZWT (S–PBGA–N361) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.
D. Falls within JEDEC MO–275.

ZCE (S–PBGA–N361) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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