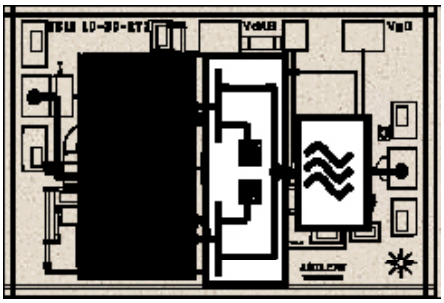
AMMC-6140

20 – 40 GHz Output x2 Active Frequency Multiplier

Data Sheet



Chip Size:	1300 x 900 µm (51 x 35 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	100 ± 10 µm (4 ± 0.4 mils)
Pad Dimensions:	120 x 80 µm (5x3 ±0.4 mils)

Description

Avago's AMMC-6140 is an easy-to-use x2 active frequency multiplier MMIC designed for commercial communication systems. The MMIC takes a 10 to 20 GHz input signal and doubles it to 20 to 40 GHz. It could also be used between 9–10 GHz and 20–22 GHz with slight degradation in Conversion Loss or Fundamental Suppression. It has an integrated matching, harmonic suppression, and bias network. The input/output are matched to 50Ω and fully DC blocked. The MMIC is fabricated using PHEMT technology. The backside of this die is both RF and DC ground. This helps simplify the assembly process and reduces assembly-related performance variations and costs. For improved reliability and moisture protection, the die is passivated at the active areas. This MMIC is a cost effective alternative to bulky hybrid FET and diode doublers that require high input drive levels, have high conversion loss and poor fundamental suppression.

Features

- Input frequency range: 10 – 20 GHz
- Broad input power range: -9 to +7 dBm
- Output power: -1 to 0 dBm (Pin = +4dB)
- Fundamental suppression of 25 dBc
- 50Ω input and output match
- Supply bias of -1.2V, 4.5V and 27 mA

Applications

- Microwave radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops
- Commercial grade military

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_d	Positive Drain Voltage	V		7
V_g	Gate Supply Voltage	V	-3.0	0.5
I_d	Drain Current	mA		-3
P_{in}	CW Input Power	dBm		15
T_{ch}	Operating Channel Temperature	°C		+150
T_{stg}	Storage Case Temperature	°C	-65	+150
T_{max}	Maximum Assembly Temp (60 sec max)	°C		+300

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 0)

Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

AMMC-6140 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_d	Drain Supply Current (under any RF power drive and temperature) (V_d = 4.5V)	mA		27	40
V_g	Gate Supply Operating Voltage	V	-1.5	-1.2	-1.0
θ_{ch-b}	Thermal Resistance[2] (Backside Temp. T_b = 25°C)	°C/W		25	

Notes:

1. Ambient operational temperature T_A = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (θ_{ch-b}) = 26°C/W at $T_{channel}$ (T_c) = 34°C as measured using infrared microscopy. Thermal Resistance at backside temperature (T_b) = 25°C calculated from measured data.

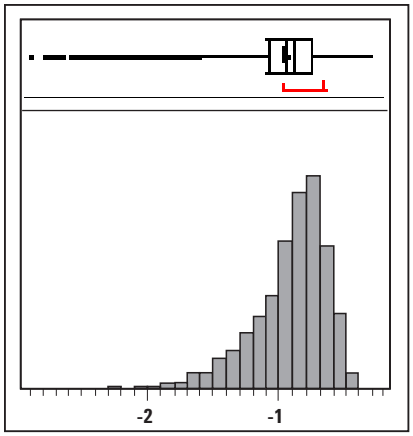
RF Specifications[3, 4, 5] (T_A = 25°C, V_d = 4.5 V, $I_{d(Q)}$ = 27 mA, Z_0 = 50Ω)

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Sigma
Fin	Input Frequency	GHz		10 to 20	
Fout	Output Frequency	GHz		20 to 40	
Po	Output Power[6]	dBm	-2	-1	0.4
Fo	Fundamental Isolation (referenced to Po): 20 – 36 GHz	dBc	20	30	5.0
	36–40 GHz	dBc	14	16	1.0
3Fo	3rd Harmonic Isolation (referenced to Po)	dBc		25	1.2
P_{-1dB}	Output Power at 1dB Gain Compression	dBm		+5	
RLin	Input Return Loss[6]	dB		-15	
RLout	Output Return Loss[6]	dB		-10	
SSB	Single Sideband Phase Noise (100 KHz offset)	dBc/Hz		-135	

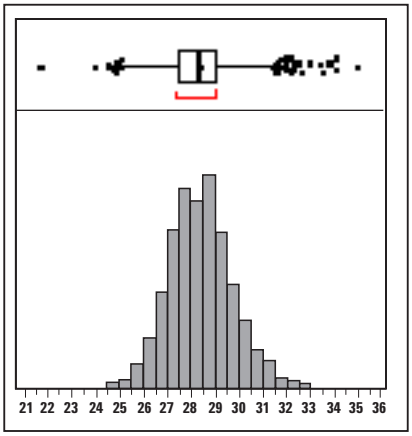
Notes:

3. Small/large signal data measured in wafer form T_A = 25°C.
4. 100% on-wafer RF test is done at Pin = +4 dBm and output frequency = 20, 28, 36 and 40 GHz.
5. Specifications are derived from measurements in a 50Ω test environment. Aspects of the multiplier performance may be improved over a narrower bandwidth by application of additional matching.

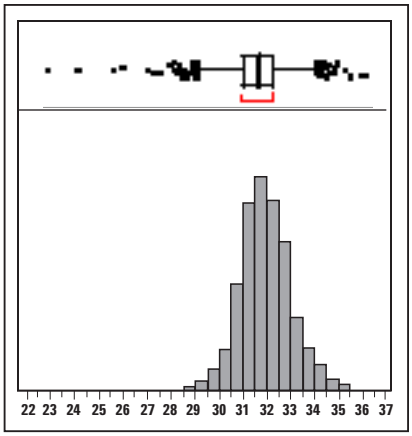
Typical distribution of Pout, 2nd Harmonic and 3rd Harmonic Suppression (Fin = 14 GHz).
Based on 2500 parts sampled over several production lots.



2Fo Pout (dBm) @ 28G Hz



Fo Suppression (dBm) @ 14 GHz



3Fo Suppression (dBm) @ 42 GHz

AMMC-6140 Typical Performances (T_A = 25°C, V_d =4 .5V, I_D = 27 mA, Vg = -1.2V, Z_{in} = Z_{out} = 50Ω unless otherwise stated)

NOTE: These measurements are in a 50Ω test environment. Aspects of the multiplier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

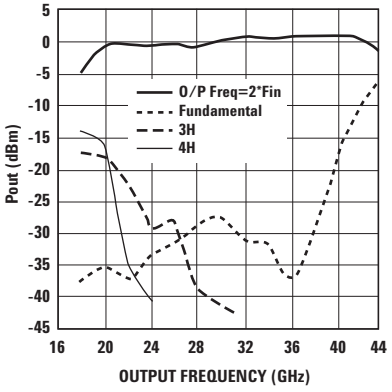


Figure 1. Typical Output Power against Fundamental, 3rd, and 4th Harmonic suppression (P_{in}=3 dBm) vs. Frequency.

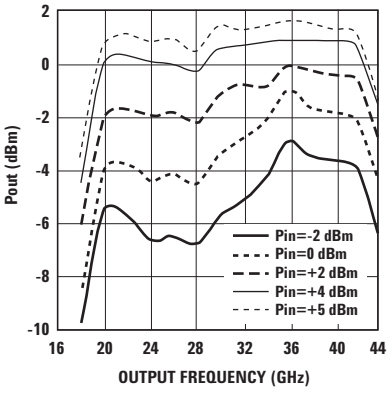


Figure 2. Typical Output Power at different Fundamental Input Power vs. Frequency.

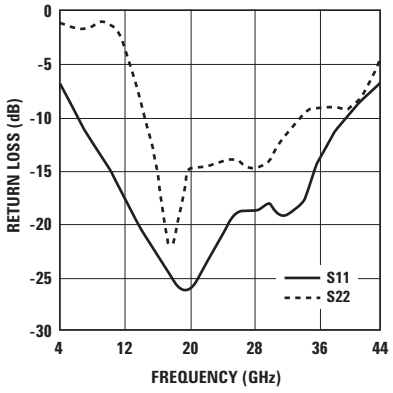


Figure 3. Typical Input & Output Return Loss.

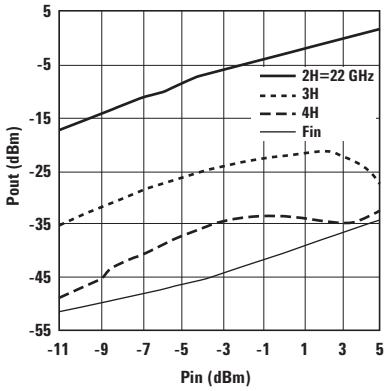


Figure 4. Typical Output Power against Fundamental 3rd and 4th Harmonic suppression vs. P_{in} (2H=22 GHz).

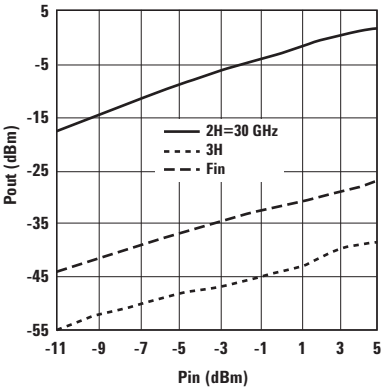


Figure 5. Typical Output Power against Fundamental and 3rd Harmonic vs. P_{in} (2H=30 GHz).

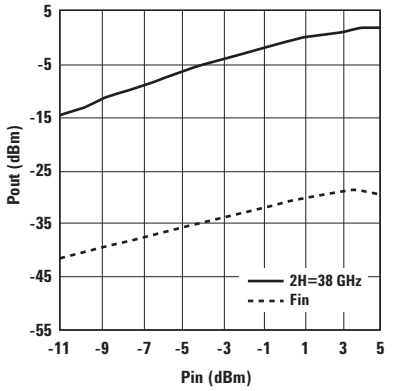


Figure 6. Typical Output Power against Fundamental vs. P_{in} (2H=38 GHz).

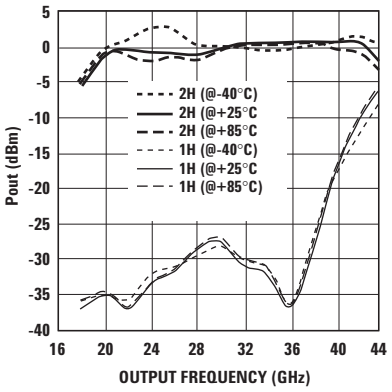


Figure 7. Typical Output Power and Fundamental Suppression vs. Temperature.

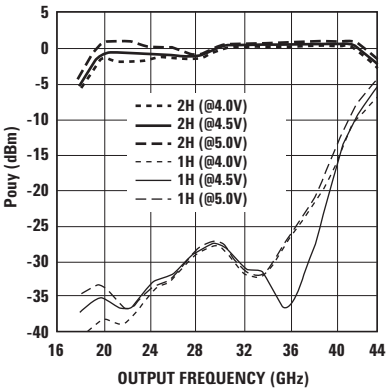


Figure 8. Typical Output Power and Fundamental Suppression vs. Vdd.

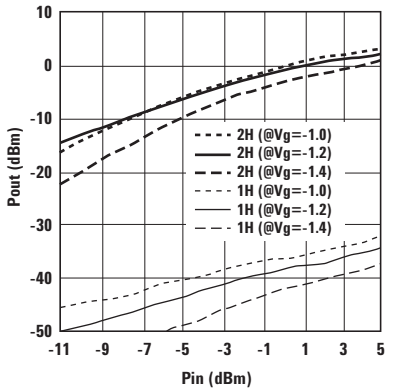
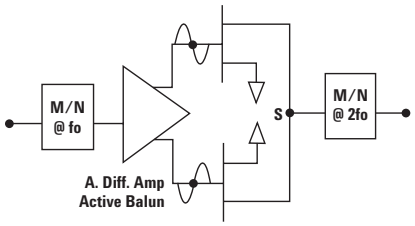


Figure 9. Typical Pout and Fundamental Suppression vs. Vg (Fout=38 GHz).

Biasing and Operation



The frequency doubler MMIC consists of a differential amplifier circuit that acts as an active balun. The outputs of this balun feed the gates of balanced FETs and the drains are connected to form the single-ended output. This results in the fundamental frequency and odd harmonics canceling and the even harmonic drain currents (in phase) adding in superposition. Node 'S' acts as a virtual ground. An input matching network (M/N) is designed to provide good match at fundamental frequencies and produces high impedance mismatch at higher harmonics.

AMMC-6140 is biased with a single positive drain supply and single negative gate supply using separate bypass capacitors. It is normally biased with the drain supply connected to the V_{DD} bond pad and the gate supply connected to the V_{gg} bond pad. It is important to have the 100 pF bypass capacitor and it should be placed as close to the die as possible. Typical bias connections are shown in Figure 12. For most of the application it is recommended to use a Vg = -1.2V and Vd=4.5V.

The AMMC-6140 performance changes very slightly with Drain (Vd) and Gate bias (Vg) as shown in Figures 8 and 9. Minor improvements in performance are possible for output power or fundamental suppression by optimizing the Vg from -1.0V to -1.4V and/or Vd from 4.0 to 5.0V.

The RF input and output ports are AC coupled, thus no DC voltage is present at either port. However, the RF output port has an internal output matching circuit that presents a DC short. Proper care should be taken while biasing a sequential circuit to the AMMC-6140 as it might cause a DC short (Use a DC block if sub sequential circuit is not AC coupled). No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Assembly Techniques

The backside of the MMIC chip is RF ground. For microstrip applications the chip should be attached directly to the ground plane (e.g. circuit carrier or heatsink) using electrically conductive epoxy[1].

For best performance, the topside of the MMIC should be brought up to the same height as the circuit surrounding it. This can be accomplished by mounting a gold plate metal shim (same length and width as the MMIC) under the chip which is of correct thickness to make the chip and adjacent circuit the same height. The amount of epoxy used for the chip and/or shim attachment should be just enough to provide a thin fillet around the bottom perimeter of the chip or shim. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment.

The location of the RF bond pads is shown in Figure 12. Note that all the RF input and output ports are in a Ground-Signal-Ground configuration.

RF connections should be kept as short as reasonable to minimize performance degradation due to undesirable series inductance. A single bond wire is normally sufficient for signal connections, however double bonding with 0.7 mil gold wire or use of gold mesh[2] is recommended for best performance, especially near the high end of the frequency band.

Thermosonic wedge bonding is the preferred method for wire attachment to the bond pads. Gold mesh can be attached using a 2 mil round tracking tool and a tool force of approximately 22 grams and a ultrasonic power of roughly 55 dB for a duration of 76 ± 8 mS. The guided wedge at an untrasonic power level of 64 dB can be used for 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

The chip is 100 µm thick and should be handled with care. This MMIC has exposed air bridges on the top surface and should be handled by the edges or with a custom collet (do not pick up the die with a vacuum on die center).

This MMIC is also static sensitive and ESD precautions should be taken.

Notes:

1. Ablebond 84-1 LM1 silver epoxy is recommended.
2. Buckbee-Mears Corporation, St. Paul, MN, 800-262-3824

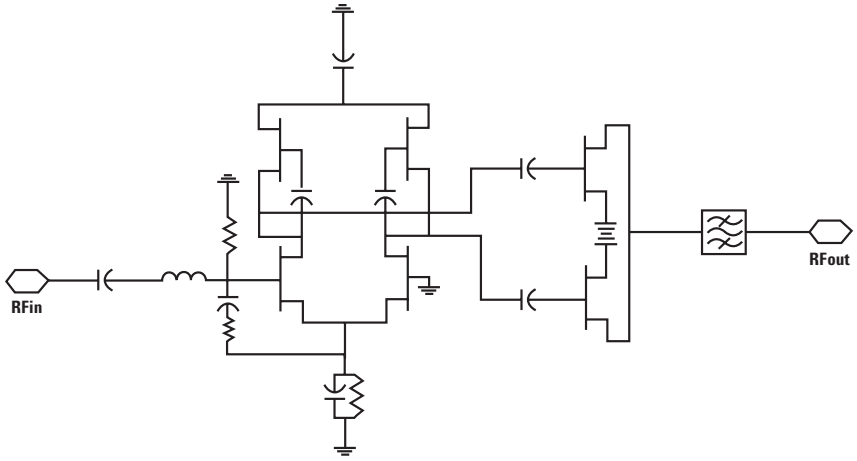


Figure 10. AMMC-6140 simplified schematic.

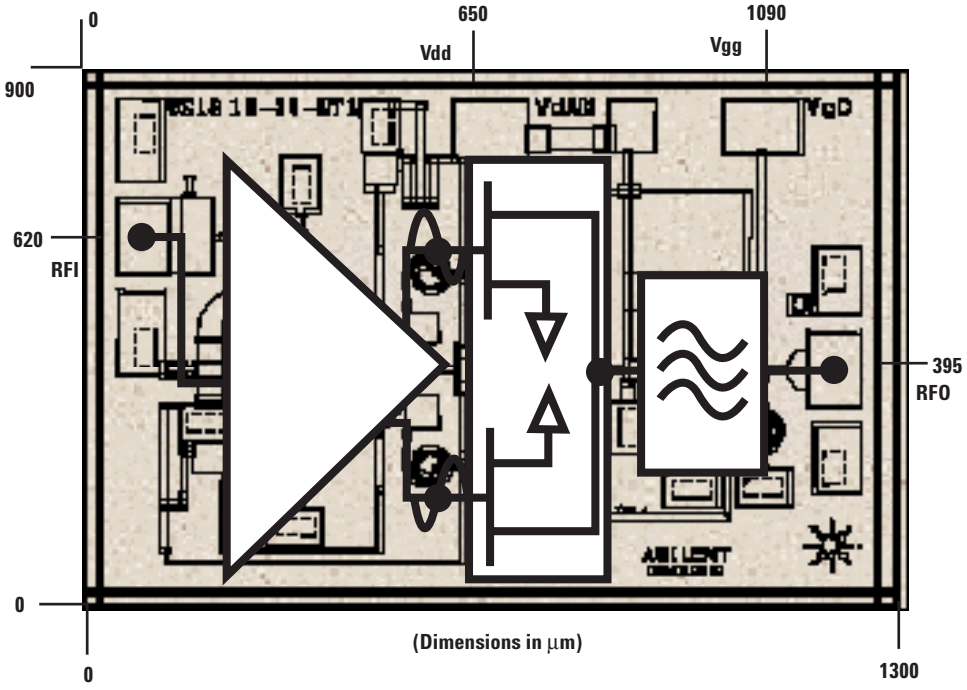


Figure 11. AMMC-6140 Bonding Pad Locations.

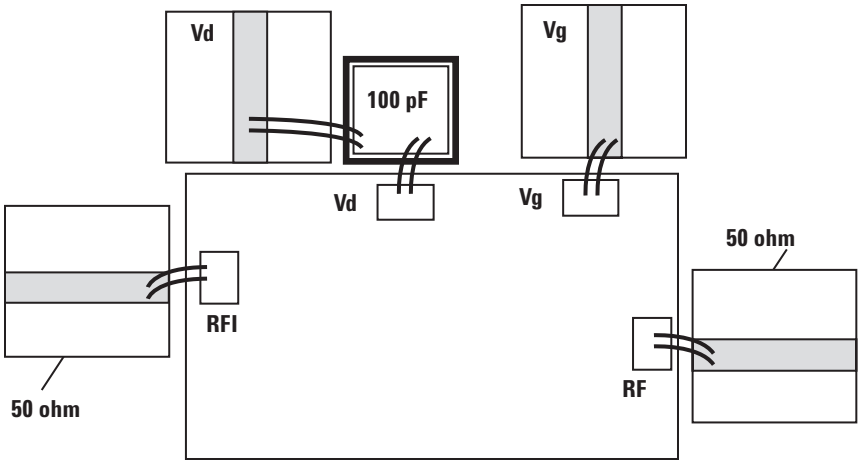


Figure 12. AMMC-6140 Assembly Diagram.

Note: 0.1uF capacitors on gate and drain lines, not shown, required.

Ordering Information

AMMC-6140-W10 = 10 devices per tray
AMMC-6140-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0701EN - September 12, 2007