



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{iss}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain
- ▶ Complementary N- and P-Channel devices
- ▶ Hi-Rel processing available

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

The Supertex 2N6661 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

| Device | Package Option | $BV_{DSS}/BV_{DGS}$<br>(V) | $R_{DS(ON)}$<br>(max)<br>( $\Omega$ ) | $I_{D(ON)}$<br>(min)<br>(A) |
|--------|----------------|----------------------------|---------------------------------------|-----------------------------|
| 2N6661 | TO-39          | 90                         | 4.0                                   | 1.5                         |

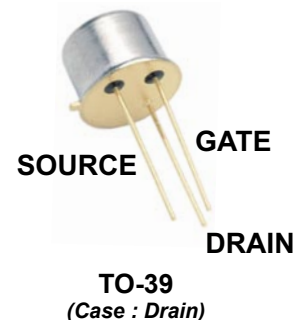
### Absolute Maximum Ratings

| Parameter                         | Value                             |
|-----------------------------------|-----------------------------------|
| Drain-to-source voltage           | $BV_{DSS}$                        |
| Drain-to-gate voltage             | $BV_{DGS}$                        |
| Gate-to-source voltage            | $\pm 20V$                         |
| Operating and storage temperature | $-55^{\circ}C$ to $+150^{\circ}C$ |
| Soldering temperature*            | $+300^{\circ}C$                   |

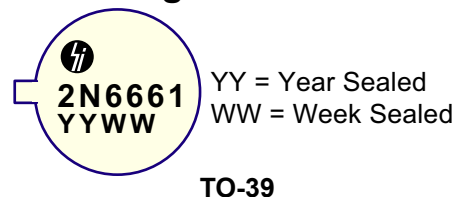
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Pin Configuration



### Product Marking



## Thermal Characteristics

| Package | $I_D$<br>(continuous) <sup>†</sup><br>(mA) | $I_D$<br>(pulsed)<br>(A) | Power Dissipation<br>@ $T_c = 25^\circ\text{C}$<br>(W) | $\theta_{jc}$<br>( $^\circ\text{C}/\text{W}$ ) | $\theta_{ja}$<br>( $^\circ\text{C}/\text{W}$ ) | $I_{DR}^\dagger$<br>(mA) | $I_{DRM}$<br>(A) |
|---------|--|--------------------------|--|--|--|--------------------------|------------------|
| TO-39   | 350  | 3.0                      | 6.25   | 20   | 125  | 350                      | 3.0              |

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_f$ .

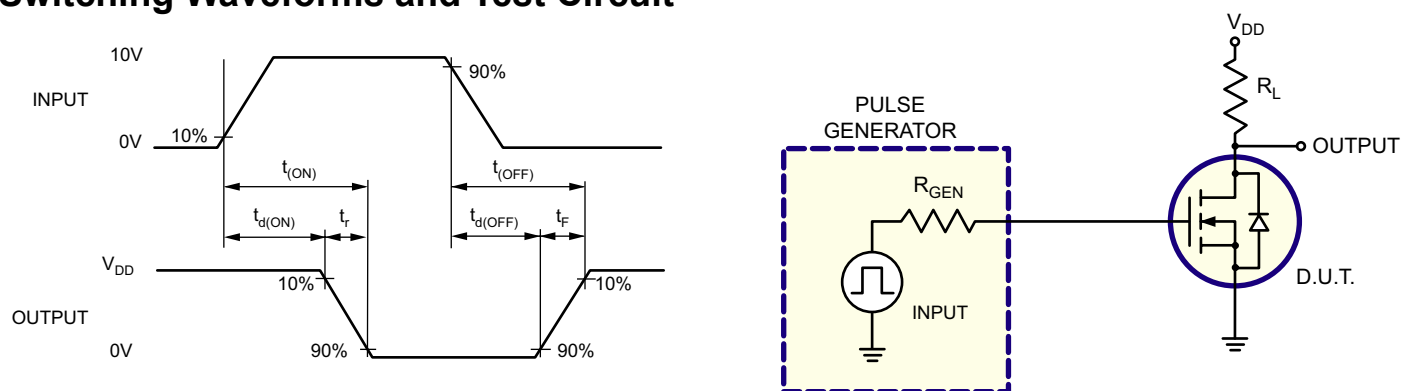
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym                 | Parameter                                  | Min | Typ  | Max  | Units                | Conditions  |
|---------------------|--|-----|------|------|----------------------|---|
| $BV_{DSS}$          | Drain-to-source breakdown voltage          | 90  | -    | -    | V                    | $V_{GS} = 0V, I_D = 10\mu\text{A}$                                      |
| $V_{GS(th)}$        | Gate threshold voltage                     | 0.8 | -    | 2.0  | V                    | $V_{GS} = V_{DS}, I_D = 1.0\text{mA}$                                   |
| $\Delta V_{GS(th)}$ | $V_{GS(th)}$ change with temperature       | -   | -3.8 | -5.5 | mV/ $^\circ\text{C}$ | $V_{GS} = V_{DS}, I_D = 1.0\text{mA}$                                   |
| $I_{GSS}$           | Gate body leakage current                  | -   | -    | 100  | nA                   | $V_{GS} = \pm 20V, V_{DS} = 0V$   |
| $I_{DSS}$           | Zero gate voltage drain current            | -   | -    | 10   | $\mu\text{A}$        | $V_{GS} = 0V, V_{DS} = \text{Max rating}$                               |
|                     |  | -   | -    | 500  |                      | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$         | On-state drain current                     | 1.5 | -    | -    | A                    | $V_{GS} = 10V, V_{DS} = 10V$  |
| $R_{DS(ON)}$        | Static drain-to-source on-state resistance | -   | -    | 5.0  | $\Omega$             | $V_{GS} = 5.0V, I_D = 0.3A$   |
|                     |  | -   | -    | 4.0  |                      | $V_{GS} = 10V, I_D = 1.0A$  |
| $G_{FS}$            | Forward transconductance                   | 170 | -    | -    | mmho                 | $V_{DS} = 25V, I_D = 0.5A$  |
| $C_{ISS}$           | Input capacitance                          | -   | -    | 50   | pF                   | $V_{GS} = 0V, V_{DS} = 24V, f = 1.0\text{MHz}$                          |
| $C_{OSS}$           | Common source output capacitance           | -   | -    | 40   |                      |   |
| $C_{RSS}$           | Reverse transfer capacitance               | -   | -    | 10   |                      |   |
| $t_{(ON)}$          | Turn-on time                               | -   | -    | 10   | ns                   | $V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25\Omega$                          |
| $t_{(OFF)}$         | Turn-off time                              | -   | -    | 10   |                      |   |
| $V_{SD}$            | Diode forward voltage drop                 | -   | 1.2  | -    | V                    | $V_{GS} = 0V, I_{SD} = 1.0A$  |
| $t_{rr}$            | Reverse recovery time                      | -   | 350  | -    | ns                   | $V_{GS} = 0V, I_{SD} = 1.0A$  |

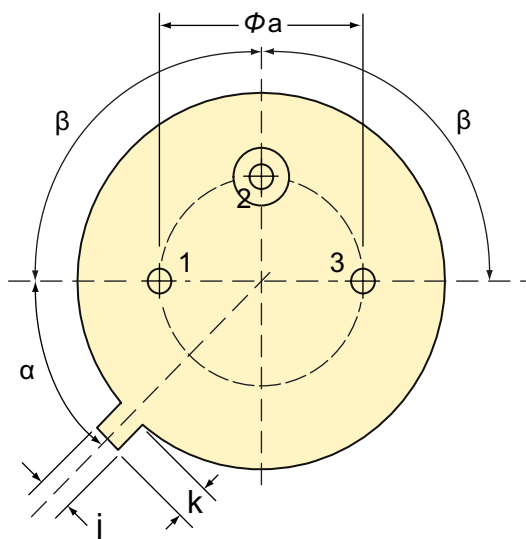
### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

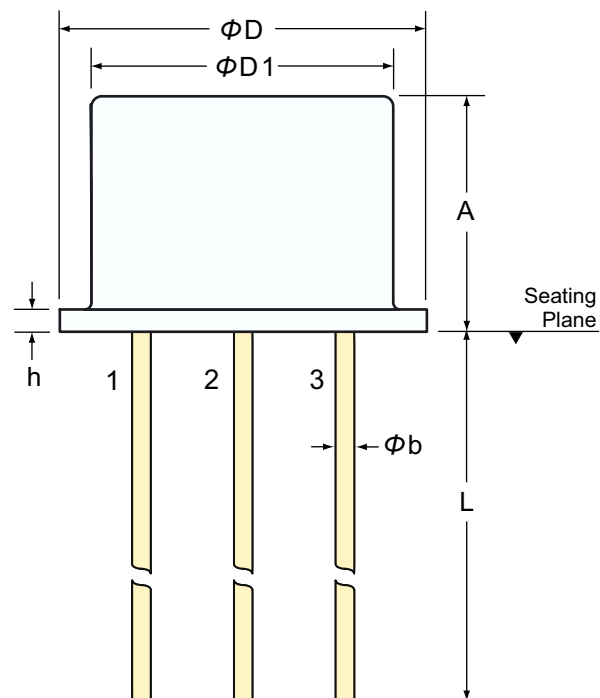
## Switching Waveforms and Test Circuit



## 3-Lead TO-39 Package Outline (N2)



**Bottom View**



**Side View**

| Symbol             | $\alpha$ | $\beta$    | A          | $\phi a$ | $\phi b$ | $\phi D$ | $\phi D1$ | h    | j    | k    | L    |       |
|--------------------|----------|------------|------------|----------|----------|----------|-----------|------|------|------|------|-------|
| Dimension (inches) | MIN      | 45°<br>NOM | 90°<br>NOM | .240     | .190     | .016     | .350      | .315 | .009 | .028 | .029 | .500  |
|                    | NOM      |            |            | -        | -        | -        | -         | -    | -    | -    | -    | -     |
|                    | MAX      |            |            | .260     | .210     | .021     | .370      | .335 | .125 | .034 | .040 | .560* |

JEDEC Registration TO-39.

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO39N2, Version A081208.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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