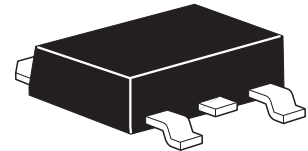


ZXMP10A18K

100V DPAK P-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
-100	0.150 @ $V_{GS} = -10V$	-5.9
	0.190 @ $V_{GS} = -6V$	-5.2



Description

This new generation trench MOSFET from Zetex features a unique structure combining the benefits of low on-resistance and fast switching, making it ideal for high efficiency power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- DPAK package

Applications

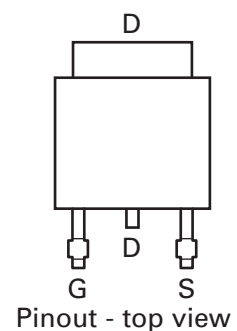
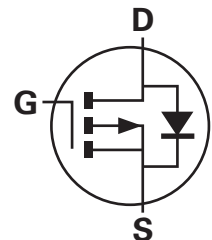
- DC-DC converters
- Power management functions
- Disconnect switches
- Motor control

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMP10A18KTC	13	16	2,500

Device marking

ZXMP
10A18



ZXMP10A18K

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	-100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS} = 10V$; $T_{amb} = 25^{\circ}C^{(b)}$	I_D	-5.9	A
@ $V_{GS} = 10V$; $T_{amb} = 70^{\circ}C^{(b)}$		-4.7	
@ $V_{GS} = 10V$; $T_{amb} = 25^{\circ}C^{(a)}$		-3.8	
Pulsed drain current ^(c)	I_{DM}	-21.1	A
Continuous source current (body diode) ^(b)	I_S	-10	A
Pulsed source current (body diode) ^(c)	I_{SM}	-21.1	A
Power dissipation at $T_{amb} = 25^{\circ}C^{(a)}$	P_D	4.3	W
Linear derating factor		34.4	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(b)}$	P_D	10.2	W
Linear derating factor		81.3	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(d)}$	P_D	2.17	W
Linear derating factor		17.4	mW/ $^{\circ}C$
Operating and storage temperature range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

Thermal resistance

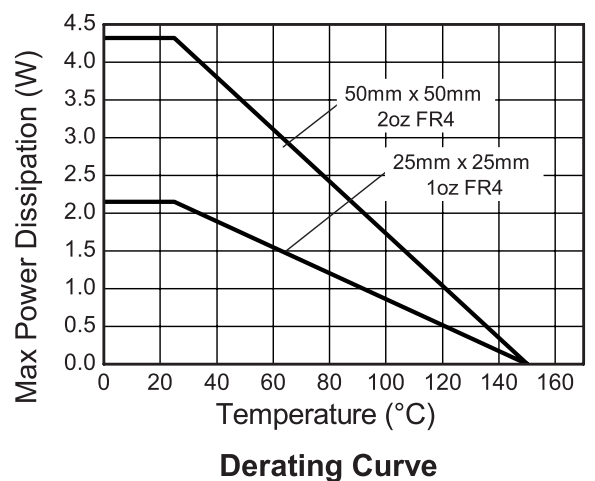
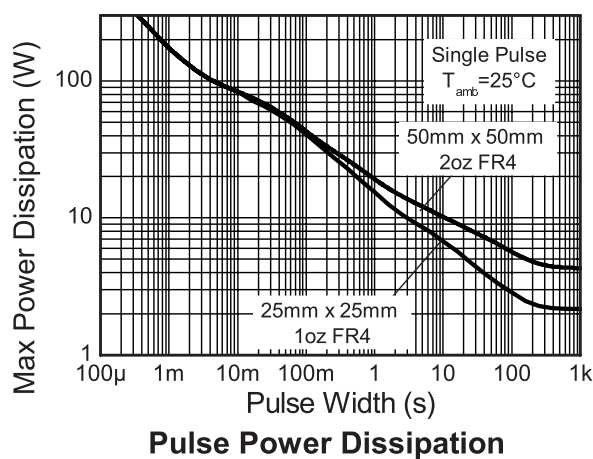
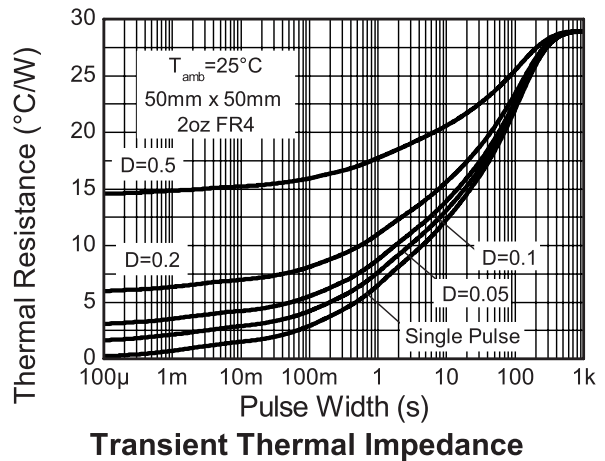
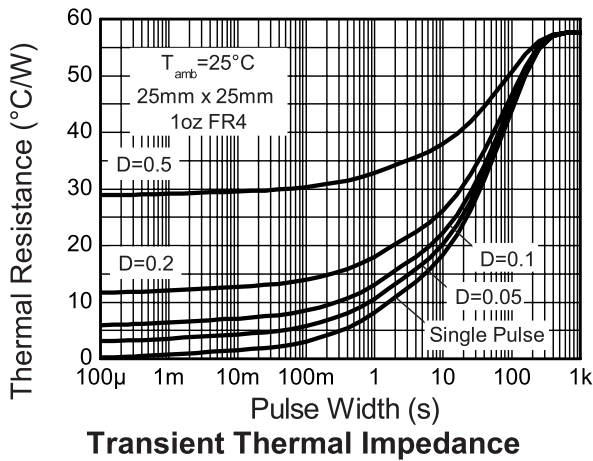
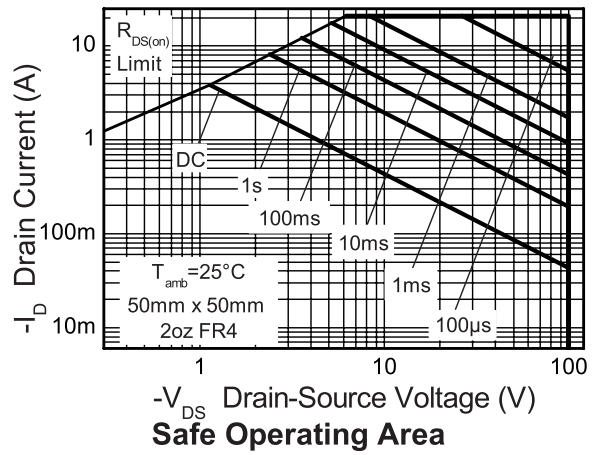
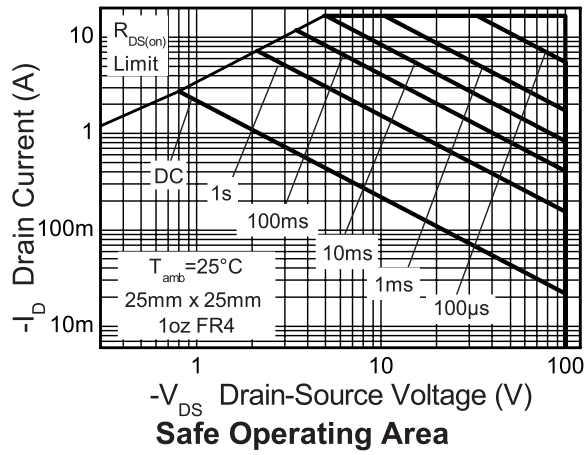
Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	29	$^{\circ}C/W$
Junction to ambient ^(b)	$R_{\theta JA}$	12.3	$^{\circ}C/W$
Junction to ambient ^(d)	$R_{\theta JA}$	57.6	$^{\circ}C/W$

NOTES:

- (a) For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating 50mm x 50mm x 1.6mm FR4 PCB, $D=0.02$ pulse width=300 μs - pulse width limited by maximum junction temperature.
- (d) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

ZXMP10A18K

Thermal characteristics



ZXMP10A18K

Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100			V	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero gate voltage drain current	I_{DSS}			-1	μA	$V_{DS} = -100\text{V}$, $V_{GS} = 0\text{V}$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Gate-source threshold voltage	$V_{GS(th)}$	-2.0		-4.0	V	$I_D = -250\mu\text{A}$, $V_{DS} = V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.150 0.190	Ω	$V_{GS} = -10\text{V}$, $I_D = -2.8\text{A}$ $V_{GS} = -6\text{V}$, $I_D = -2.4\text{A}$
Forward transconductance ^{(*)(‡)}	g_{fs}		6.0		S	$V_{DS} = -15\text{V}$, $I_D = -2.8\text{A}$
Dynamic^(‡) (3)						
Input capacitance	C_{iss}		1055		pF	$V_{DS} = -50\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		90		pF	
Reverse transfer capacitance	C_{rss}		76		pF	
Switching^(†) (‡)						
Turn-on-delay time	$t_{d(on)}$		4.9		ns	$V_{DD} = -50\text{V}$, $I_D = -1\text{A}$ $R_G = 6.0\Omega$, $V_{GS} = -10\text{V}$
Rise time	t_r		6.8		ns	
Turn-off delay time	$t_{d(off)}$		33.9		ns	
Fall time	t_f		17.9		ns	
Total gate charge	Q_g		26.9		nC	$V_{DS} = -50\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -2.8\text{A}$
Gate-source charge	Q_{gs}		3.9		nC	
Gate drain charge	Q_{gd}		10.2		nC	
Source-drain diode						
Diode forward voltage ^(*)	V_{SD}		-0.85	-0.95	V	$T_j = 25^{\circ}\text{C}$, $I_S = -3.5\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time ^(‡)	t_{rr}		49		ns	$T_j = 25^{\circ}\text{C}$, $I_S = -2.8\text{A}$, $di/dt = 100\text{A/ms}$
Reverse recovery charge ^(‡)	Q_{rr}		107		nC	

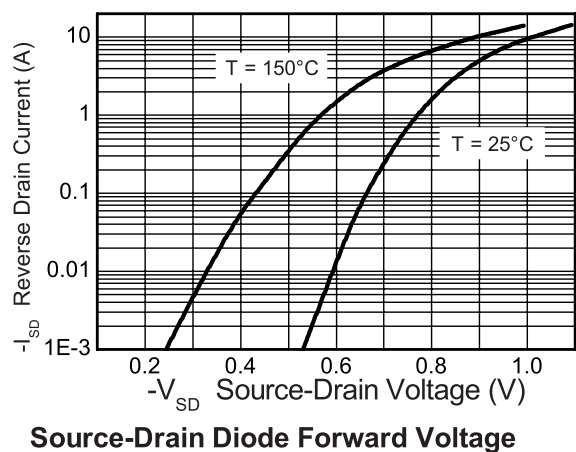
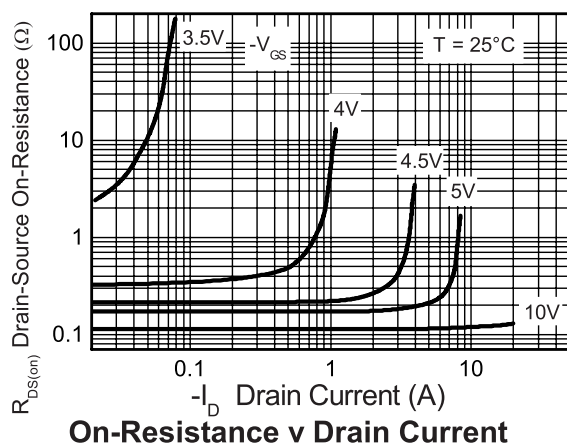
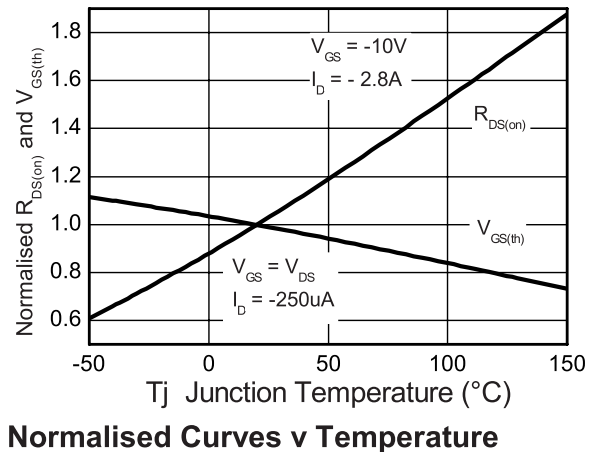
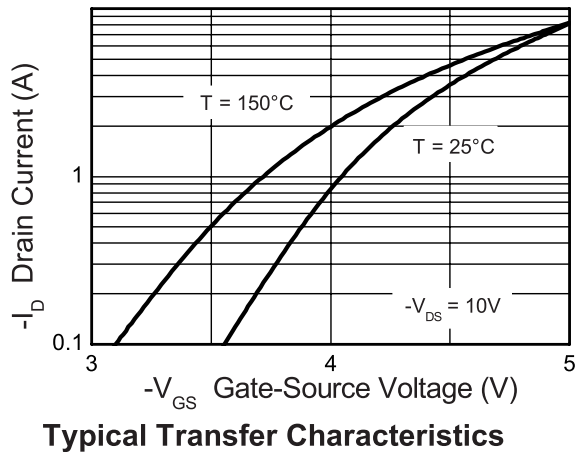
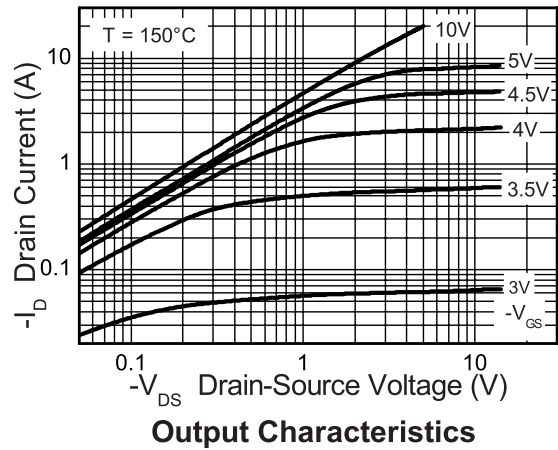
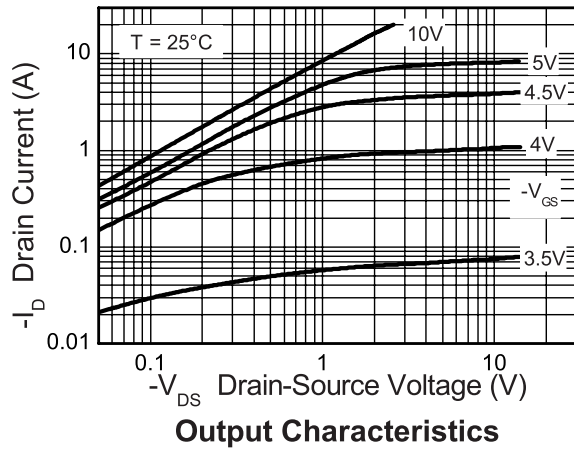
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$

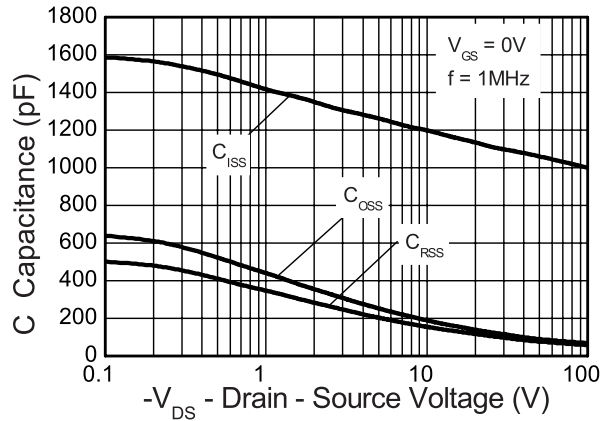
(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing.

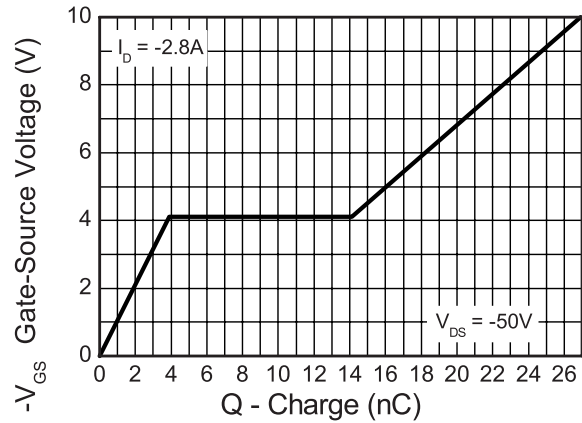
Typical characteristics



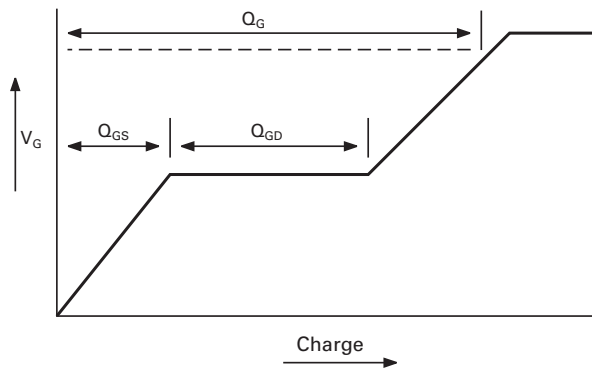
Typical characteristics



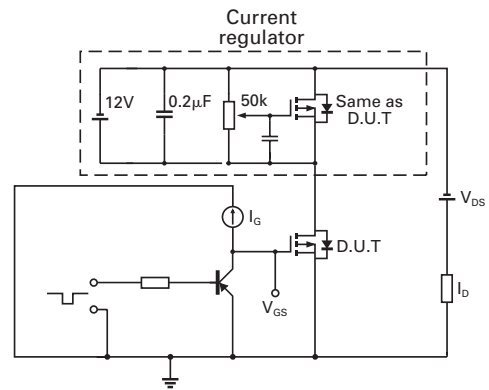
Capacitance v Drain-Source Voltage



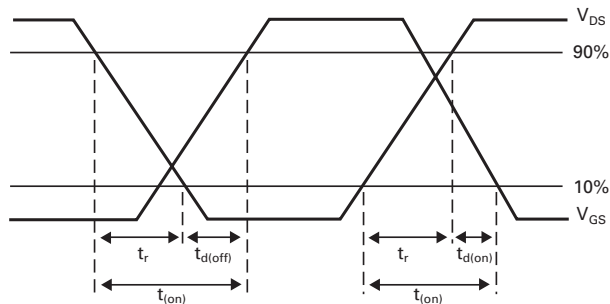
Gate-Source Voltage v Gate Charge



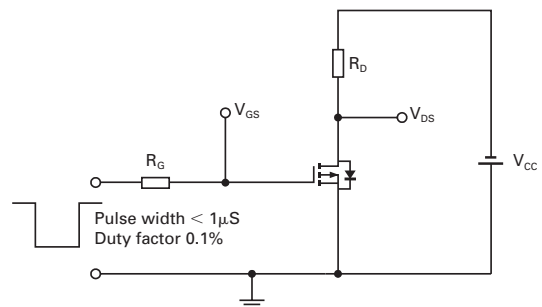
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



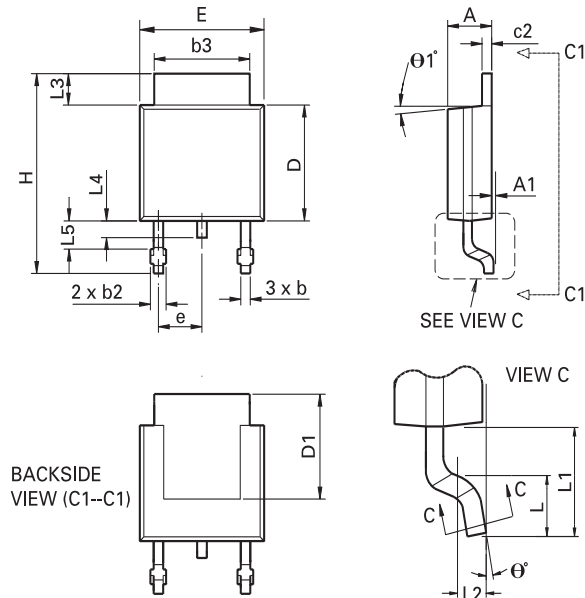
Switching time test circuit

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Package outline - DPAK



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.086	0.094	2.18	2.39	e	0.090 BSC		2.29 BSC	
A1	-	0.005	-	0.127	H	0.370	0.410	9.40	10.41
b	0.020	0.035	0.508	0.89	L	0.055	0.070	1.40	1.78
b2	0.030	0.045	0.762	1.14	L1	0.108 REF		2.74 REF	
b3	0.205	0.215	5.21	5.46	L2	0.020 BSC		0.508 BSC	
c	0.018	0.024	0.457	0.61	L3	0.035	0.065	0.89	1.65
c2	0.018	0.023	0.457	0.584	L4	0.025	0.040	0.635	1.016
D	0.213	0.245	5.41	6.22	L5	0.045	0.060	1.14	1.52
D1	0.205	-	5.21	-	theta 1°	0°	10°	0°	10°
E	0.250	0.265	6.35	6.73	theta 0°	0°	15°	0°	15°
E1	0.170	-	4.32	-	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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