ATF-501P8

High Linearity Enhancement Mode[1] Pseudomorphic HEMT in 2x2 mm^2 LPCC[3] Package

Data Sheet

Description

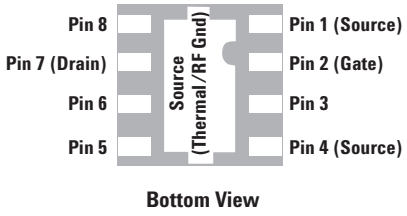
Avago Technologies's ATF-501P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC-standard leadless plastic chip carrier (LPCC[3]) package. The device is ideal as a medium-power amplifier. Its operating frequency range is from 400 MHz to 3.9 GHz.

The thermally efficient package measures only 2mm x 2mm x 0.75mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85ºC. All devices are 100% RF & DC tested.

Notes:

1. Enhancement mode technology employs a single positive V_{gs}, eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data.
3. Conforms to JEDEC reference outline MO229 for DRP-N.
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

Pin Connections and Package Marking



Bottom View

Top View

Note:

Package marking provides orientation and identification:

"0P" = Device Code

"x" = Date code indicates the month of manufacture.

Features

- Single voltage operation
- High Linearity and P1dB
- Low Noise Figure
- Excellent uniformity in product specifications
- Small package size: 2.0 x 2.0 x 0.75 mm^3
- Point MTTF > 300 years[2]
- MSL-1 and lead-free
- Tape-and-Reel packaging option available

Specifications

- 2 GHz; 4.5V, 280 mA (Typ.)
- 45.5 dBm Output IP3
- 29 dBm Output Power at 1dB gain compression
- 1 dB Noise Figure
- 15 dB Gain
- 14.5 dB LFOM[4]
- 65% PAE
- 23ºC/W thermal resistance

Applications

- Front-end LNA Q2 and Q3, Driver or Pre-driver Amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver Amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 1C)

Refer to Agilent Application Note A004R: Electrostatic Discharge Damage and Control.

ATF-501P8 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain–Source Voltage[2]	V	7
V_{GS}	Gate–Source Voltage[2]	V	-5 to 0.8
V_{GD}	Gate Drain Voltage[2]	V	-5 to 1
I_{DS}	Drain Current[2]	A	1
I_{GS}	Gate Current	mA	12
P_{diss}	Total Power Dissipation[3]	W	3.5
$P_{in\ max.}$	RF Input Power	dBm	30
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{ch_b}	Thermal Resistance[4]	°C/W	23

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperature T_B is 25°C. Derate 43.5 mW/°C for T_B > 69.5°C.
4. Channel-to-board thermal resistance measured using 150°C Liquid Crystal Measurement method.

Product Consistency Distribution Charts at 2 GHz, 4.5V, 200 mA [5,6]

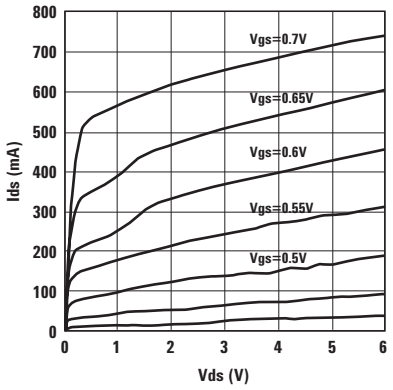


Figure 1. Typical IV curve (Vgs = 0.01V) per step.

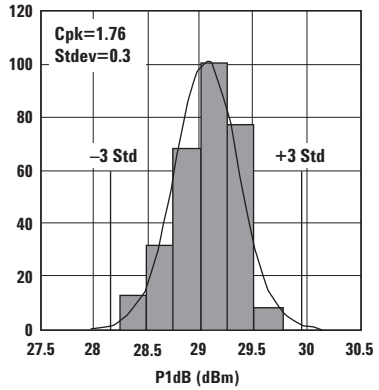


Figure 2. P1dB.

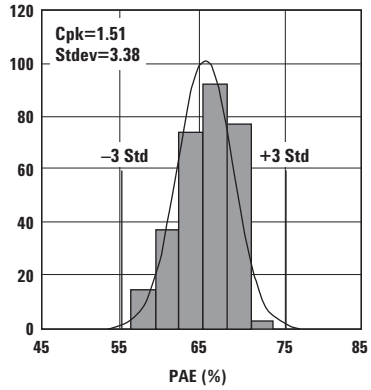


Figure 3. PAE.

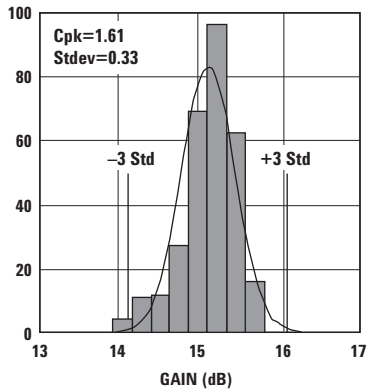


Figure 4. Gain.

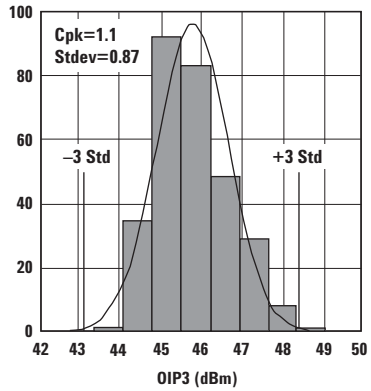


Figure 5. OIP3.

Notes:
5. Distribution data sample size is 300 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-501P8 Electrical Specifications

T_A = 25°C, DC bias for RF parameters is Vds = 4.5V and Ids = 280 mA unless otherwise specified.

Symbol	Parameter and Test Condition		Units	Min.	Typ.	Max.
Vgs	Operational Gate Voltage	Vds = 4.5V, Ids = 280 mA	V	0.42	0.55	0.67
Vth	Threshold Voltage	Vds = 4.5V, Ids = 32 mA	V	—	0.33	—
Idss	Saturated Drain Current	Vds = 4.5V, Vgs = 0V	µA	—	5	—
Gm	Transconductance	Vds = 4.5V, Gm = ΔIds/ΔVgs; ΔVgs = Vgs1 – Vgs2 Vgs1 = 0.55V, Vgs2 = 0.5V	mmho	—	1872	—
Igss	Gate Leakage Current	Vds = 0V, Vgs = -4.5V	µA	-30	-0.8	—
NF	Noise Figure[1]	f = 2 GHz f = 900 MHz	dB dB	— —	1 —	— —
G	Gain[1]	f = 2 GHz f = 900 MHz	dB dB	13.5 —	15 16.6	16.5 —
OIP3	Output 3rd Order Intercept Point[1,2]	f = 2 GHz f = 900 MHz	dBm dBm	43 —	45.5 42	— —
P1dB	Output 1dB Compressed[1]	f = 2 GHz f = 900 MHz	dBm dBm	27.5 —	29 27.3	— —
PAE	Power Added Efficiency[1]	f = 2 GHz f = 900 MHz	% %	50 —	65 49	— —
ACLR	Adjacent Channel Leakage Power Ratio[1,3]	Offset BW = 5 MHz Offset BW = 10 MHz	dBc dBc	— —	63.9 64.1	— —

Notes:

1. Measurements at 2 GHz obtained using production test board described in Figure 2 while measurement at 0.9GHz obtained from load pull tuner.
2. i) 2 GHz OIP3 test condition: F1 = 2.0 GHz, F2 = 2.01 GHz and Pin = -5 dBm per tone.
   ii) 900 MHz OIP3 test condition: F1 = 900 MHz, F2 = 910 MHz and Pin = -5dBm per tone.
3. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)
   - Test Model 1
   - Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)
   - Freq = 2140 MHz
   - Pin = -5 dBm
   - Channel Integrate Bandwidth = 3.84 MHz
4. Use proper bias, board, heatsinking and derating designs to ensure max channel temperature is not exceeded.
   See absolute max ratings and application note for more details.

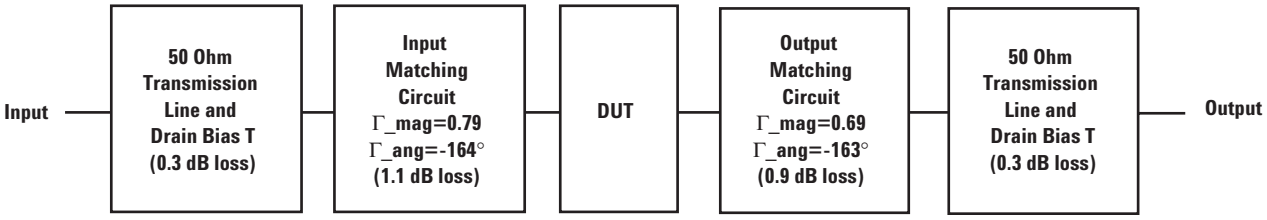


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3 , P1dB and PAE measurements at 2 GHz. This circuit achieves a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

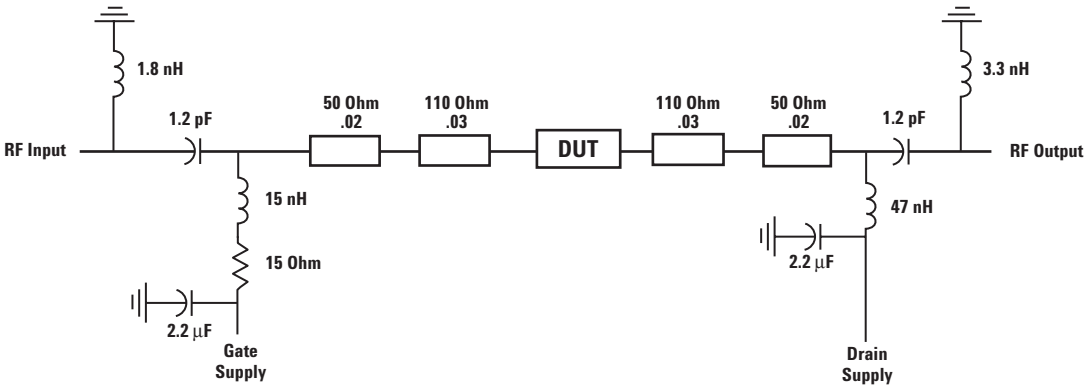


Figure 3. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 and P1dB Tuning Conditions

The device's optimum OIP3 and P1dB measurements were determined using a load pull system at 4.5V 280 mA and 4.5V 400 mA quiesent bias respectively:

Typical Gammas at Optimum OIP3 at 4.5V 280 mA

	Optimized for maximum OIP3 at 4.5V 280 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	46.42	16.03	26.67	45.80	0.305 < -140	0.577 < 162
2.0	45.50	15.07	28.93	50.30	0.806 < -179.2	0.511 < 164
2.4	44.83	12.97	29.03	45.70	0.756 < -167	0.589 < -168
3.9	43.97	6.11	27.33	33.90	0.782 < -162	0.524 < -153

Typical Gammas at Optimum P1dB at 4.5V 280mA

	Optimized for maximum P1dB at 4.5V 280 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	39.29	20.90	30.49	41.00	0.859 < 165	0.757 < 179
2.0	41.79	14.72	30.60	45.30	0.76 < -171	0.691 < -168
2.4	42.37	11.25	30.24	39.70	0.745 < -166	0.694 < -161
3.9	42.00	5.63	28.26	25.80	0.759 < -159	0.708 < -149

Typical Gammas at Optimum OIP3 at 4.5V 400 mA

	Optimized for maximum OIP3 at 4.5V 400 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	49.15	16.85	27.86	44.20	0.5852 < -135.80	0.4785 < 177.00
2.0	48.18	14.72	29.36	48.89	0.7267 < -175.37	0.7338 < 179.56
2.4	47.54	12.47	29.10	46.83	0.6155 < -171.71	0.5411 < -172.02
3.9	45.44	8.05	28.49	37.02	0.7888 < -148.43	0.5247 < -145.84

Typical Gammas at Optimum P1dB at 4.5V 400 mA

	Optimized for maximum P1dB at 4.5V 400 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	41.78	21.84	31.23	49.97	0.7765 < 168.50	0.7589 < -175.09
2.0	43.28	14.83	31.03	44.78	0.8172 < -175.74	0.8011 < -165.75
2.4	42.46	11.90	30.66	41.00	0.8149 < -163.78	0.8042 < -161.79
3.9	42.94	7.70	29.56	33.06	0.8394 < -151.21	0.7826 < -149.00

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3 at 4.5V 280 mA

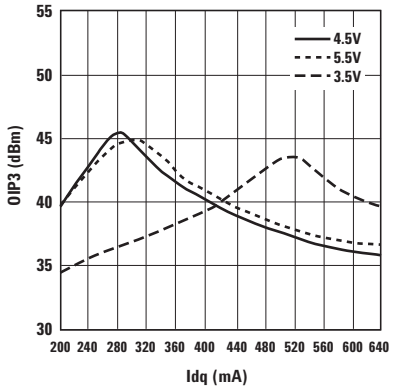


Figure 8. OIP3 vs. Idq and Vds at 2 GHz.

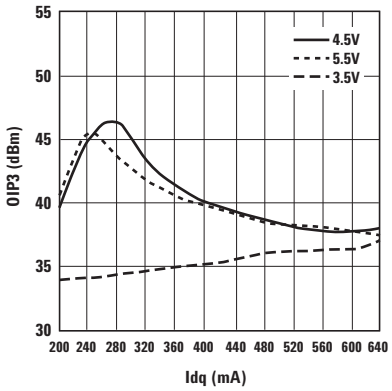


Figure 9. OIP3 vs. Idq and Vds at 0.9 GHz.

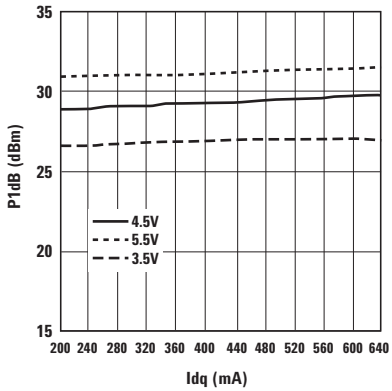


Figure 10. P1dB vs. Idq and Vds at 2 GHz.

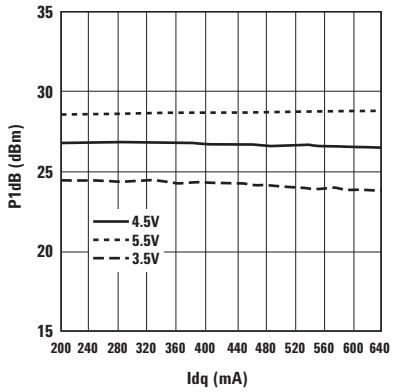


Figure 11. P1dB vs. Idq and Vds at 0.9 GHz.

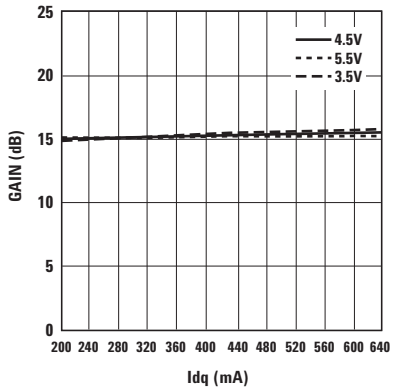


Figure 12. Gain vs. Idq and Vds at 2 GHz.

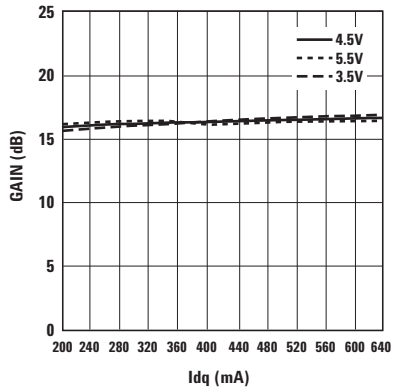


Figure 13. Gain vs. Idq and Vds at 0.9 GHz.

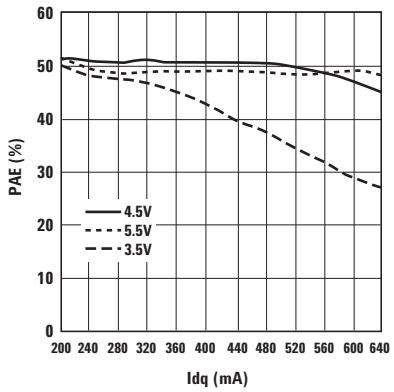


Figure 14. PAE vs. Idq and Vds at 2 GHz.

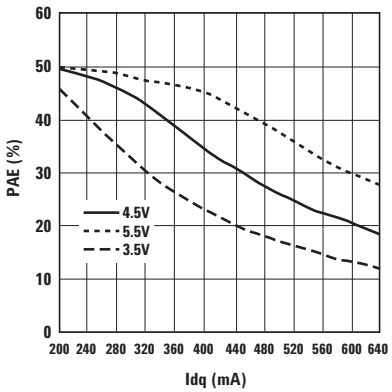


Figure 15. PAE vs. Idq and Vds at 0.9 GHz.

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal P1dB at 4.5V 280 mA

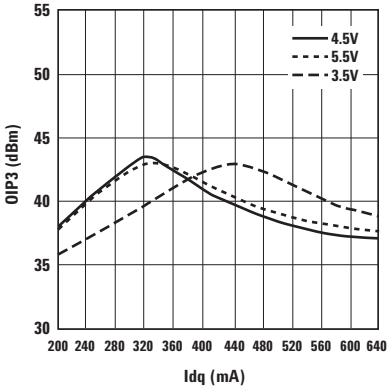


Figure 16. OIP3 vs. Idq and Vds at 2 GHz.

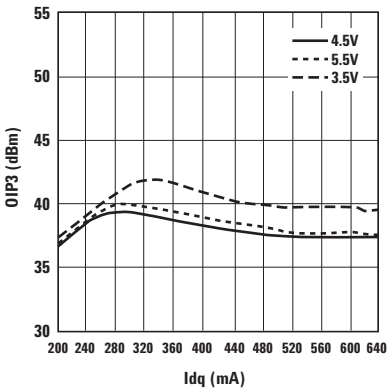


Figure 17. OIP3 vs. Idq and Vds at 0.9 GHz.

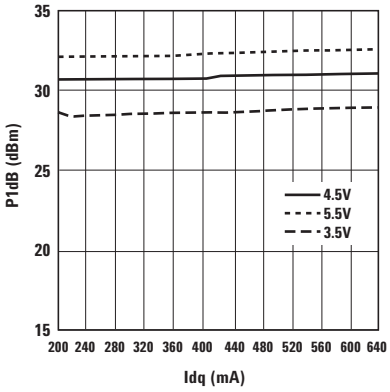


Figure 18. P1dB vs. Idq and Vds at 2 GHz.

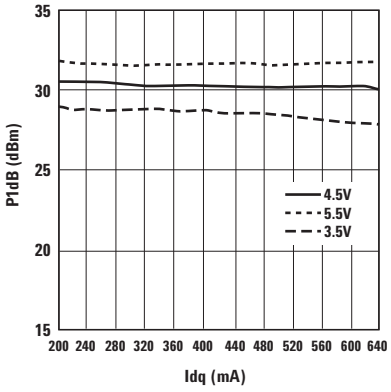


Figure 19. P1dB vs. Idq and Vds at 0.9 GHz.

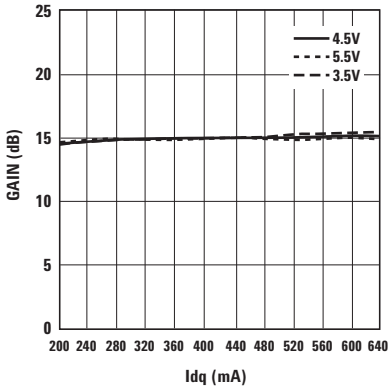


Figure 20. Gain vs. Idq and Vds at 2 GHz.

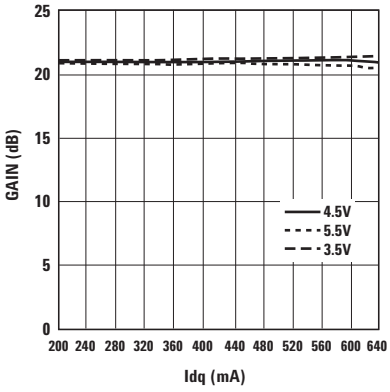


Figure 21. Gain vs. Idq and Vds at 0.9 GHz.

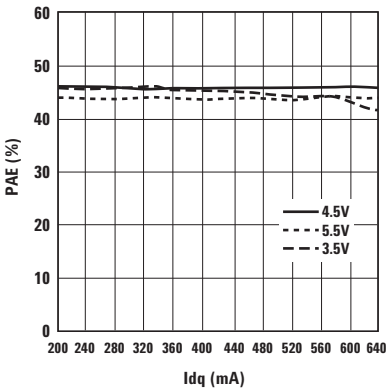


Figure 22. PAE vs. Idq and Vds at 2 GHz.

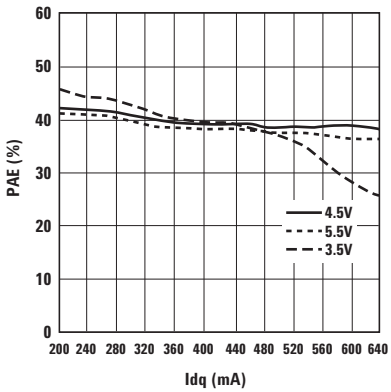


Figure 23. PAE vs. Idq and Vds at 0.9 GHz.