AD824–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = 5.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.1	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		300	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		300		pA
Input Voltage Range			–0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	80		dB
		V_{CM} = 0 V to 3 V	60	74		dB
		T_{MIN} to T_{MAX}	60			dB
Input Impedance				$10^{13}\|\|3.3$		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 4.0 V				
		R_L = 2 kΩ	20	40		V/mV
		R_L = 10 kΩ	50	100		V/mV
		R_L = 100 kΩ	250	1000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	180	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	4.975	4.988		V
		T_{MIN} to T_{MAX}	4.97	4.985		V
		I_{SOURCE} = 2.5 mA	4.80	4.85		V
		T_{MIN} to T_{MAX}	4.75	4.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/Source		±12		mA
		T_{MIN} to T_{MAX}		±10		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 4 V p-p		150		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 4.5 V, to 0.01%		2.5		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo	No Load		50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.8		fA/√Hz
Total Harmonic Distortion	THD	f = 10 kHz, R_L = 0, A_V = +1		0.005		%

ELECTRICAL SPECIFICATIONS (@ V_S = ±15.0 V, V_{OUT} = 0 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.5	2.5	mV
		T_{MIN} to T_{MAX}		0.6	4.0	mV
Input Bias Current	I_B	V_{CM} = 0 V		4	35	pA
		T_{MIN} to T_{MAX}		500	4000	pA
	I_B	V_{CM} = –10 V		25		pA
Input Offset Current	I_{OS}			3	20	pA
		T_{MIN} to T_{MAX}		500		pA
Input Voltage Range			–15		13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15 V to 13 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Input Impedance				$10^{13}\|\|3.3$		Ω||pF
Large Signal Voltage Gain	A_{VO}	Vo = –10 V to +10 V;				
		R_L = 2 kΩ	12	50		V/mV
		R_L = 10 kΩ	50	200		V/mV
		R_L = 100 kΩ	300	2000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	200	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	14.975	14.988		V
		T_{MIN} to T_{MAX}	14.970	14.985		V
		I_{SOURCE} = 2.5 mA	14.80	14.85		V
		T_{MIN} to T_{MAX}	14.75	14.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		–14.985	–14.975	V
		T_{MIN} to T_{MAX}		–14.98	–14.97	V
		I_{SINK} = 2.5 mA		–14.88	–14.85	V
		T_{MIN} to T_{MAX}		–14.86	–14.8	V
Short Circuit Limit	I_{SC}	Sink/Source, T_{MIN} to T_{MAX}	±8	±20		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 15 V	70	80		dB
		T_{MIN} to T_{MAX}	68			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		560	625	µA
		T_{MIN} to T_{MAX}			675	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 20 V p-p		33		kHz
Settling Time	t_S	V_{OUT} = 0 V to 10 V, to 0.01%		6		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L =2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.1		fA/√Hz
Total Harmonic Distortion	THD	f =10 kHz, V_O = 3 V rms,				
		R_L = 10 kΩ		0.005		%

AD824–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = 3.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.2	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		250	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		250		pA
Input Voltage Range			0		1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1 V	58	74		dB
		T_{MIN} to T_{MAX}	56			dB
Input Impedance				$10^{13}\|\|3.3$		Ω‖pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 2.0 V				
		R_L = 2 kΩ	10	20		V/mV
		R_L = 10 kΩ	30	65		V/mV
		R_L = 100 kΩ	180	500		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	90	250		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	2.975	2.988		V
		T_{MIN} to T_{MAX}	2.97	2.985		V
		I_{SOURCE} = 2.5 mA	2.8	2.85		V
		T_{MIN} to T_{MAX}	2.75	2.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/Source		±8		mA
	I_{SC}	Sink/Source, T_{MIN} to T_{MAX}		±6		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V,	70			dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	V_O = 0.2 V, T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 2 V p-p		300		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 2.5 V, to 0.01%		2		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.8		fA/$\sqrt{\text{Hz}}$
Total Harmonic Distortion	THD	f = 10 kHz, R_L = 0, A_V = +1		0.01		%

WAFER TEST LIMITS (@ V_S = 5.0 V, V_{CM} = 0 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Unit
Offset Voltage	V_{OS}		1.0	mV max
Input Bias Current	I_B		12	pA max
Input Offset Current	I_{OS}		20	pA
Input Voltage Range	V_{CM}		–0.2 to 3.0	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	dB min
Power Supply Rejection Ratio	PSRR	V = + 2.7 V to +12 V	70	μV/V
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	15	V/mV min
Output Voltage High	V_{OH}	I_{SOURCE} = 20 μA	4.975	V min
Output Voltage Low	V_{OL}	I_{SINK} = 20 μA	25	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	600	μA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . $–V_S$ – 0.2 V to $+V_S$
Differential Input Voltage . . . . . ±30 V
Output Short Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
R-14, R-16 Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD824A . . . . . –40°C to +85°C
Junction Temperature Range
R-14, R-16 Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
14-Lead SOIC (R)	120	36	°C/W
16-Lead SOIC (R)	92	27	°C/W

NOTES
[1] Absolute maximum ratings apply to packaged parts unless otherwise noted.
[2] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD824AR-14	–40°C to +85°C	14-Pin SOIC	R-14
AD824AR-14-3V	–40°C to +85°C	14-Pin SOIC	R-14
AD824AR-16	–40°C to +85°C	16-Pin SOIC	R-16

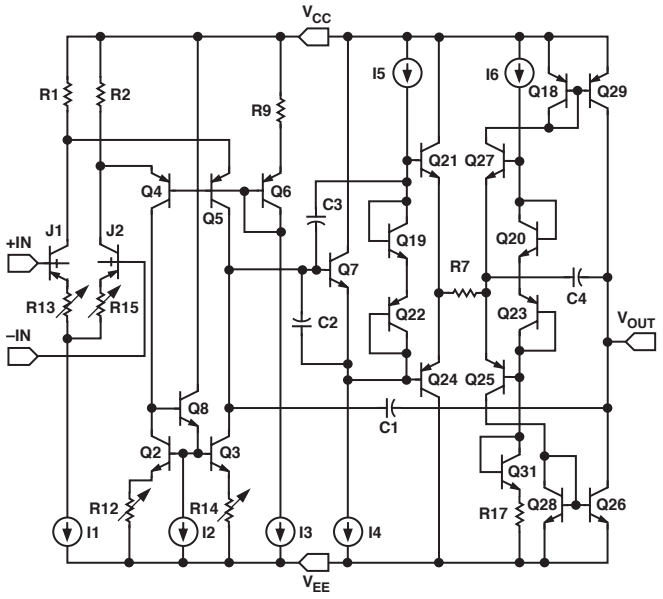
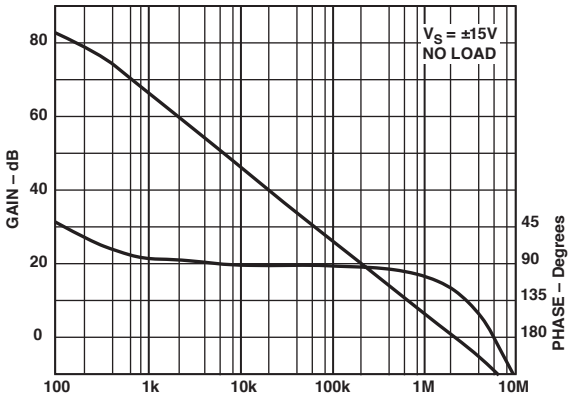


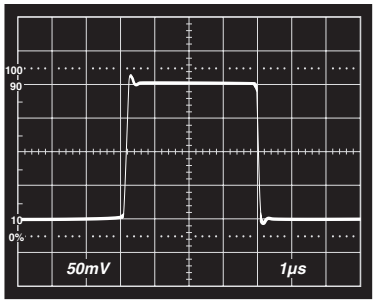
Figure 1. Simplified Schematic of 1/4 AD824

CAUTION

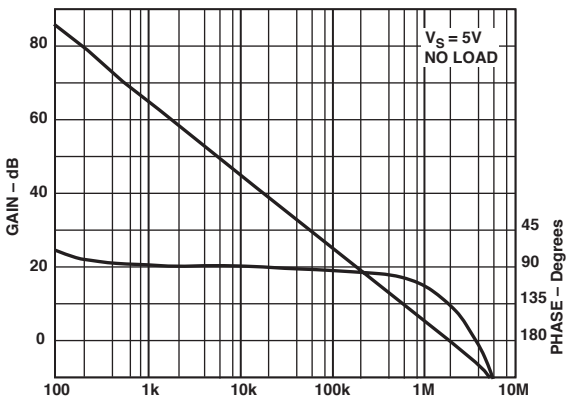
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD824 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

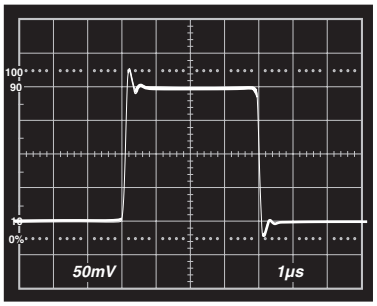
AD824–Typical Performance Characteristics



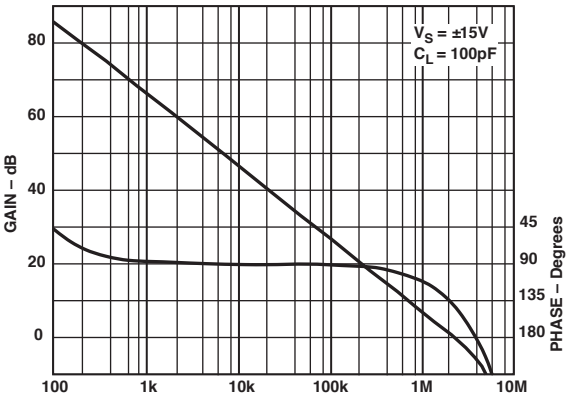


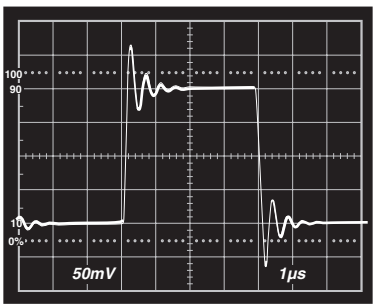
TPC 1. Open-Loop Gain/Phase and Small Signal Response, V_S = ±15 V, No Load



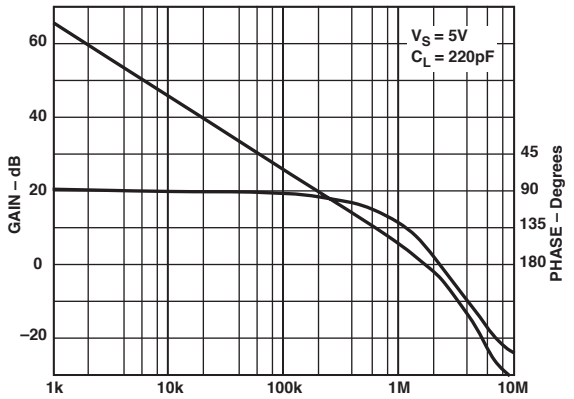


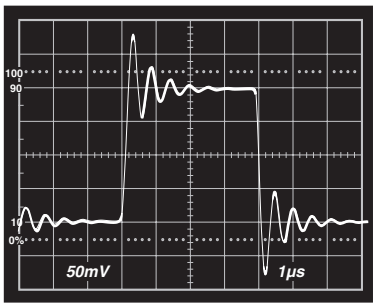
TPC 3. Open-Loop Gain/Phase and Small Signal Response, V_S = 5 V, No Load



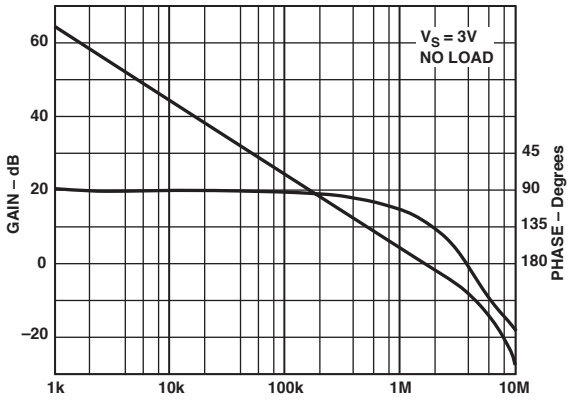


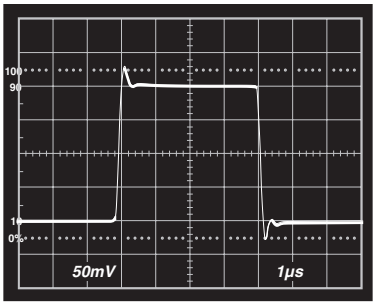
TPC 2. Open-Loop Gain/Phase and Small Signal Response, V_S = ±15 V, C_L = 100 pF



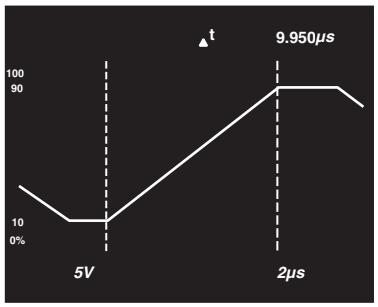


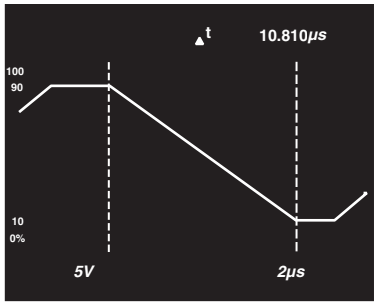
TPC 4. Open-Loop Gain/Phase and Small Signal Response, V_S = 5 V, C_L = 220 pF



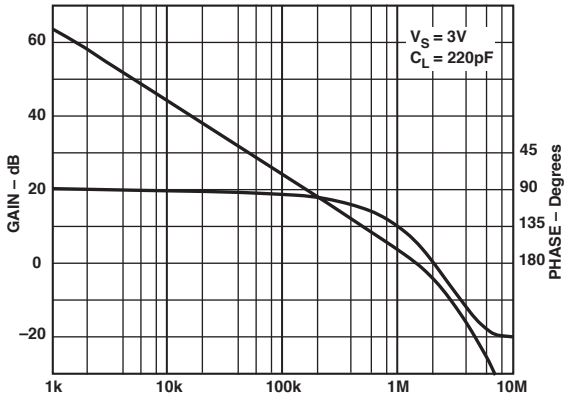


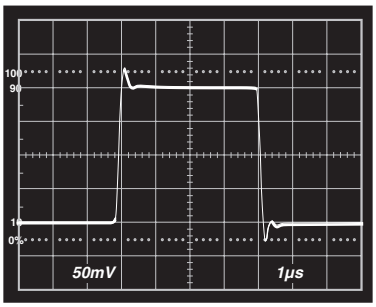
TPC 5. Open-Loop Gain/Phase and Small Signal Response, V_S = 3 V, No Load



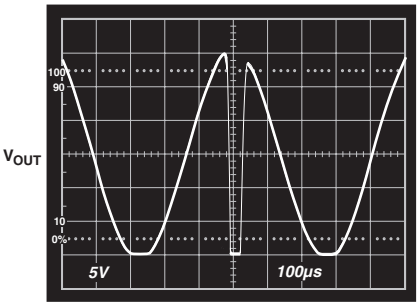


TPC 7. Slew Rate, R_L = 10k

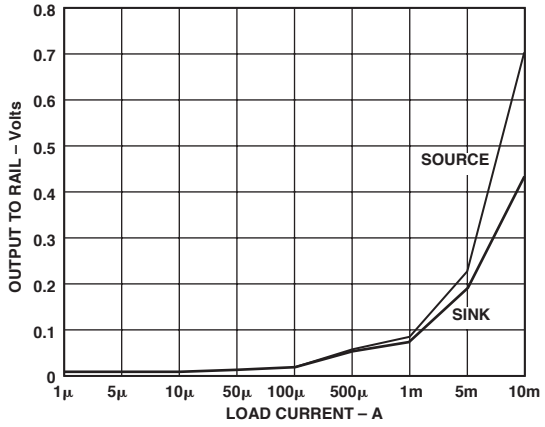




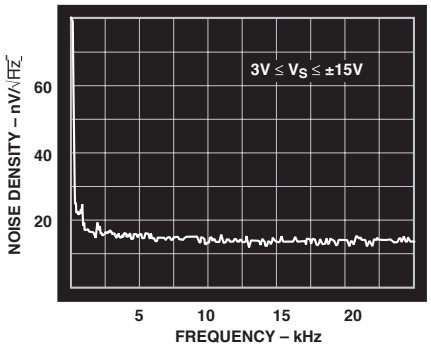
TPC 6. Open-Loop Gain/Phase and Small Signal Response, V_S = 3 V, C_L = 220 pF



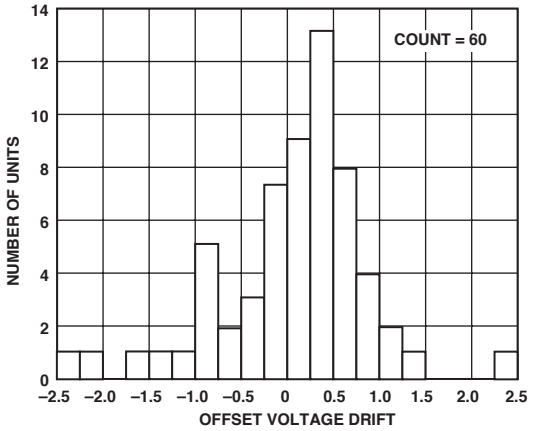
TPC 8. Phase Reversal with Inputs Exceeding Supply by 1 V



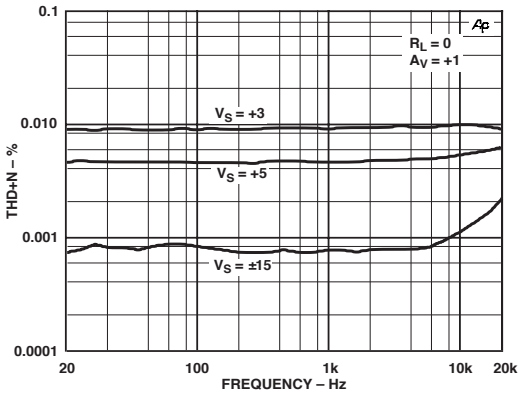
TPC 9. Output Voltage to Supply Rail vs. Sink and Source Load Currents



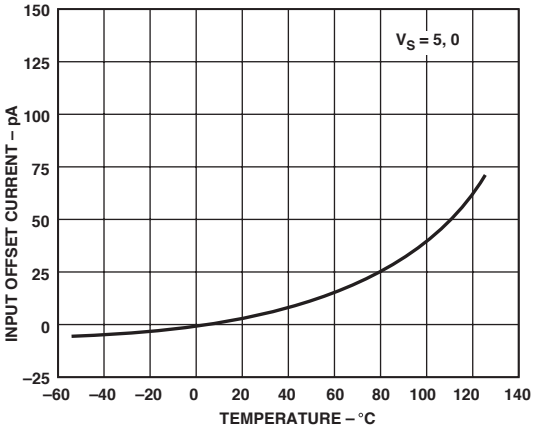
TPC 10. Voltage Noise Density



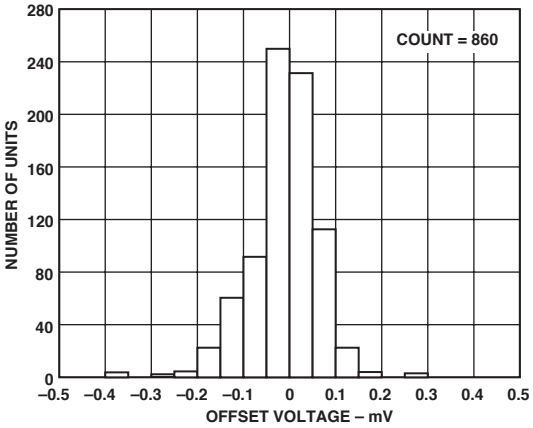
TPC 13. TC V_{OS} Distribution, –55°C to +125°C, V_S = 5, 0



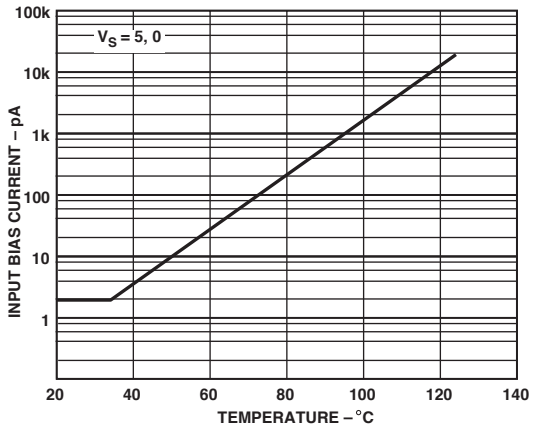
TPC 11. Total Harmonic Distortion



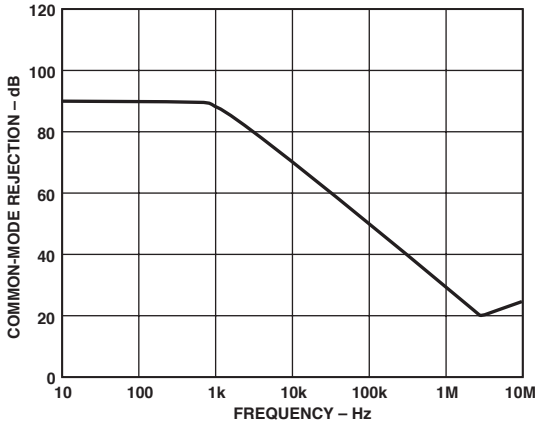
TPC 14. Input Offset Current vs. Temperature



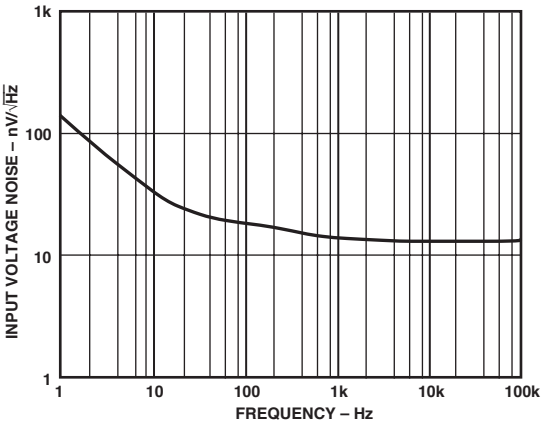
TPC 12. Input Offset Distribution, V_S = 5, 0



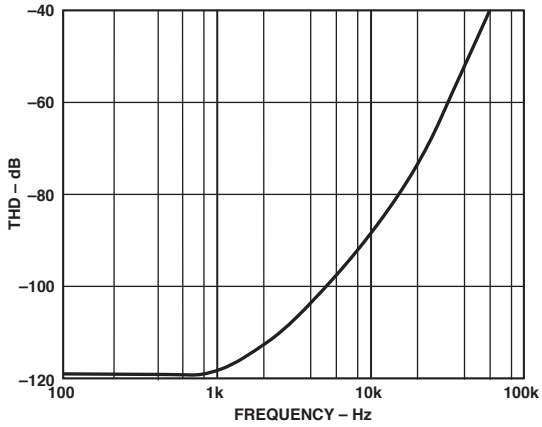
TPC 15. Input Bias Current vs. Temperature



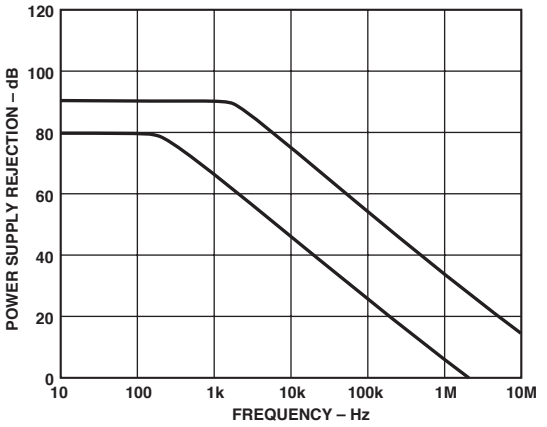
TPC 16. Common-Mode Rejection vs. Frequency



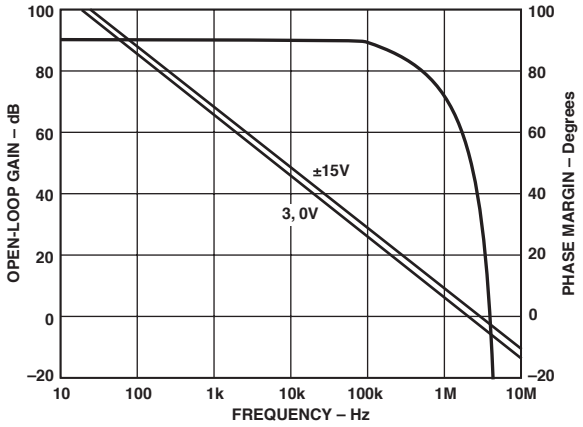
TPC 19. Input Voltage Noise Spectral Density vs. Frequency



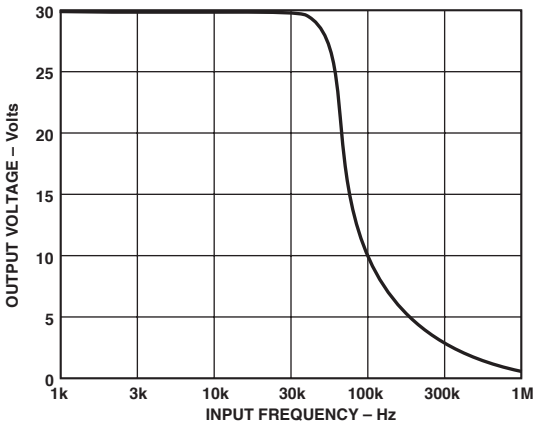
TPC 17. THD vs. Frequency, 3 V rms



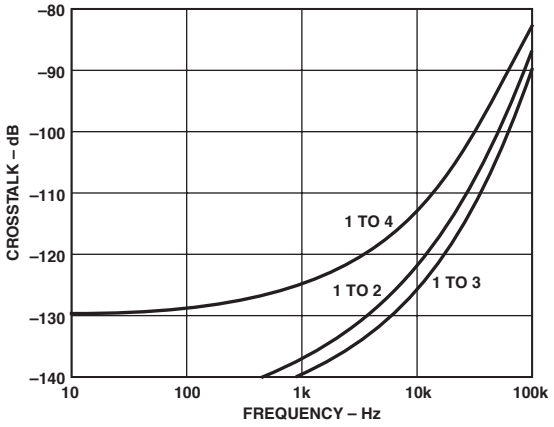
TPC 20. Power Supply Rejection vs. Frequency



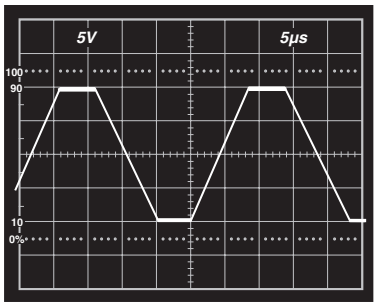
TPC 18. Open-Loop Gain and Phase vs. Frequency



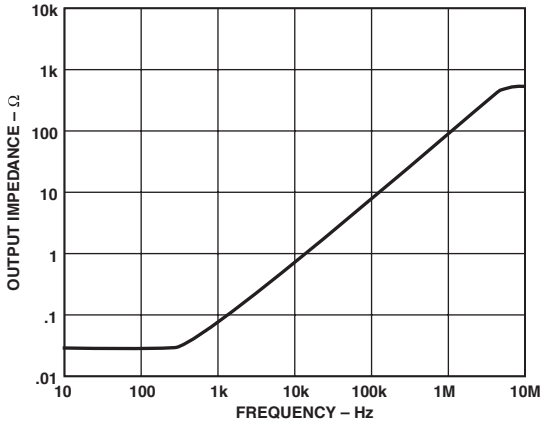
TPC 21. Large Signal Frequency Response



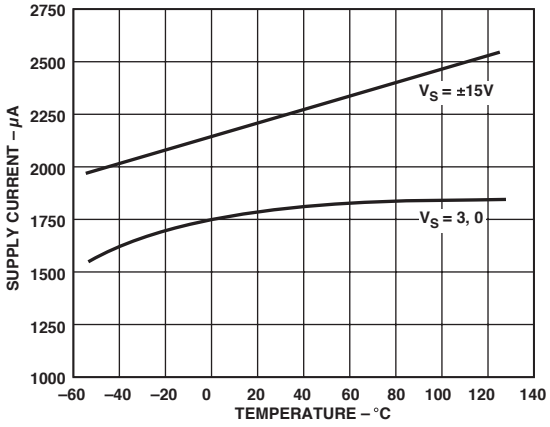
TPC 22. Crosstalk vs. Frequency



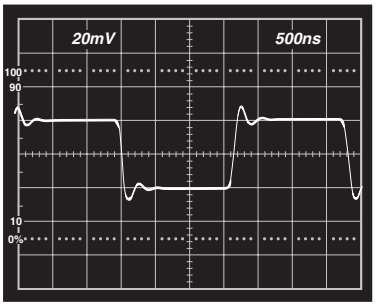
TPC 25. Large Signal Response



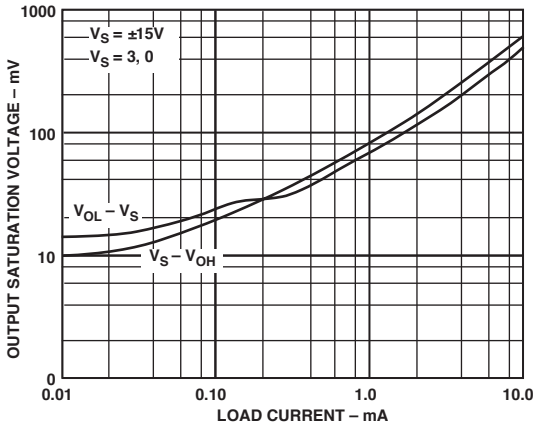
TPC 23. Output Impedance vs. Frequency, Gain = +1



TPC 26. Supply Current vs. Temperature



TPC 24. Small Signal Response, Unity Gain Follower, 10k‖100 pF Load



TPC 27. Output Saturation Voltage

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD824, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth.

The AD824 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 2a shows the response of an AD824 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD824's noninverting input will prevent phase reversal at the expense of greater input voltage noise. This is illustrated in Figure 2b.

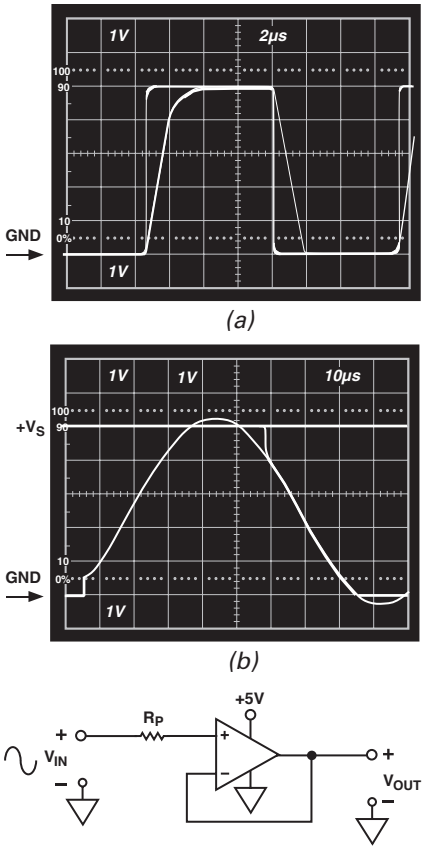


Figure 2. (a) Response with R_P = 0; V_{IN} from 0 to $+V_S$
(b) V_{IN} = 0 to + V_S + 200 m V
V_{OUT} = 0 to + V_S
R_P = 49.9 kΩ

Since the input stage uses n-channel JFETs, input current during normal operation is positive; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S$ – 0.4 V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in TPC 8.

A current-limiting resistor should be used in series with the input of the AD824 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV or if an input voltage will be applied to the AD824 when $\pm V_S$ = 0. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

OUTPUT CHARACTERISTICS

The AD824's unique bipolar rail-to-rail output stage swings within 15 mV of the positive and negative supply voltages. The AD824's approximate output saturation resistance is 100 Ω for both sourcing and sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, the saturation voltage will be 0.5 V from either supply with a 5 mA current load.

For load resistances over 20 kΩ, the AD824's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD824's output is overdriven so as to saturate either of the output devices, the amplifier will recover within 2 µs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. TPC 4 and 6 show the AD824's pulse response as a unity gain follower driving 220 pF. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

Figure 3 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

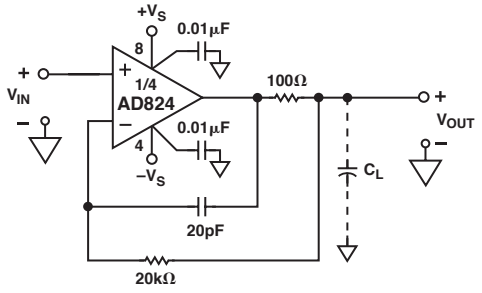


Figure 3. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

A design consideration in sample-and-hold circuits is voltage droop at the output caused by op amp bias and switch leakage currents. By choosing a JFET op amp and a low leakage CMOS switch, this design minimizes droop rate error to better than 0.1 μV/μs in this circuit. Higher values of C_H will yield a lower droop rate. For best performance, C_H and C2 should be polystyrene, polypropylene or Teflon capacitors. These types of capacitors exhibit low leakage and low dielectric absorption. Additionally, 1% metal film resistors were used throughout the design.

In the sample mode, SW1 and SW4 are closed, and the output is $V_{OUT} = -V_{IN}$. The purpose of SW4, which operates in parallel with SW1, is to reduce the pedestal, or hold step, error by injecting the same amount of charge into the noninverting input of A3 that SW1 injects into the inverting input of A3. This creates a common-mode voltage across the inputs of A3 and is then rejected by the CMR of A3; otherwise, the charge injection from SW1 would create a differential voltage step error that would appear at V_{OUT}. The pedestal error for this circuit is less than 2 mV over the entire 0 V to 3.3 V/5 V signal range. Another method of reducing pedestal error is to reduce the pulse amplitude applied to the control pins. In order to control the ADG513, only 2.4 V are required for the "ON" state and 0.8 V for the "OFF" state. If possible, use an input control signal whose amplitude ranges from 0.8 V to 2.4 V instead of a full range 0 V to 3.3 V/5 V for minimum pedestal error.

Other circuit features include an acquisition time of less than 3 μs to 1%; reducing C_H and C2 will speed up the acquisition time further, but an increased pedestal error will result. Settling time is less than 300 ns to 1%, and the sample-mode signal BW is 80 kHz.

The ADG513 was chosen for its ability to work with 3 V/5 V supplies and for having normallyopen and normallyclosed precision CMOS switches on a dielectrically isolated process. SW2 is not required in this circuit; however, it was used in parallel with SW3 to provide a lower R_{ON} analog switch.