



# STS25N3LLH6

N-channel 30 V, 0.0025  $\Omega$ , 22 A, SO-8  
STripFET™ VI DeepGATE™ Power MOSFET

Preliminary Data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS25N3LLH6	30 V	0.0032 $\Omega$	22 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

## Application

- Switching applications

## Description

This product utilizes the 6<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in a standard package, that makes it suitable for the most demanding DC-DC converter applications, where high power density has to be achieved.

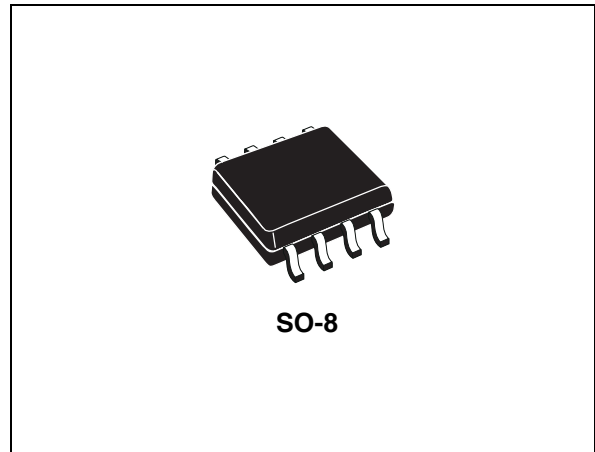


Figure 1. Internal schematic diagram

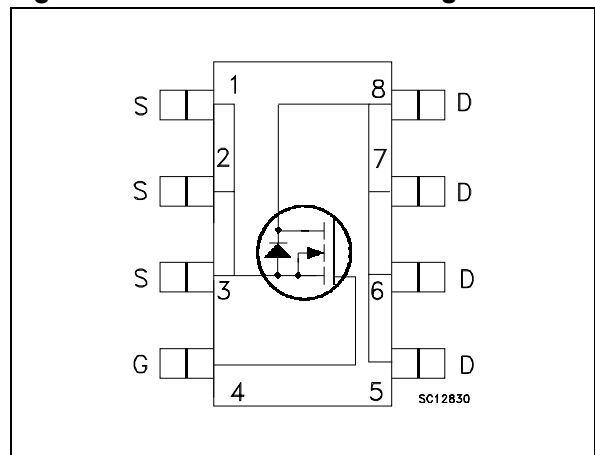


Table 1. Device summary

Order code	Marking	Packag	Packaging
STS25N3LLH6	25G3L	SO-8	Tape and reel

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}^{(1)}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	13.7	A
$I_{DM}^{(2)}$	Drain current (pulsed)	88	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.7	W
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Continuous mode
2. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	47	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current	TBD	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ )	TBD	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 15\text{ A}$		0.0025 0.0042	0.0032 TBD	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		2100		pF
$C_{oss}$	Output capacitance			400		pF
$C_{rss}$	Reverse transfer capacitance			170		pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 22\text{ A}$ $V_{GS} = 4.5\text{ V}$ <i>Figure 8</i>		16	TBD	nC
$Q_{gs}$	Gate-source charge			TBD		nC
$Q_{gd}$	Gate-drain charge			TBD		nC
$R_G$	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain		TBD		$\Omega$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=11\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=4.5\text{ V}$ <i>Figure 2</i>		TBD		ns
$t_r$	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
$t_f$	Fall time			TBD		ns

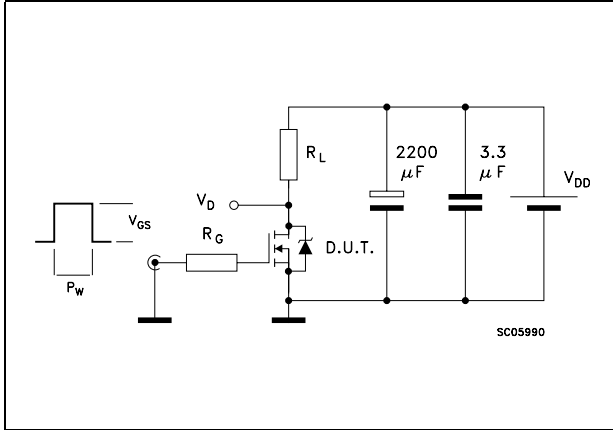
**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				88	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=22\text{ A}$ , $V_{GS}=0$			1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=22\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>Figure 4</i>		TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		nC
$I_{RRM}$	Reverse recovery current			TBD		A

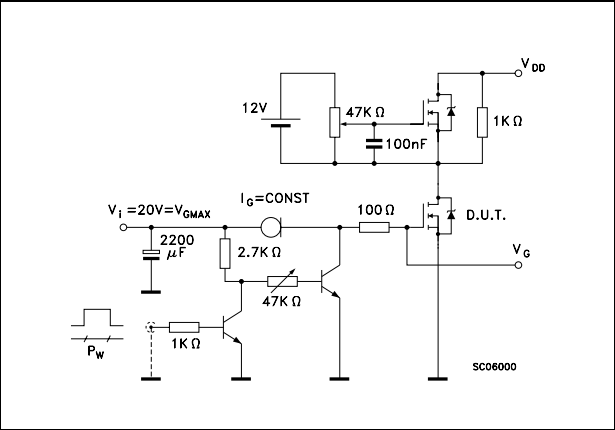
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuit

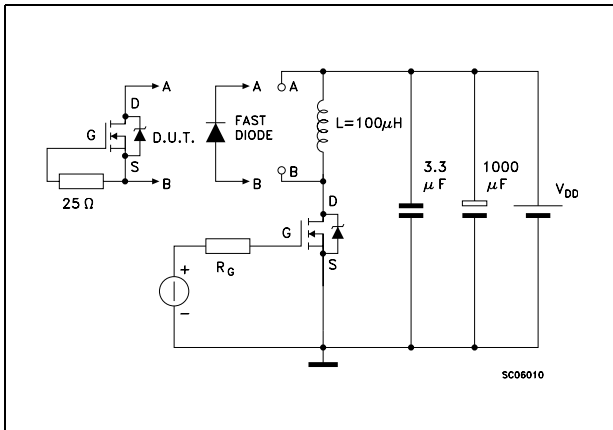
**Figure 2. Switching times test circuit for resistive load**



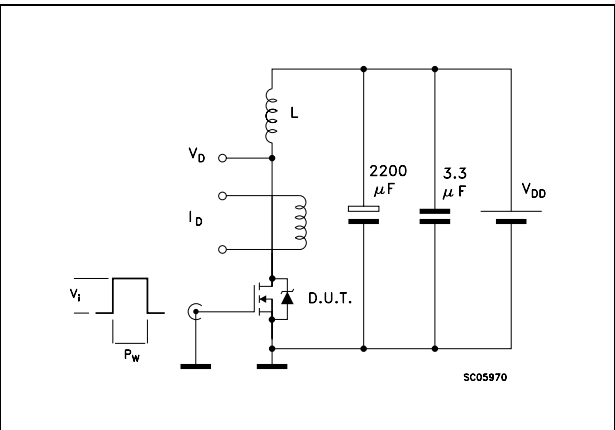
**Figure 3. Gate charge test circuit**



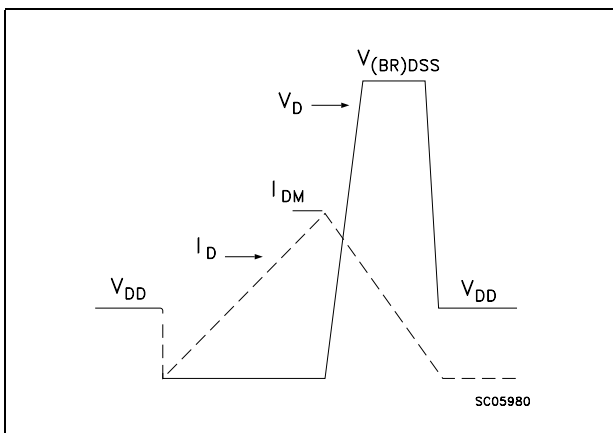
**Figure 4. Test circuit for inductive load switching and diode recovery times**



**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**

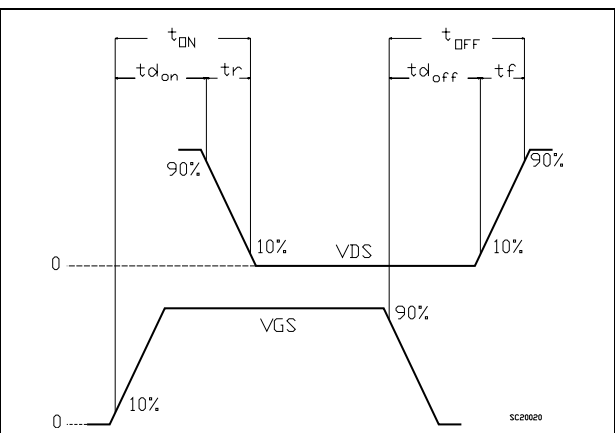
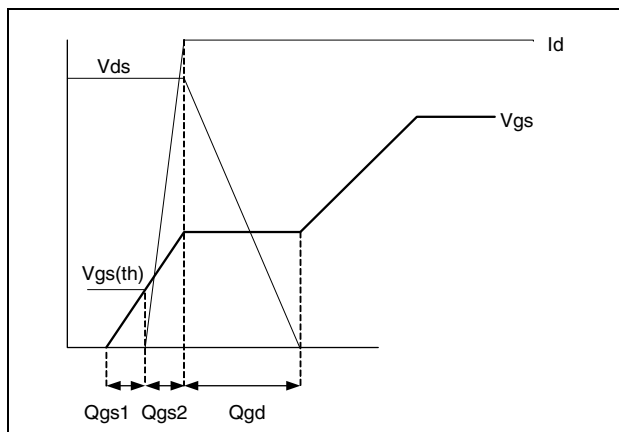


Figure 8. Gate charge waveform



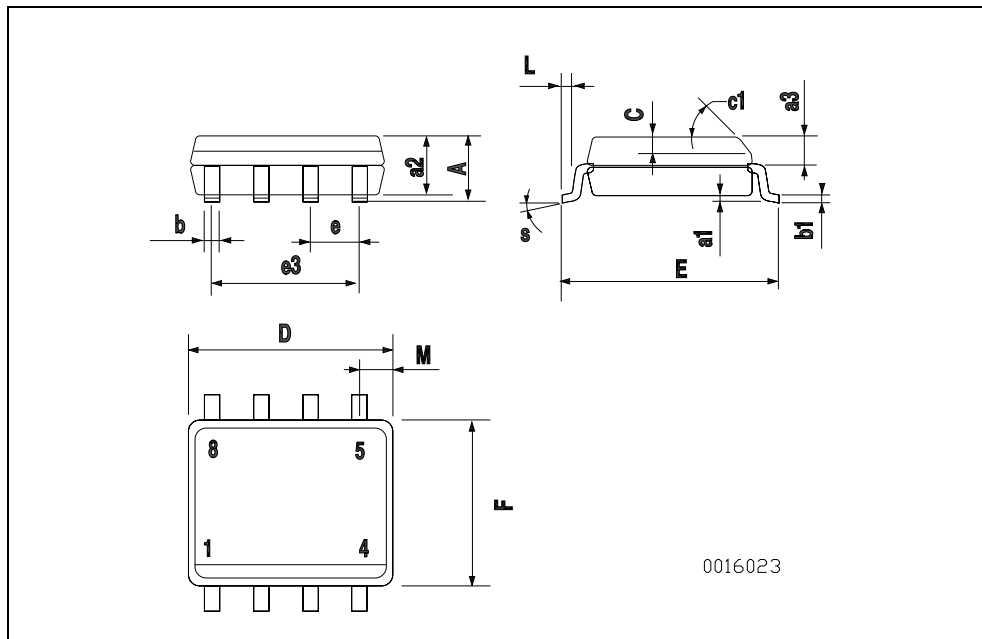
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
27-Jan-2009	1	First release

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