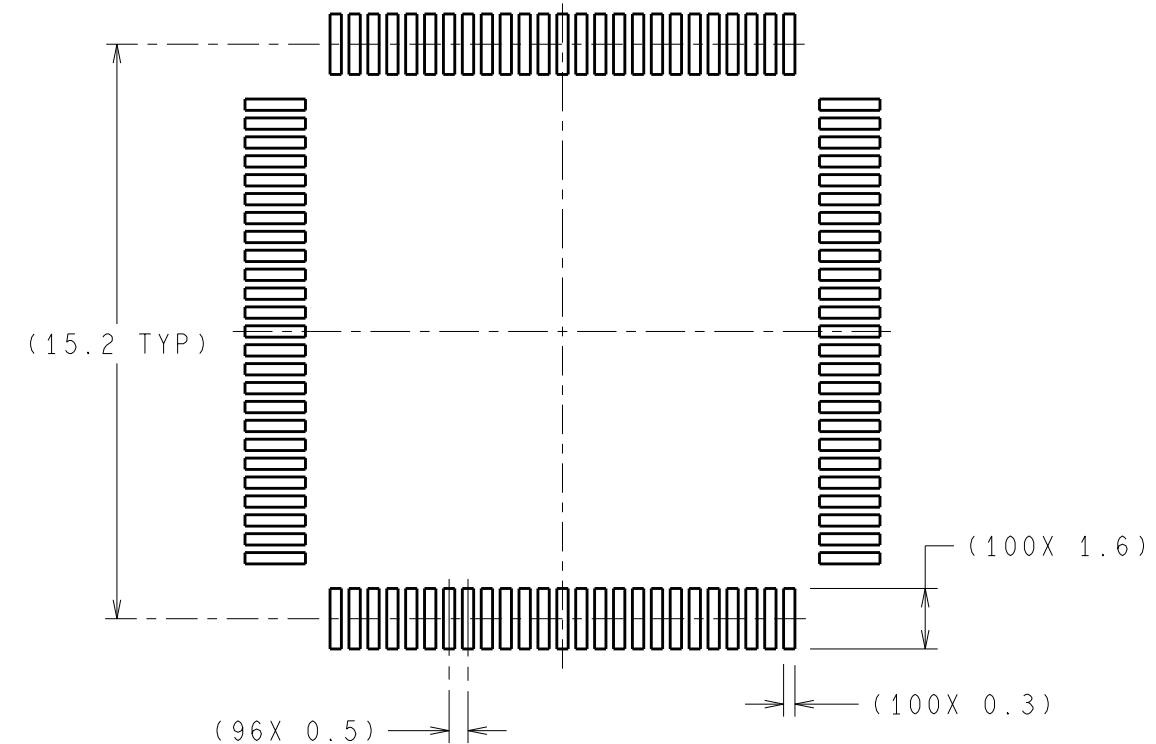
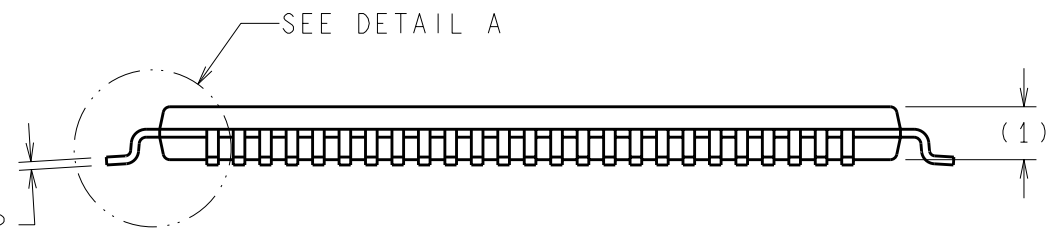
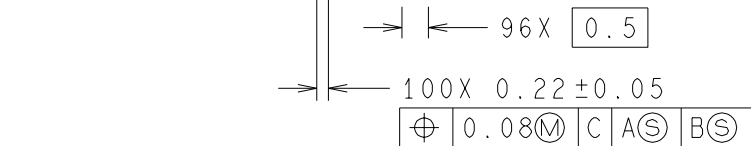
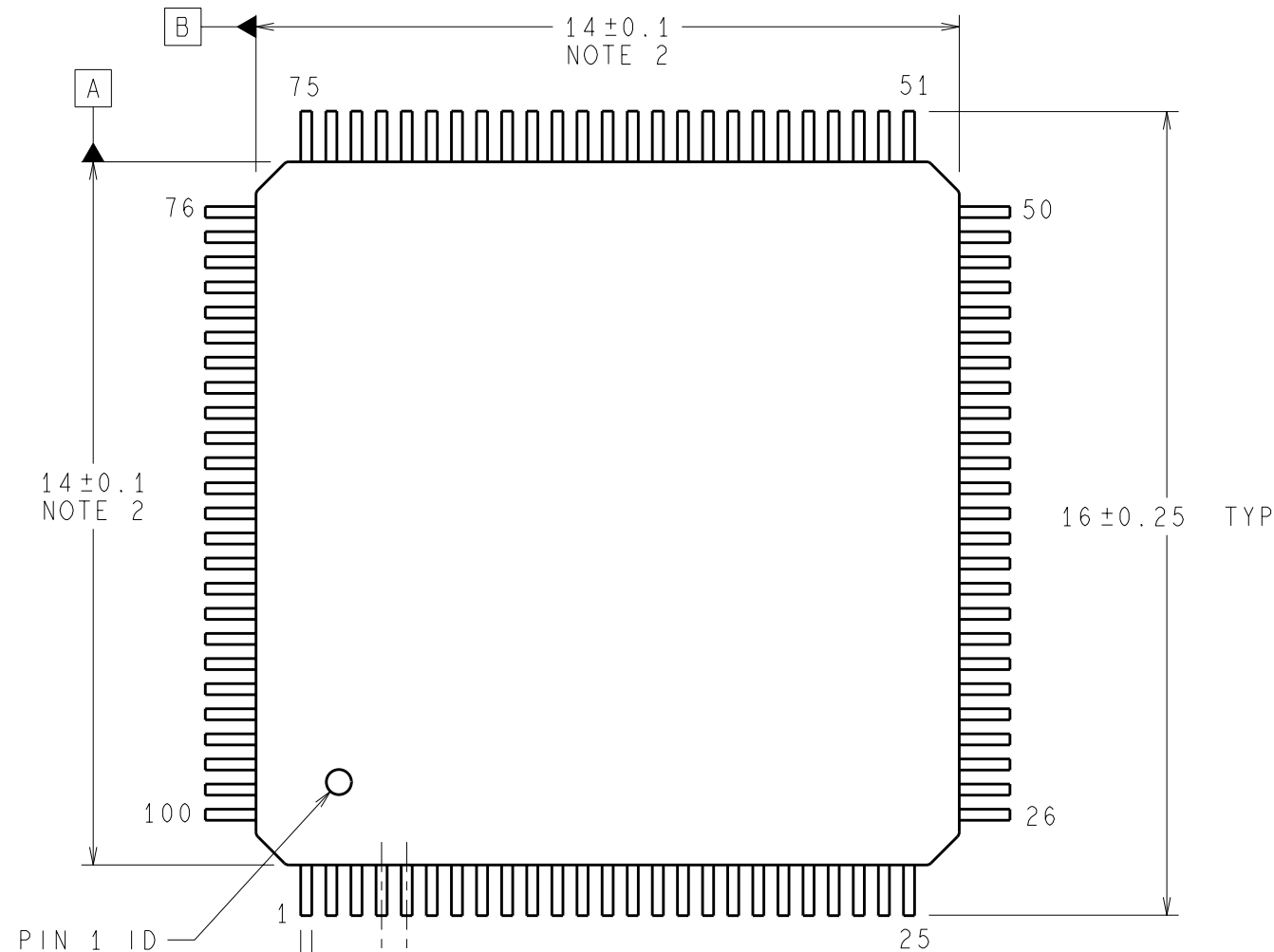
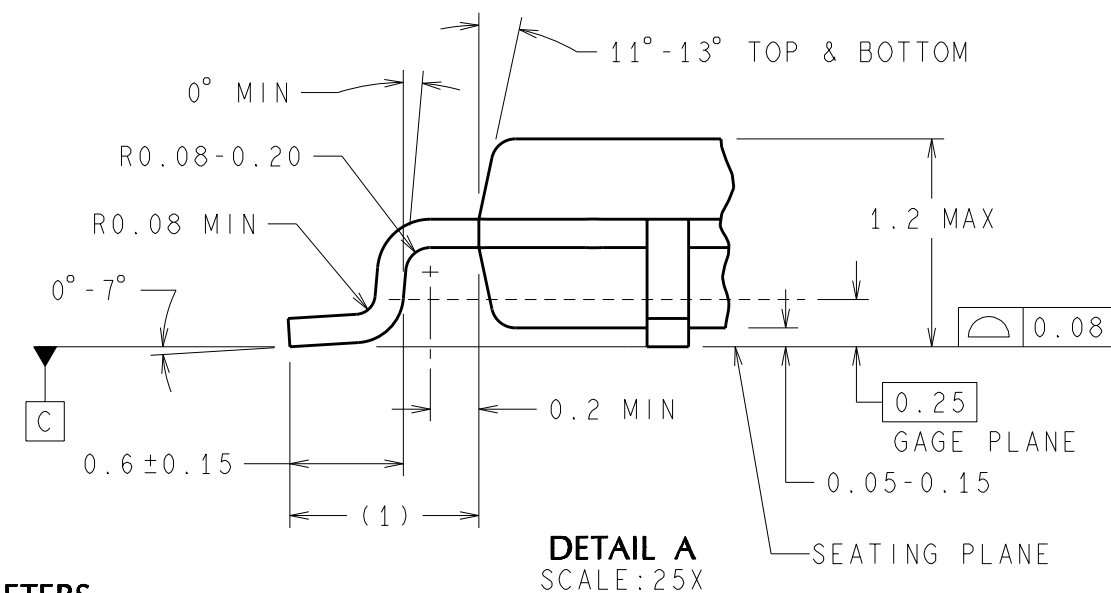


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	10712	11/22/1994	DEG/HJK
B	TITLE: TOFP WAS POPF; UPDATE NOTE 3; ADD GEOMETRIC TOLERANCE	12317	12/02/1999	ACS/MS/RW
C	REV NOTE 1; ADD LAND PATTERN; CHG DWG FORMAT TO B SIZE; BODY THICKNESS: (1) WAS 1+/-0.05	1263	05/11/2004	TL/RW



RECOMMENDED LAND PATTERN



DETAIL A
SCALE: 25X

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
- REFERENCE JEDEC REGISTRATION MS-026, VARIATION AED.

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRWN	DE Grady	11/22/1994		
DFTG. CHK.	MARTA SUCHY	05/11/2004	TOFP, JEDEC METRIC, 14 X 14 X 1.0mm, 100 LEAD	
ENGR. CHK.	RANDALL WALBERG	05/11/2004		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-VJD100A	C
FORMERLY: N/A			SHEET 1 of 1	