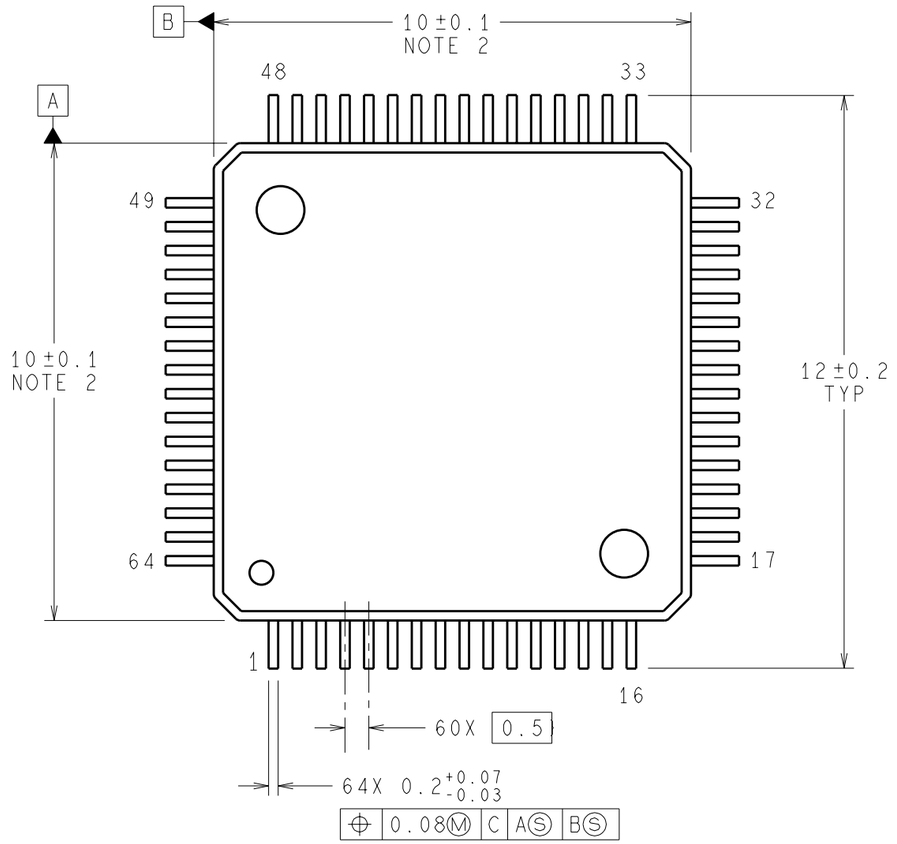
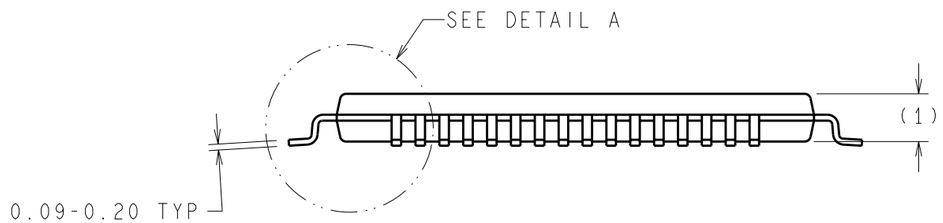
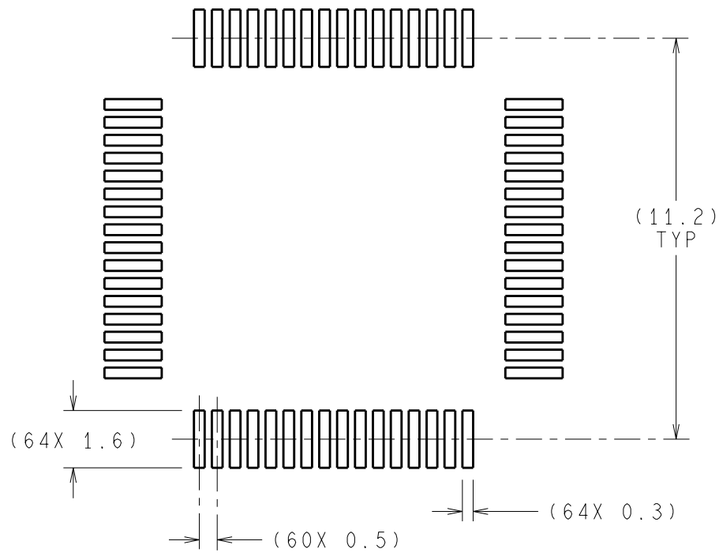
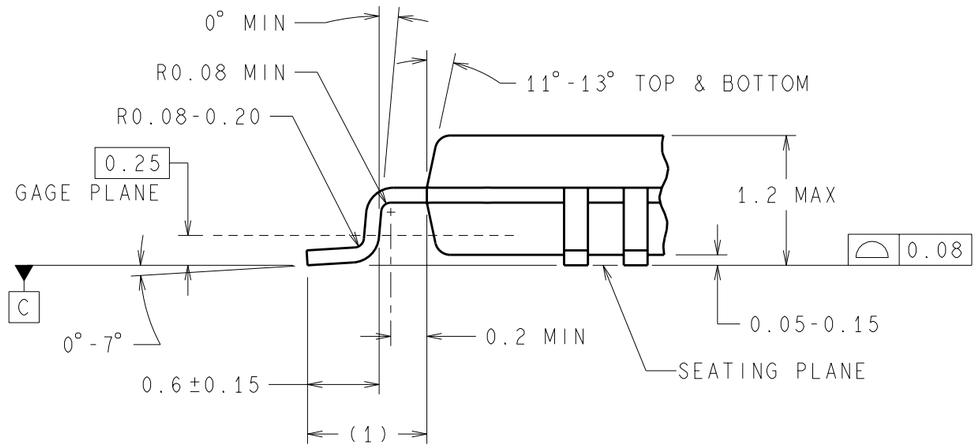
| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| A | RELEASE TO DOCUMENT CONTROL | 12379 | 05/01/2000 | MS/RW |
| B | UPDATE DWG & TITLE PER CURRENT STD; REVISE NOTE 1 & UPDATE NOTE 3; CHANGE DWG FORMAT TO B SIZE. | 1025 | 07/15/2003 | MS/RW |




**LAND PATTERN RECOMMENDATION**




**DETAIL A**
TYPICAL

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com)
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
3. REFERENCE JEDEC REGISTRATION MS-026, VARIATION ACD.

**DIMENSIONS ARE IN MILLIMETERS**
DIMENSIONS IN ( ) FOR REFERENCE ONLY

| APPROVALS | DATE |
|---|---|
| DRAWN MARTA SUCHY | 05/01/2000 |
| DFTG. CHK. THANH LEQUANG | 07/15/2003 |
| ENGR. CHK. RANDALL WALBERG | 07/15/2003 |

National Semiconductor
2900 Semiconductor Dr, Santa Clara, CA 95052-8090

TQFP, JEDEC METRIC, 10x10x1.0mm, 64 LD, 0.5mm PITCH

PROJECTION MM

| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| NTS | B | (SC)MKT-VEC64A | B |

FORMERLY: N/A SHEET 1 of 1