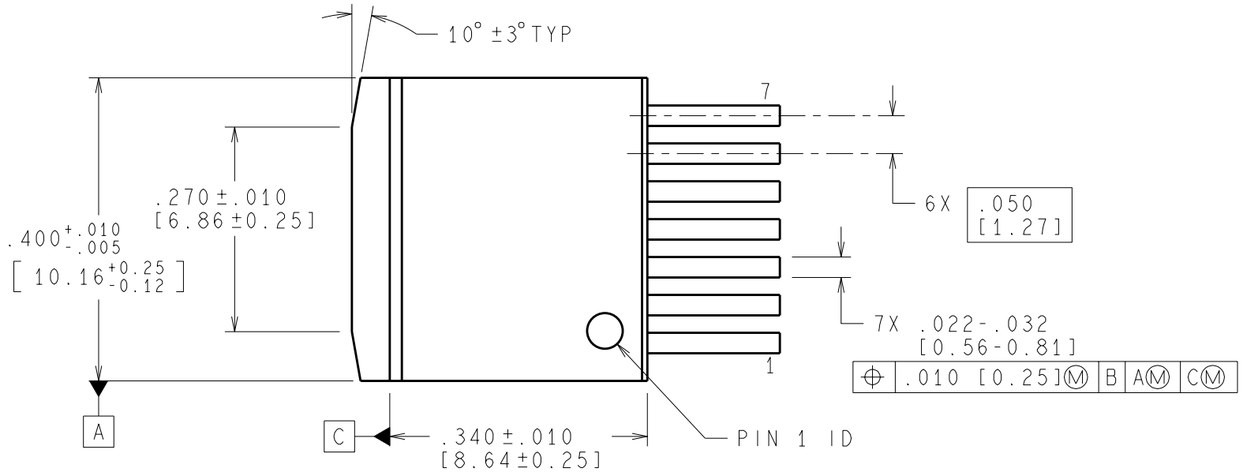
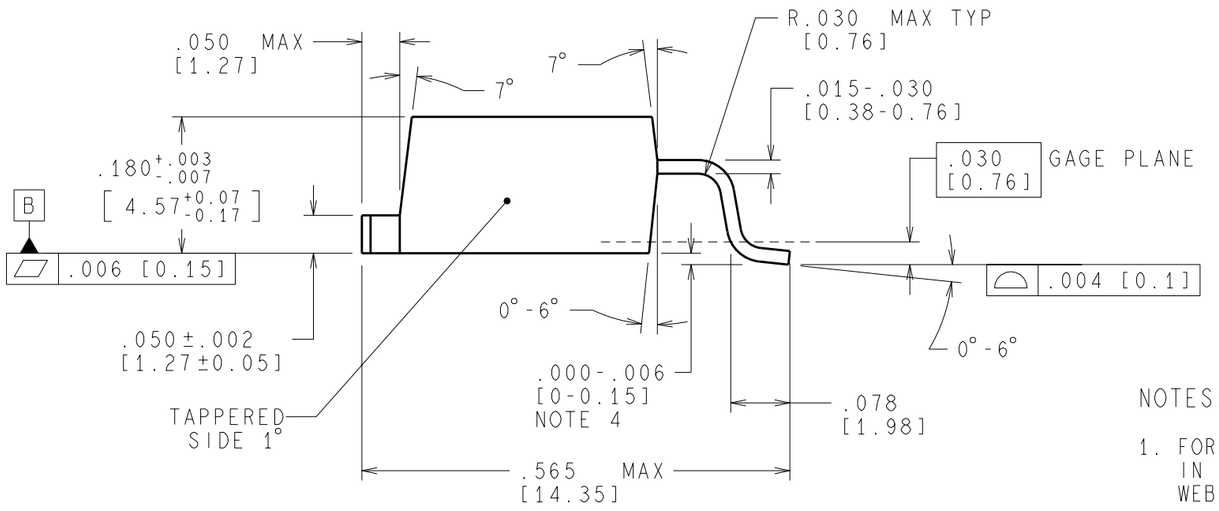
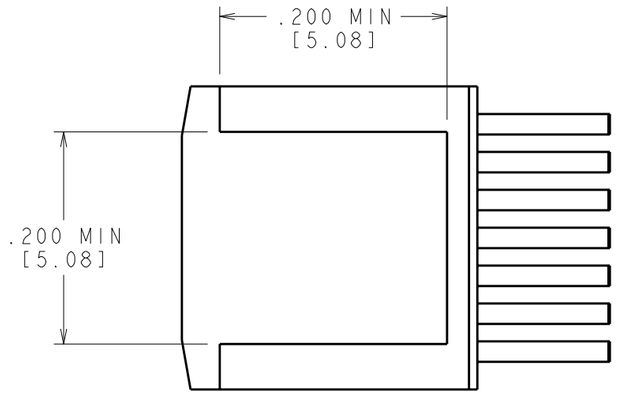
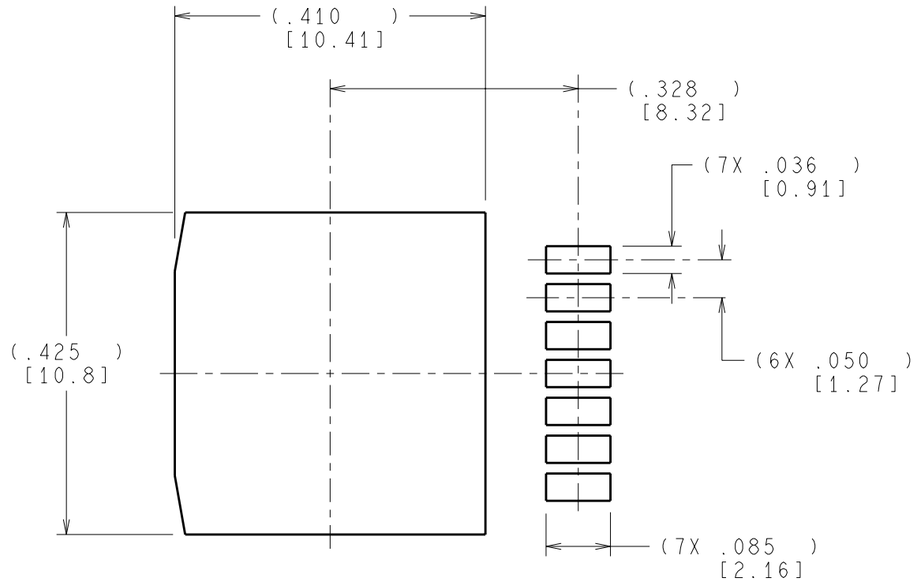
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
D	REVISE & REDRAW PER CURRENT STD.	12181	06/02/1999	TL/CD
E	UPDATE DWG & TITLE PER CURRENT STD; REVISE NOTE 1 & UPDATE NOTE 5; CHANGE DWG FORMAT TO B SIZE.	1025	07/15/2003	MS/RW









LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM VERTICAL BURR ON HEATSINK NOT TO EXCEED .003 IN/ 0.08 mm.
3. NO PACKAGE CHIPS, CRACKS OR SURFACE INDENTATION ALLOWED AFTER FORMING.
4. UNDER ALL CONDITIONS, LEADS MUST NOT BE ABOVE DATUM -B-.
5. REFERENCE JEDEC REGISTRATION MO-169, VARIATION AC.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

APPROVALS	DATE
DRAWN T. LEQUANG	06/02/1999
DFTG. CHK. THANH LEQUANG	07/15/2003
ENGR. CHK. RANDALL WALBERG	07/15/2003

PROJECTION INCH (MM)

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

TO-263, MOLDED, .400x.390x.180in BODY, 7 LD, .050in PITCH, SURF.MOUNT

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-TS7B	E

FORMERLY: N/A

SHEET 1 of 1