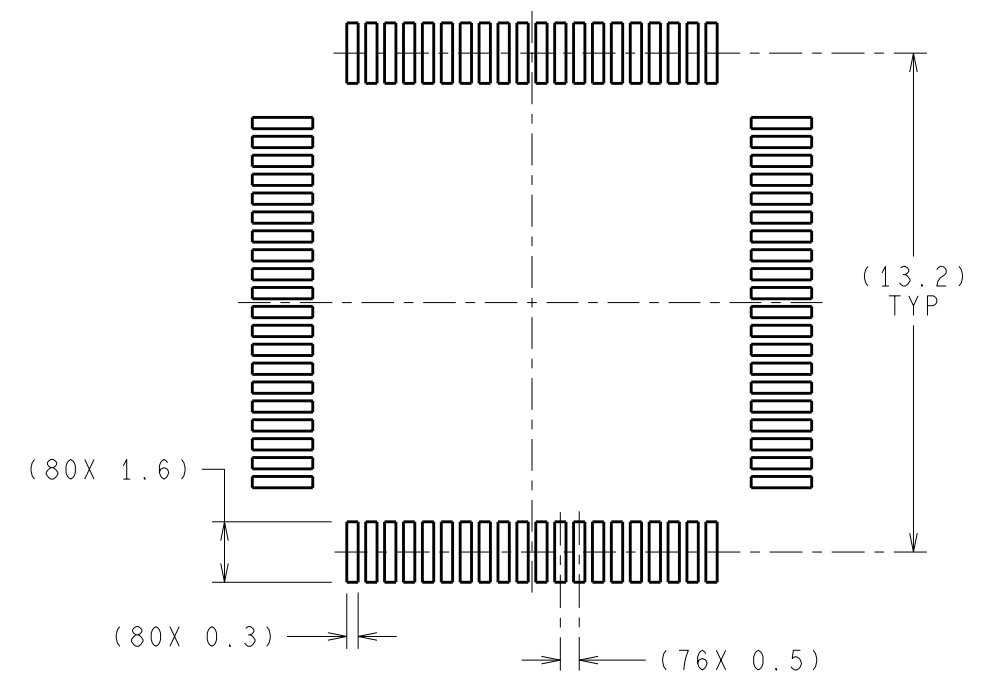
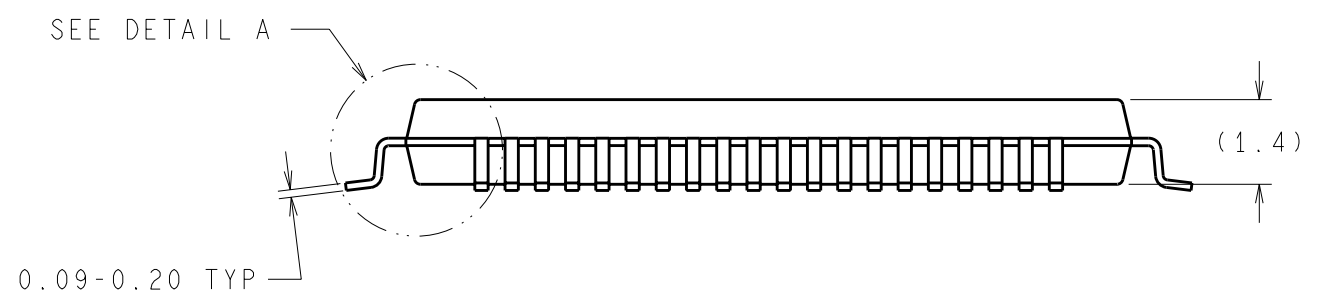
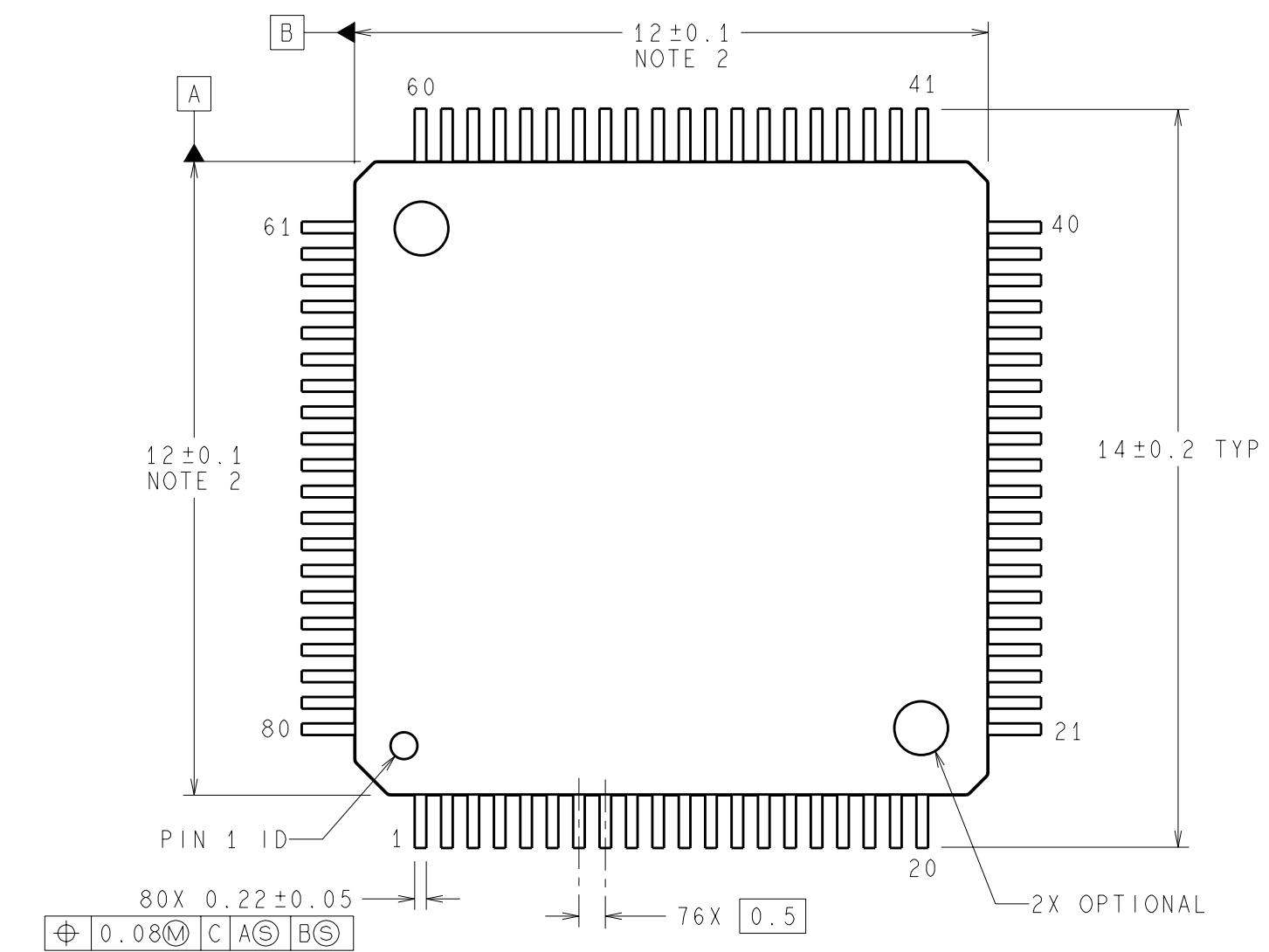
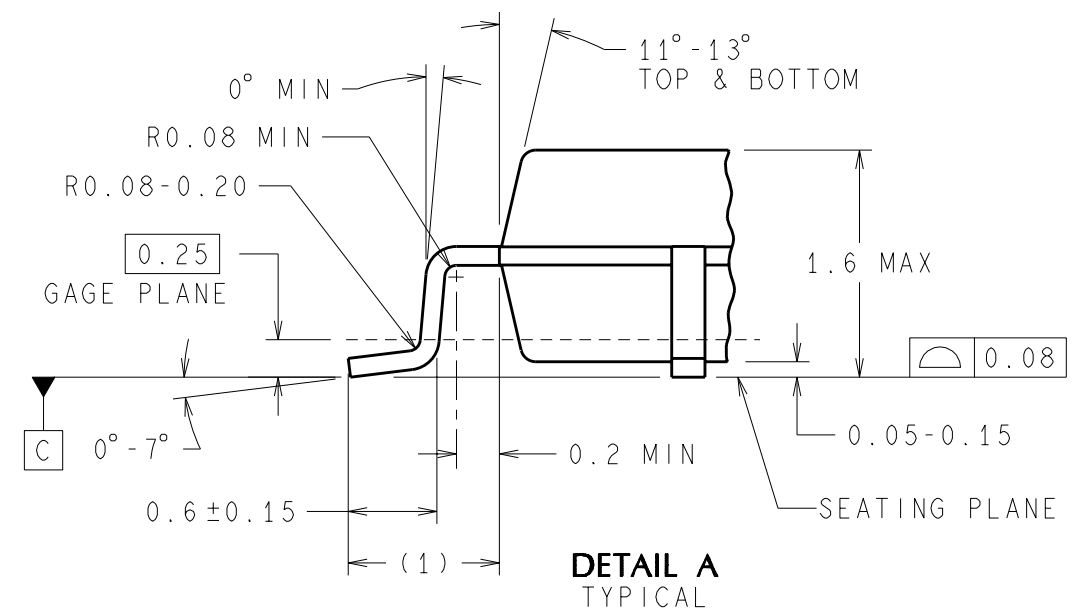


REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW	10176	01/26/1994	DEG/HJK
D	TITLE: LOFP WAS POFP; UPDATE NOTE 3; ADD GEOMETRIC TOLERANCE	12317	11/30/1999	ACS/MS/RW
E	ADD LAND PATTERN; UPDATE NOTE 1, TITLE & REFORMAT DWG IN B SIZE PER CURRENT STD	1729	02/16/2005	TL/RW



RECOMMENDED LAND PATTERN



DETAIL A TYPICAL

NOTES: UNLESS OTHERWISE SPECIFIED

- FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com)
- DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
- REFERENCE JEDEC REGISTRATION MS-026, VARIATION BDD.

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

APPROVALS		DATE	 2900 Semiconductor Dr., Santa Clara, CA 95052-8090
DRAWN	DE GRADY	01/26/1994	
DFTG. CHK.	MARTA SUCHY	02/16/2005	
ENGR. CHK.	RANDALL WALBERG	02/16/2005	
PROJECTION:			SCALE: NTS SIZE: B DRAWING NUMBER: (SC)MKT-VHG80A FORMERLY: N/A
			REV: E SHEET 1 of 1