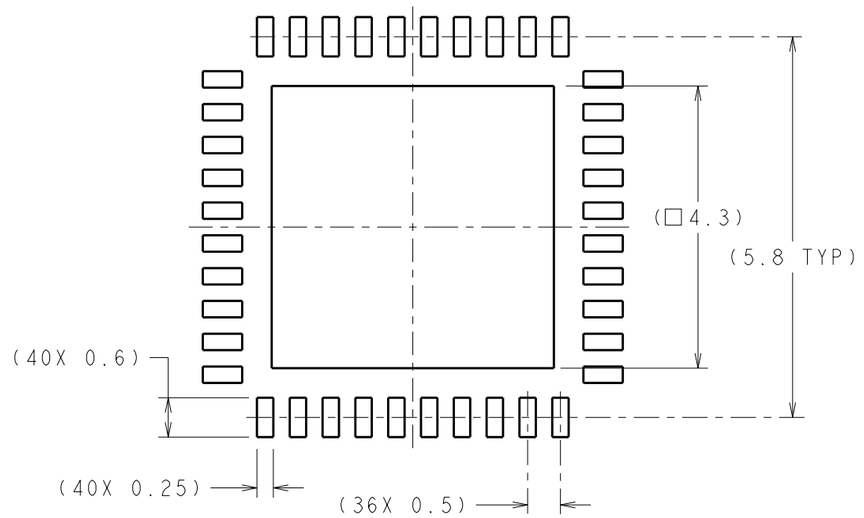
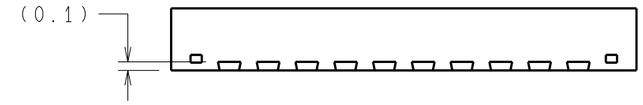
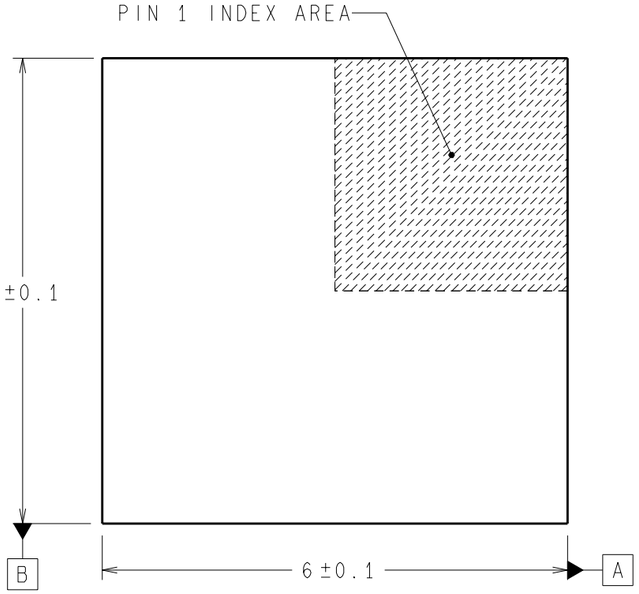
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1438	03/22/2004	MS/AT

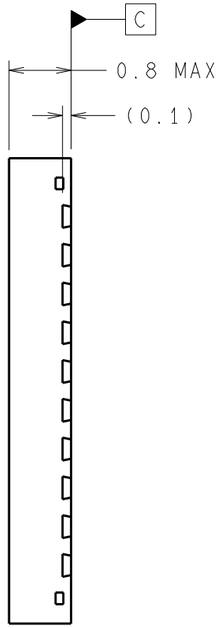


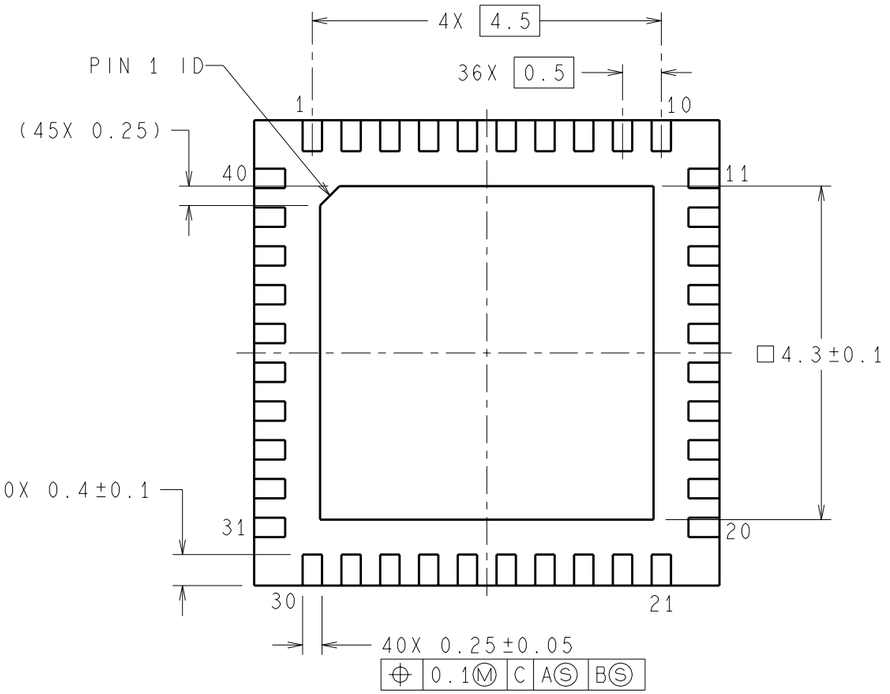
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF MARCH 2004.

APPROVALS	DATE
DRAWN: MARTA SUCHY	03/22/2004
DFTG. CHK.: THANH LEQUANG	03/22/2004
ENGR. CHK.: ANNY TU	03/22/2004

PROJECTION: MM

National Semiconductor
2900 Semiconductor Dr. Santa Clara, CA 95052-8090

LLP, QUAD, 6x6x0.8mm,
40 LD, SMALL DAP,
0.5mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SQA40B	A

FORMERLY: N/A

SHEET 1 of 1