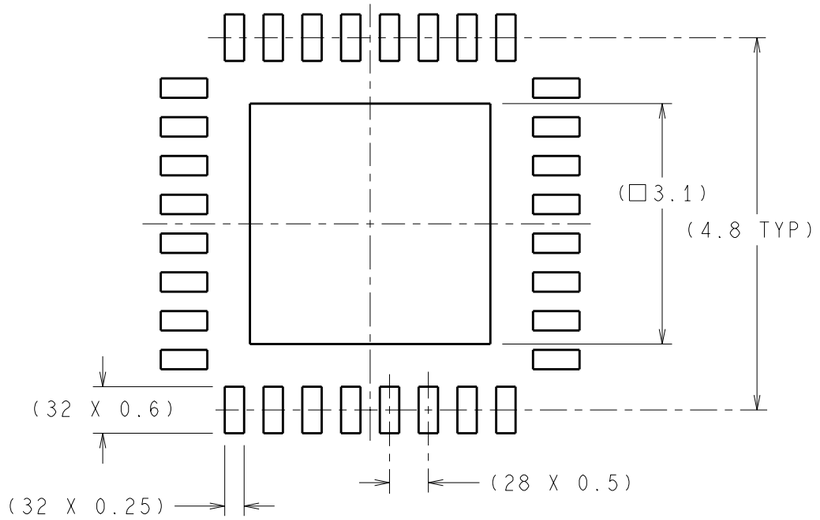
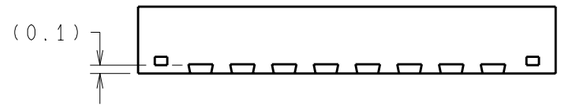
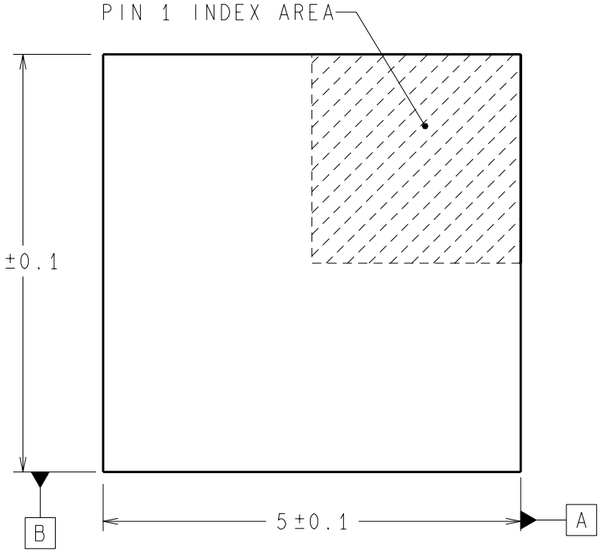
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1456	07/06/2004	HL/MS/SN

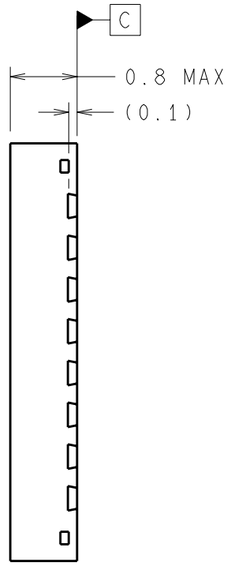


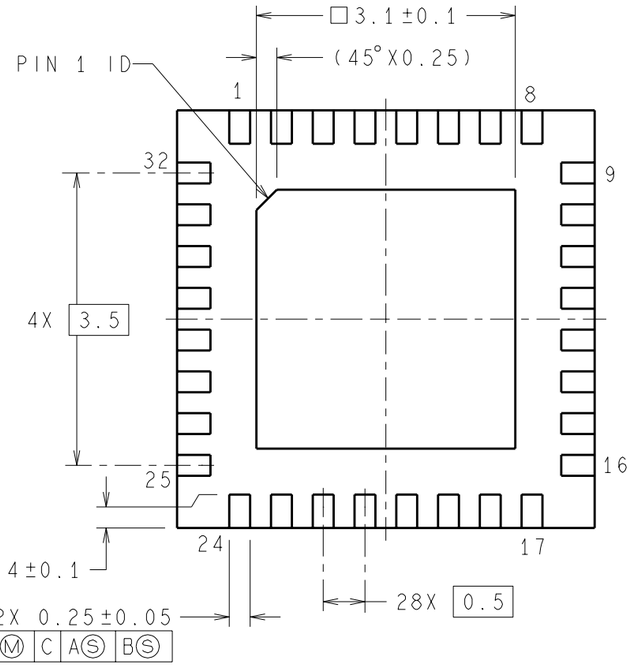
DIMENSIONS ARE IN MILLIMITERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN







NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMANTION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. NO JEDEC REGISTRATION AS OF JULY 2004.

APPROVALS	DATE
DRAWN: HENRY LIM	07/06/2004
DFTG. CHK.: MARTA SUCHY	07/06/2004
ENGR. CHK.: SANTHIRAN N	07/06/2004

PROJECTION: MM

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

LLP,QUAD,5x5x0.8mm,32 LD, 0.5mm PITCH,NO PULLBACK, 3.1x3.1mm EXP PAD

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SQA32A	A

FORMERLY: N/A