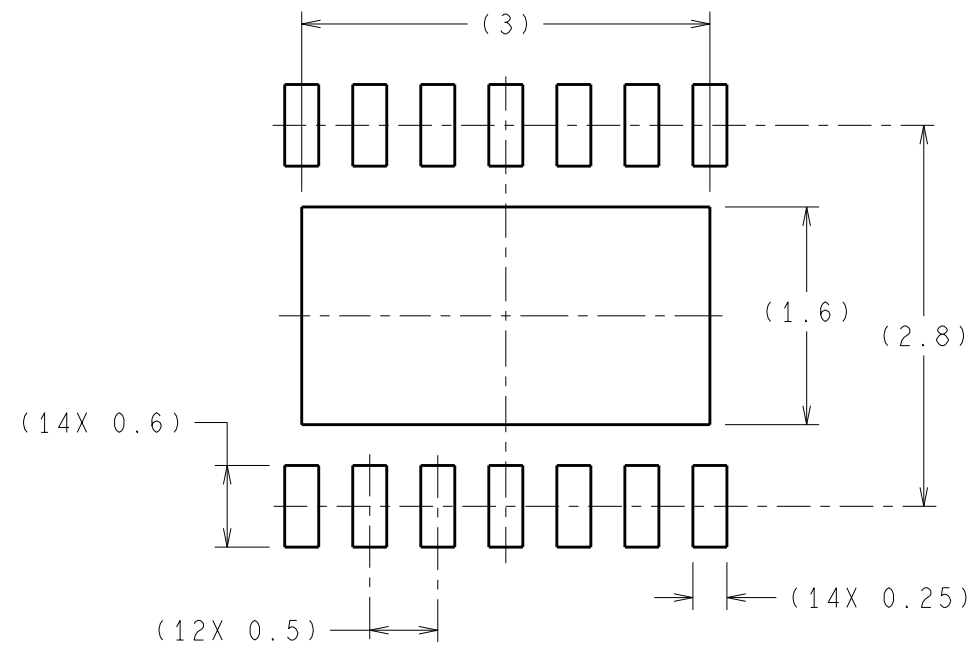
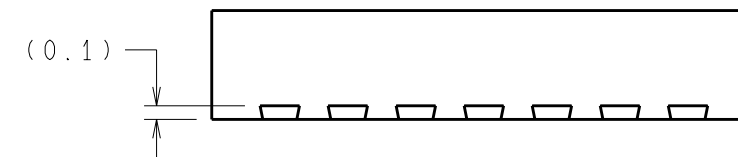


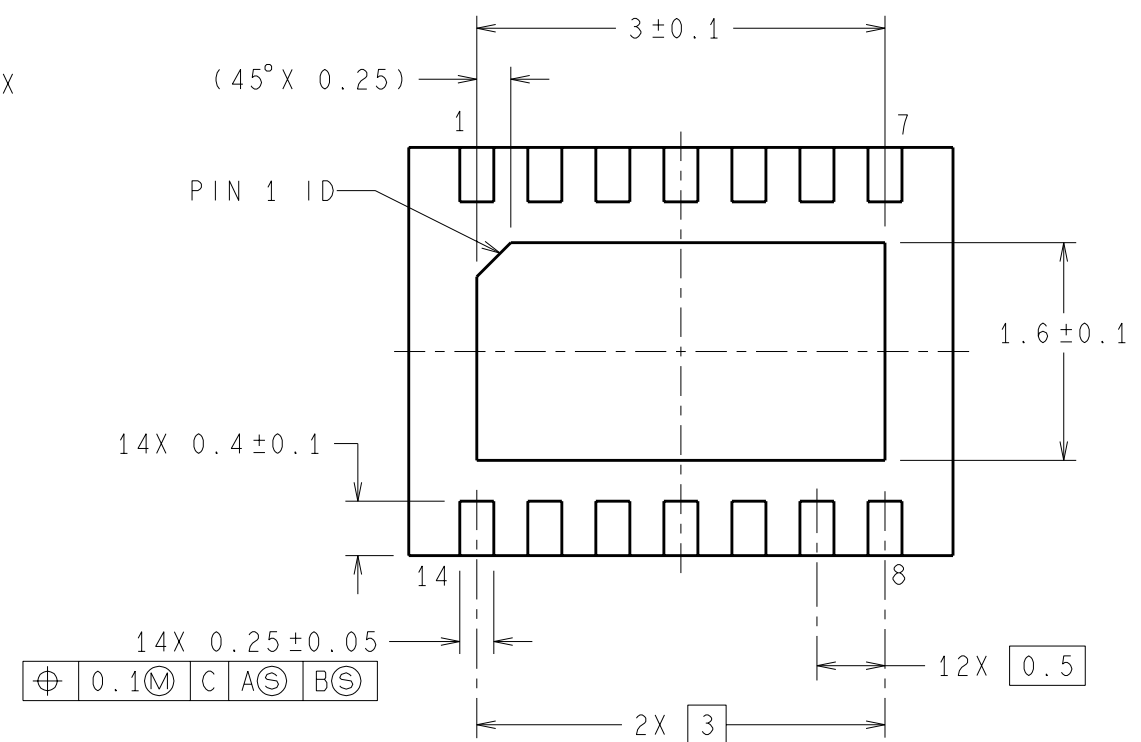
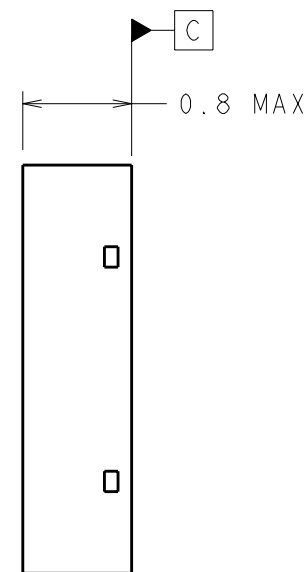
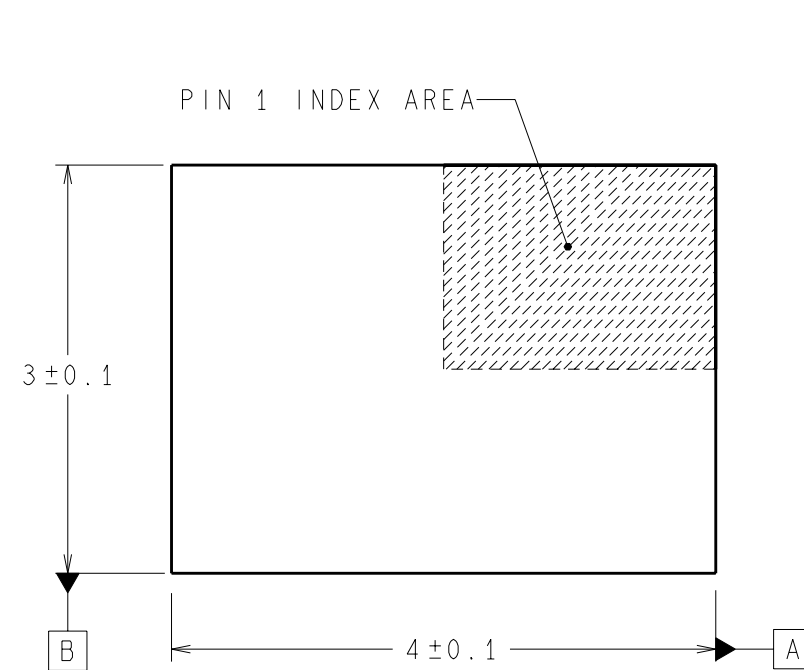
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1104	06/30/2003	AS/TL/SN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED.

- FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
- NO JEDEC REGISTRATION AS OF JUNE 2003.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	ASNOR SULAIMAN	06/30/2003		
DFTG. CHK.	THANH LEQUANG	06/30/2003	LLP, PLASTIC, DUAL, 4x3x0.8mm BODY, 14 LD 0.5 mm PITCH, NO PULLBACK	
ENGR. CHK.	SANTHIRAN N	06/30/2003		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
 MM	NTS	B	(SC)MKT-SDA14A	A
FORMERLY: N/A			SHEET 1 of 1	