



# STS3DPF60L

## DUAL P-CHANNEL 60V - 0.10 $\Omega$ - 3A SO-8 STripFET™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS3DPF60L	60 V	< 0.12 $\Omega$	3 A

- TYPICAL R<sub>DS(on)</sub> = 0.10  $\Omega$  @ 10V
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

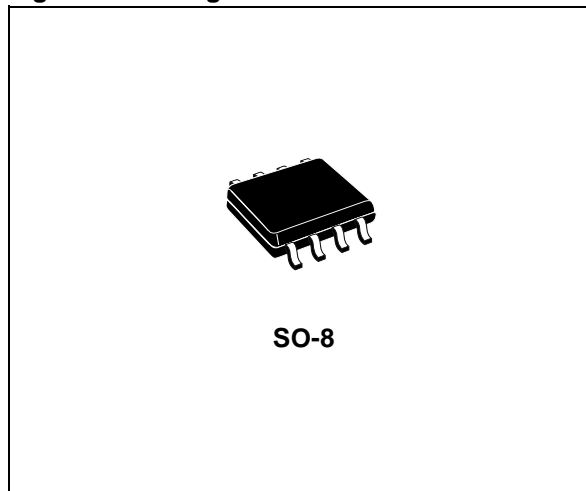
### DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

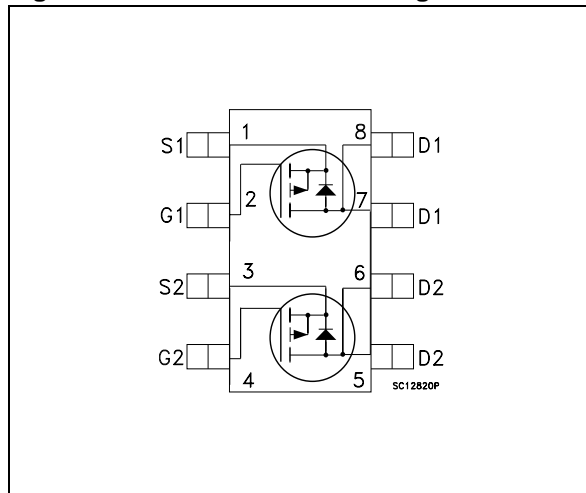
### APPLICATIONS

- DC-DC CONVERTERS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS3DPF60L	S3DPF60L	SO-8	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	60	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	60	V
$V_{GS}$	Gate- source Voltage	$\pm 16$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	3	A
	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	1.9	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	12	A
$P_{tot}$	Total Dissipation at $T_C = 25^\circ\text{C}$	2	W
$T_{stg}$	Storage Temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating Junction Temperature		

( $\bullet$ ) Pulse width limited by safe operating area.

**Table 4: Thermal Data**

$R_{thj-amb}$	(*)Thermal Resistance Junction-ambient	62.5	$^\circ\text{C}/\text{W}$
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(\*) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu  $t \leq 10\text{ s}$

**ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**

**Table 5: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$			1	$\mu\text{A}$
		$V_{DS} = \text{Max Rating}, T_C = 125^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$		0.10	0.12	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$		0.130	0.160	$\Omega$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(*)}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 3\text{ A}$		7.2		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		630 121 49		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}, I_D = 1.5\text{ A}$ $R_G = 4.7\ \Omega, V_{GS} = 4.5\text{ V}$ (see Figure 16)		124 54 39 14.5		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}, I_D = 3\text{ A}, V_{GS} = 4.5\text{ V}$ (see Figure 19)		11.6 4.5 4.7	15.7	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(\bullet)}$	Source-drain Current Source-drain Current (pulsed)				3 12	A A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 3\text{ A}, V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}, T_j = 150^\circ\text{C}$ (see Figure 17)		44 68.2 3.1		ns nC A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

( $\bullet$ ) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

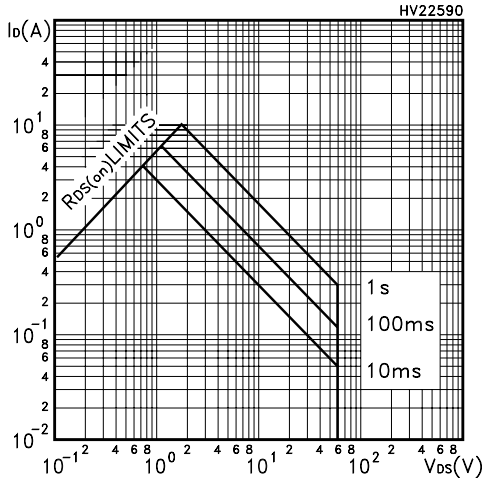


Figure 4: Output Characteristics

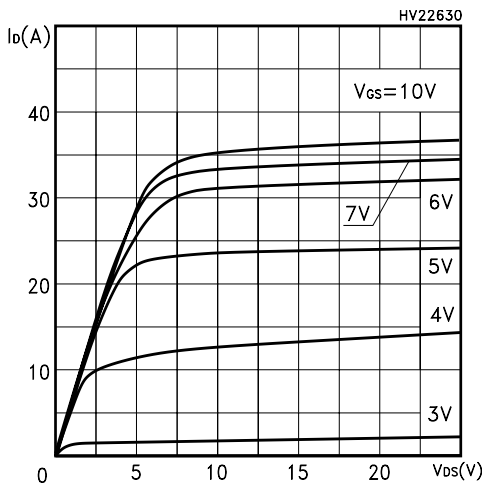


Figure 5: Transconductance

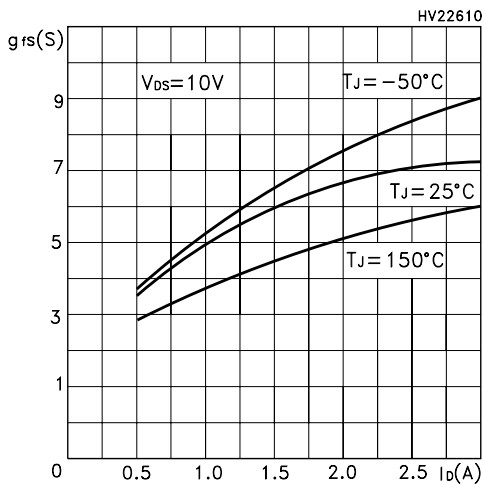


Figure 6: Thermal Impedance

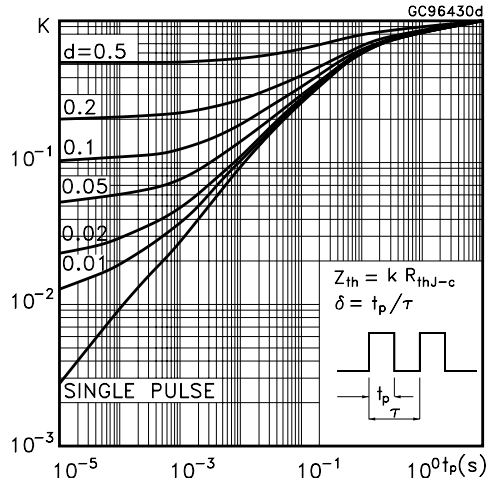


Figure 7: Transfer Characteristics

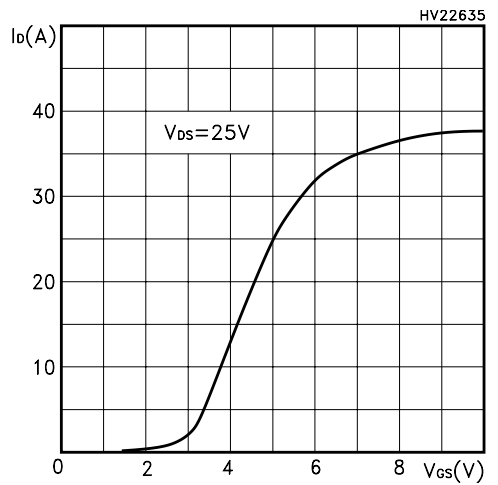


Figure 8: Static Drain-source On Resistance

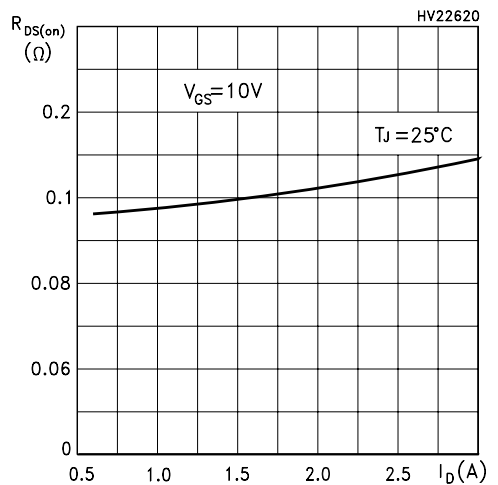


Figure 9: Gate Charge vs Gate-source Voltage

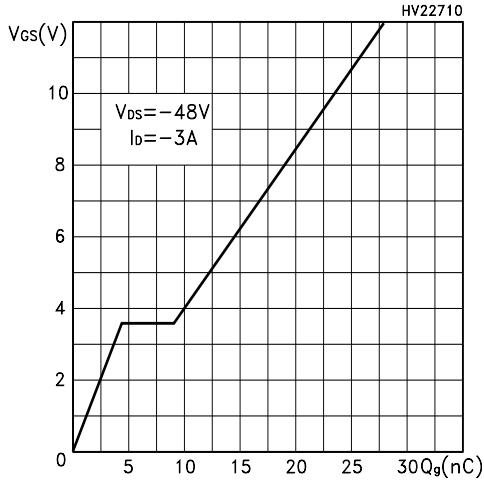


Figure 10: Normalized Gate Threshold Voltage vs Temperature

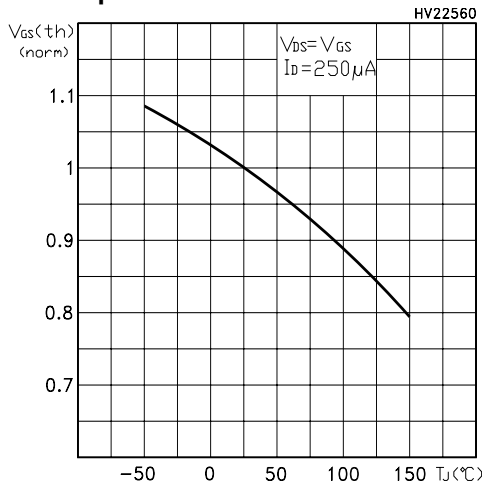


Figure 11: Dource-Drain Diode Forward Characteristics

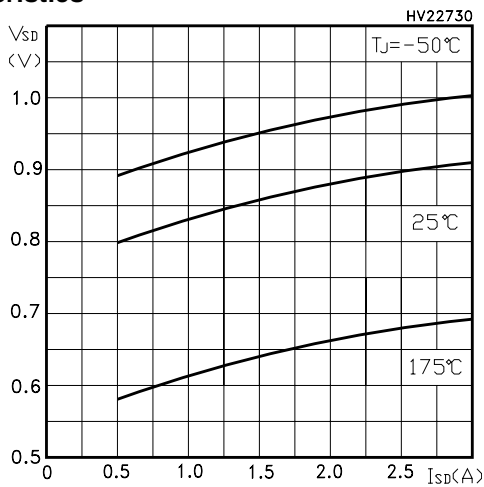


Figure 12: Capacitance Variations

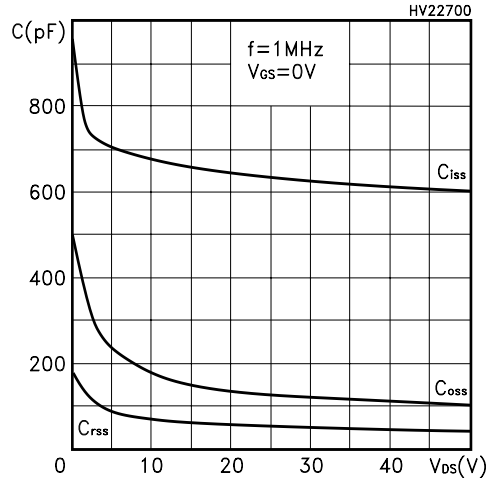


Figure 13: Normalized On Resistance vs Temperature

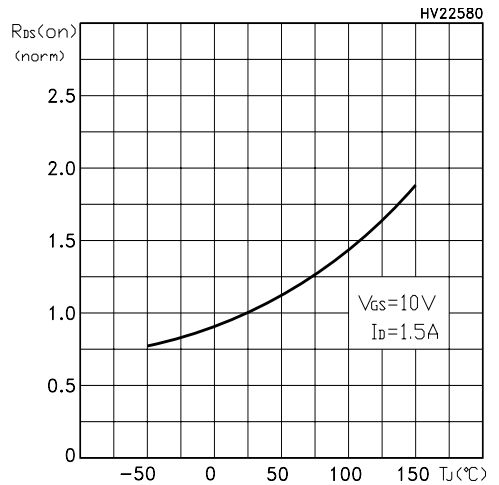


Figure 14: Normalized Breakdown Voltage vs Temperature

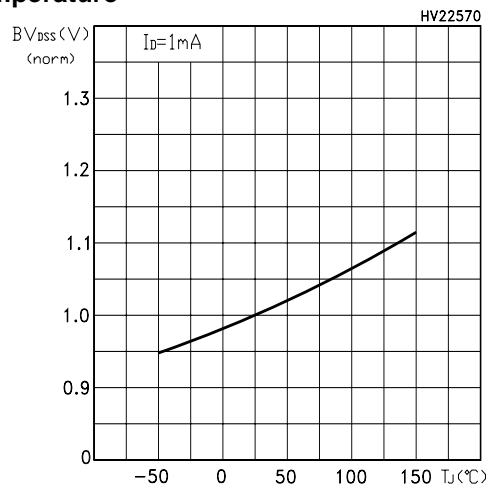


Figure 15: Unclamped Inductive Load Test Circuit

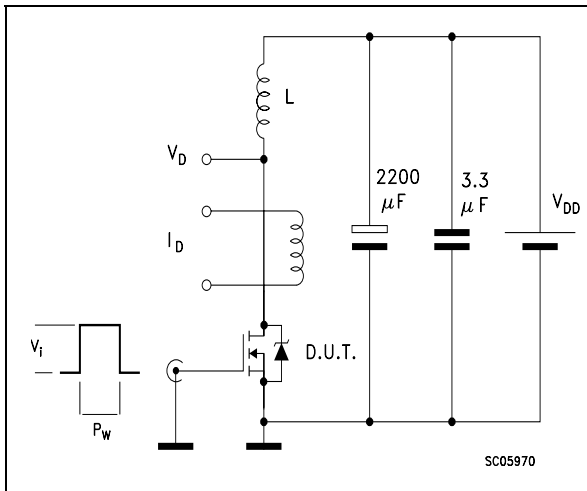


Figure 16: Switching Times Test Circuit For Resistive Load

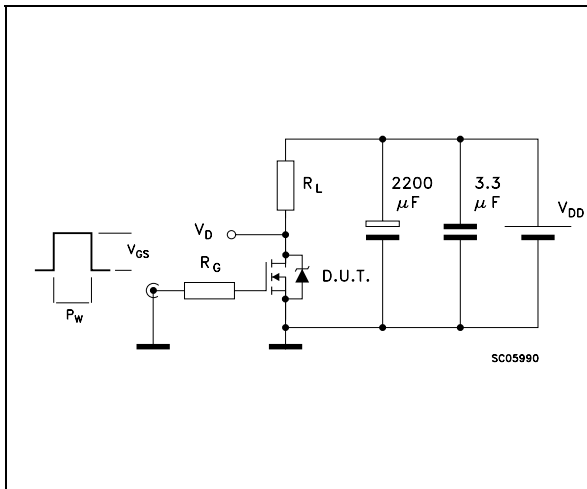


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

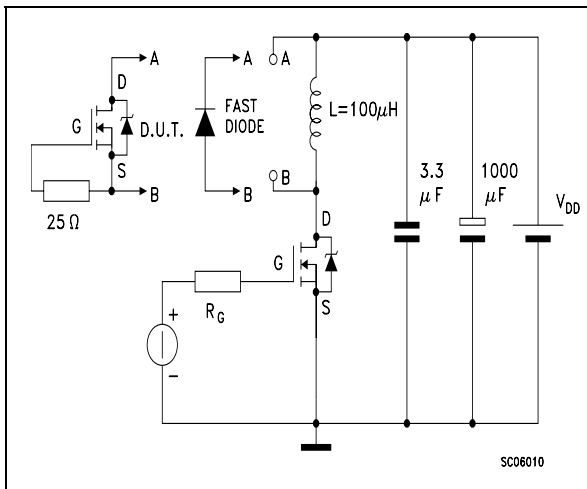


Figure 18: Unclamped Inductive Waferform

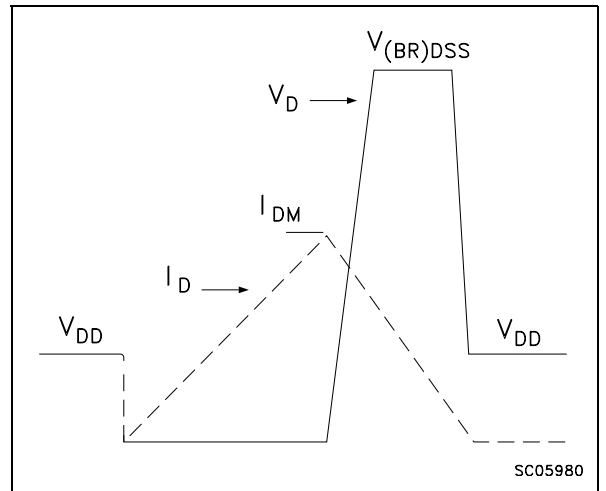
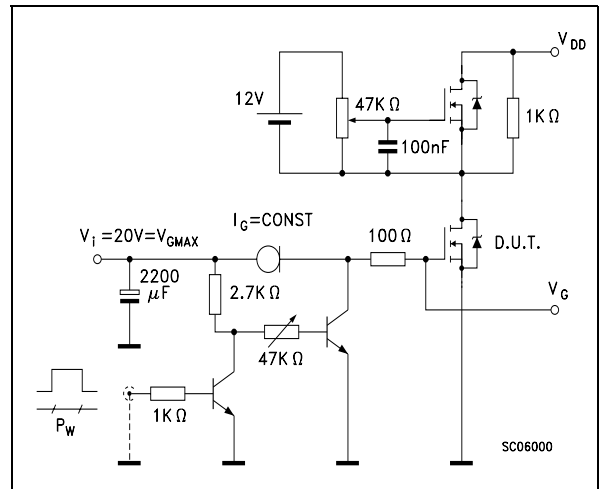
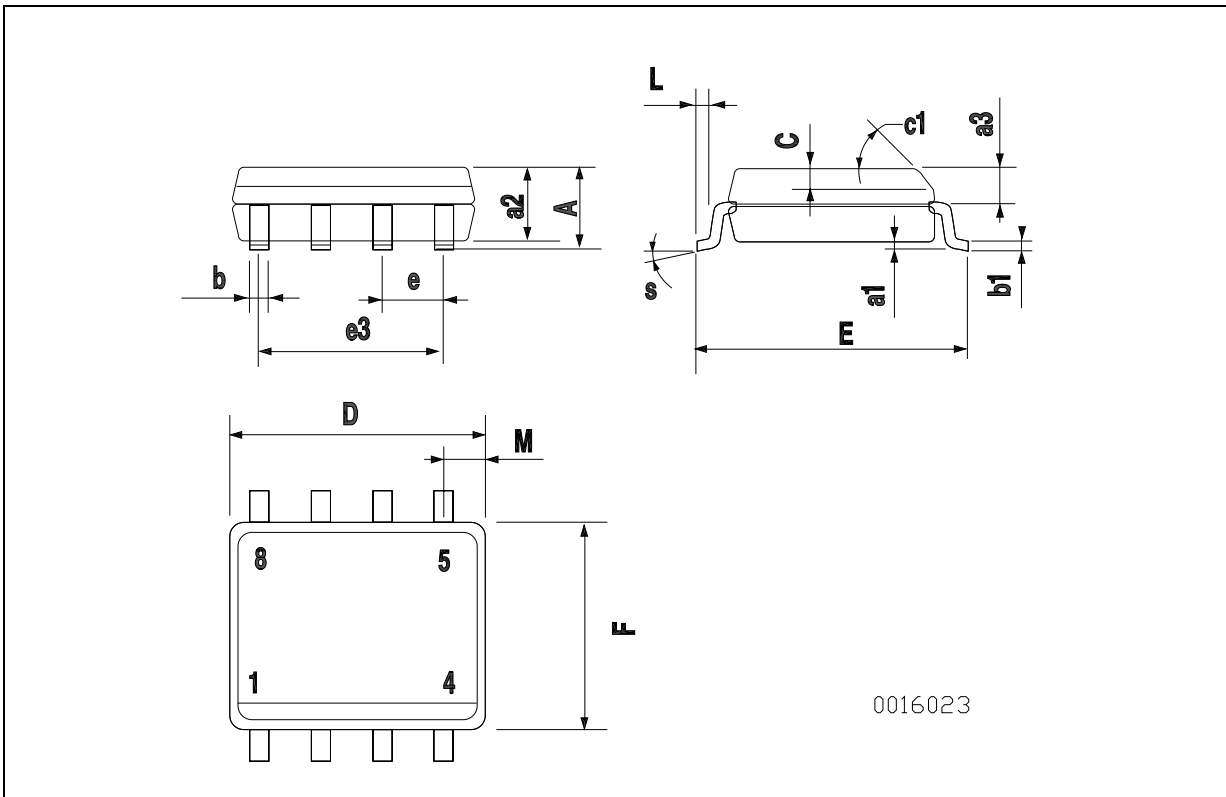


Figure 19: Gate Charge Test Circuit



**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

**Table 8: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
16-Sep-2004	1	New release.



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