



STP16NK60Z - STB16NK60Z-S STW16NK60Z

N-CHANNEL 600V - 0.38 Ω - 14 A TO-220 /I²SPAK/TO-247

Zener - Protecdet SuperMESH™ MOSFET

TARGET SPECIFICATION

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP16NK60Z	600 V	< 0.42 Ω	14 A	190 W
STB16NK60Z-S	600 V	< 0.42 Ω	14 A	190 W
STW16NK60Z	600 V	< 0.42 Ω	14 A	190 W

- TYPICAL R_{DS(on)} = 0.38 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES

Figure 1: Package

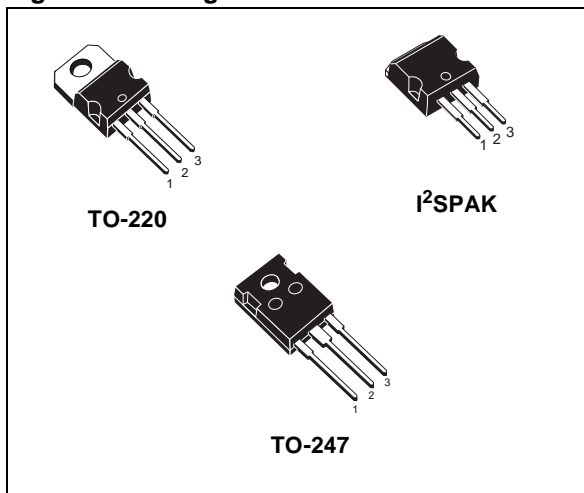


Figure 2: Internal Schematic Diagram

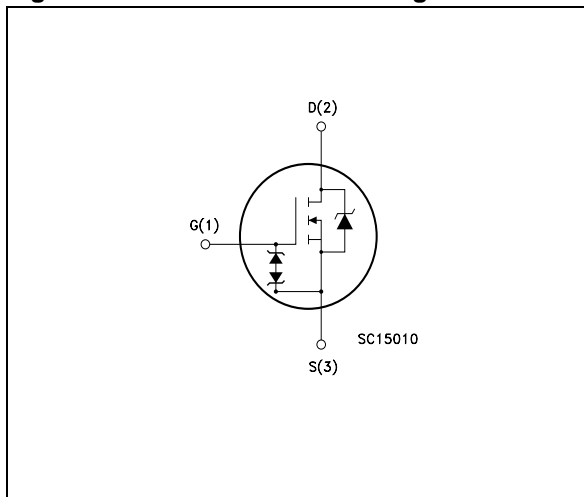


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP16NK60Z	P16NK60Z	TO-220	TUBE
STB16NK60Z-S	B16NK60Z	I ² SPAK	TUBE
STW16NK60Z	W16NK60Z	TO-247	TUBE

Rev. 1

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	600	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	14	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	8.8	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	56	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	190	W
	Derating Factor	1.51	W/ $^\circ\text{C}$
$V_{ESD}(G-S)$	Gate source ESD (HBM-C= 100pF, R= 1.5K Ω)	6000	V

●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 14\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 4: Thermal Data

		TO-220/ P ² SPAK	TO-247
Rthj-case	Thermal Resistance Junction-case Max	0.66	
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	50
T_I	Maximum Lead Temperature For Soldering Purpose	300	

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	14	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	360	mJ

Table 6: GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{ mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\ \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 7\text{ A}$		0.38	0.42	Ω
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	600			V

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 7\text{ A}$		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1\text{ MHz}, V_{GS} = 0$		2650 285 62		pF pF pF
$C_{oss\ eq. (*)}$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V\text{ to }480V$		158		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 480\text{ V}, I_D = 14\text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		30 25 70 15		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V, I_D = 14\text{ A},$ $V_{GS} = 10V$		86 17 46		nC nC nC

(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				14 56	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 14\text{ A}, V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 14\text{ A}, di/dt = 100\text{ A}/\mu s$ $V_{DD} = 100\text{ V}, T_j = 25^{\circ}C$ (see test circuit, Figure 5)		490 5.4 22		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 14\text{ A}, di/dt = 100\text{ A}/\mu s$ $V_{DD} = 100\text{ V}, T_j = 150^{\circ}C$ (see test circuit, Figure 5)		585 7 24		ns μC A
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				14 56	A A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Figure 3: Unclamped Inductive Load Test Circuit

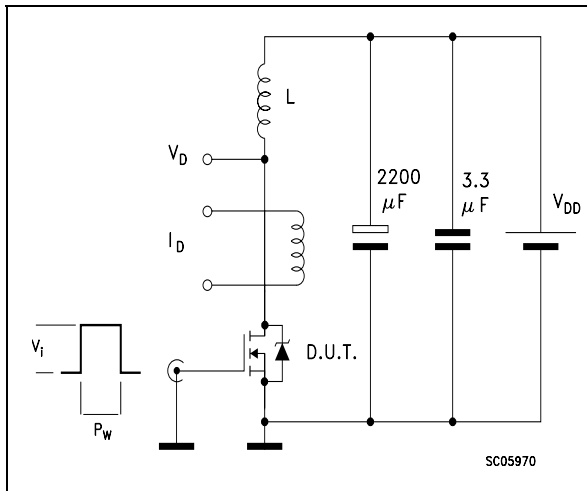


Figure 4: Switching Times Test Circuit For Resistive Load

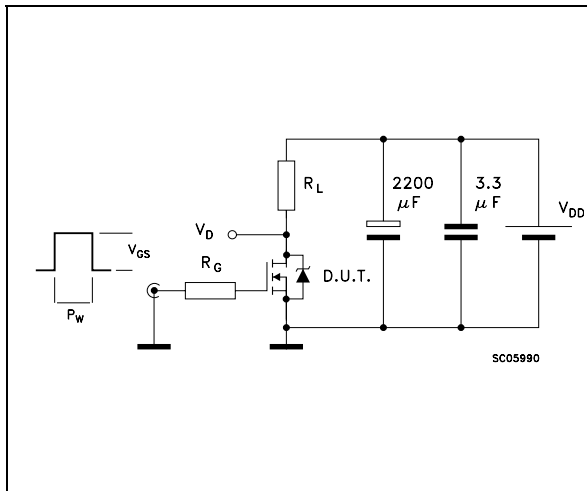


Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times

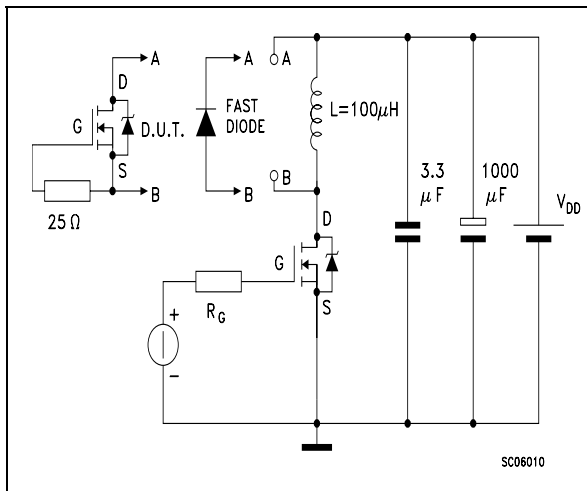


Figure 6: Unclamped Inductive Waferform

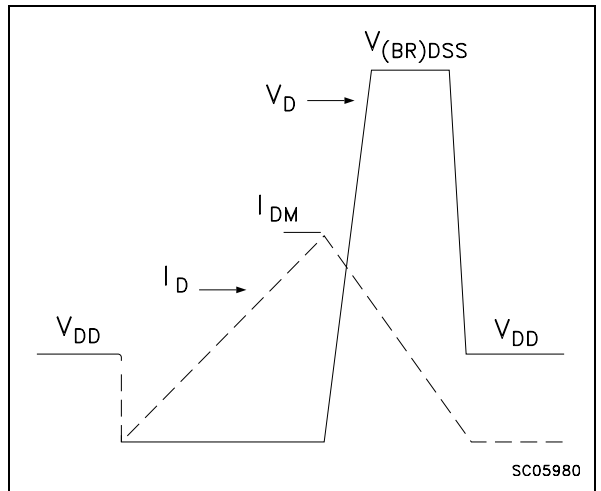
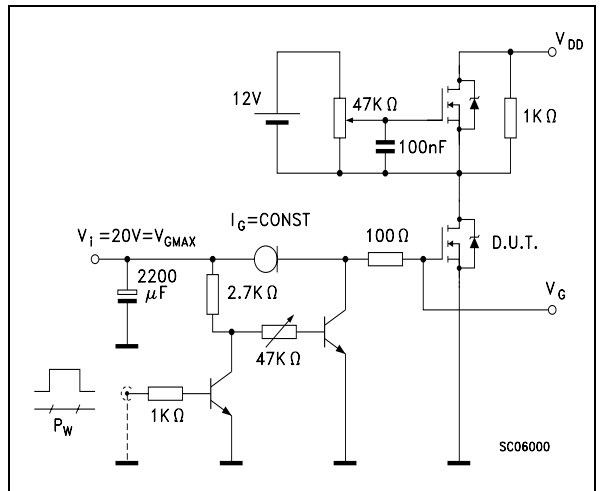


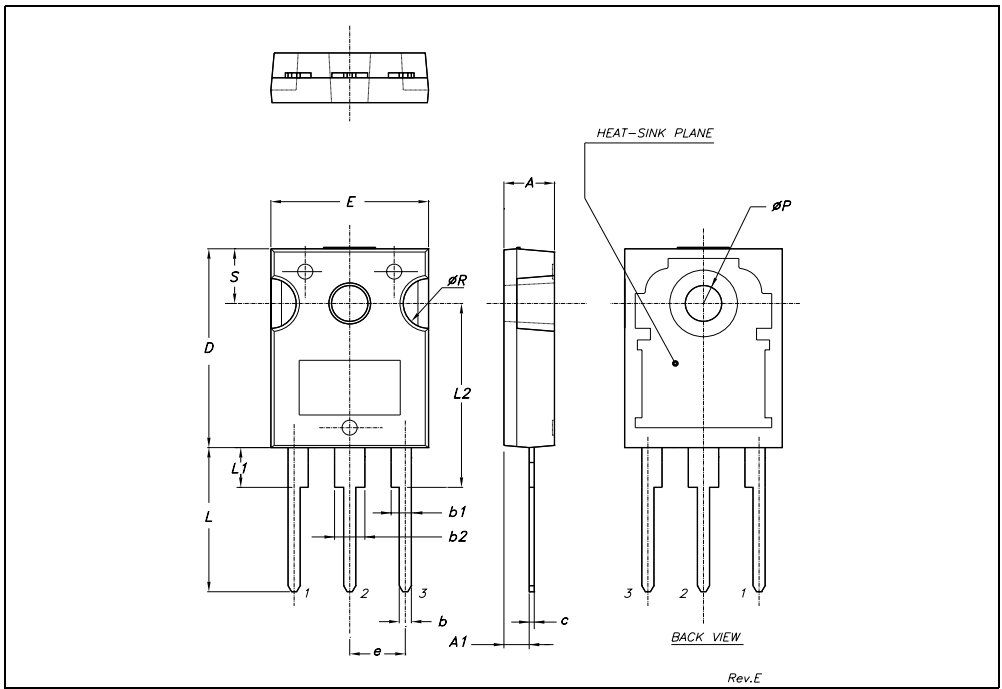
Figure 7: Gate Charge Test Circuit



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

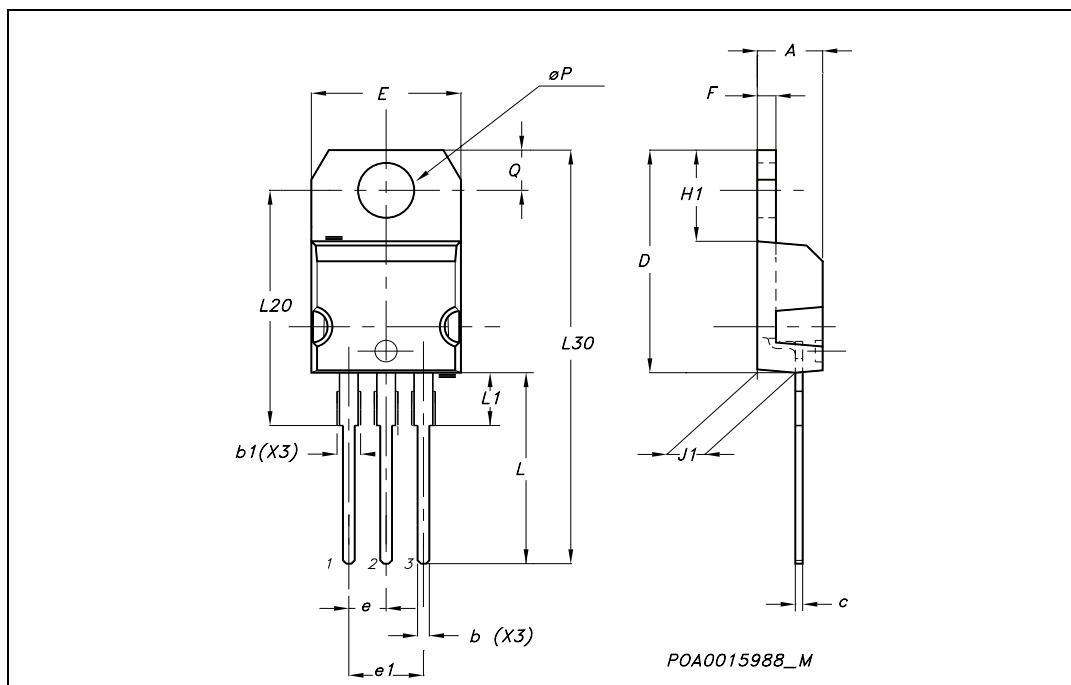
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



I²SPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.70		0.93	0.027		0.037
B2	1.14		1.70	0.045		0.067
C	0.45		0.60	0.018		0.024
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10.00		10.40	0.394		0.409
G	4.88		5.28	0.192		0.208
L	16.7		17.5	0.657		0.689
L2	1.27		1.4	0.05		0.055
L3	13.82		14.42	0.544		0.568

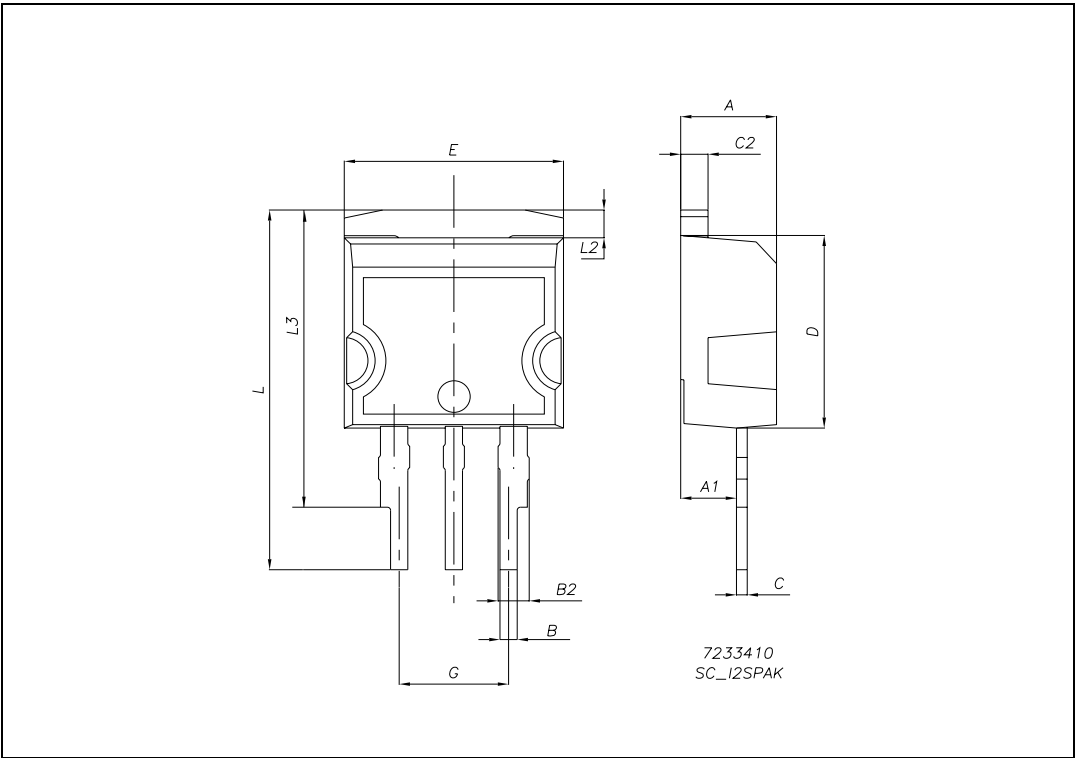


Table 10: Revision History

Date	Revision	Description of Changes
06-Jul-2004	1	First Release.
06-Sep-2005	2	Inserted Ecopak indication

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