ISD14B20

SINGLE-CHIP, MULTIPLE-MESSAGE

VOICE RECORD/PLAYBACK DEVICE

10.6- TO 32-SECONDS DURATION

Publication Release Date: October 9, 2007

winbond

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1. GENERAL DESCRIPTION

Winbond's ISD14B20 ChipCorder® is a new single-chip multiple-message record/playback series with dual operating modes (address trigger and direct trigger) with wide operating voltage ranging from 2.4V to 5.5V. The sampling frequency can be selected from 4 to 12 kHz via an external resistor, which also determines the duration from 10.6 to 32 seconds. The device is designed for mostly standalone applications, and of course, it can be manipulated by a microcontroller, if necessary.

The two operating modes are address trigger and direct trigger. While in address trigger mode, both record and playback operations are manipulated according to the start address and end address specified through the start address and end address pins. However, in direct trigger mode, the device can configure the memory up to as many as eight equal messages, pending upon the fixed message configuration settings. With the record or playback feature being pre-selected, each message can be randomly accessed via its message control pin.

The device has a selectable differential microphone input with AGC feature or single-ended analog input, AnaIn, under feed-through mode. Its differential Class D PWM speaker driver can directly drive a typical speaker or buzzer.

2. FEATURES

The ISD14B20 is a multiple messages record/playback device with two operational modes: address trigger (**NORM**) and direct trigger (**$\overline{\text{MODE}}$**). The analog inputs and the outputs are:

- Supply voltage: 2.4V to 5.5V.
- External resistor, Rosc, selects sampling frequency and duration.

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	53.3 KΩ	80 KΩ	100 KΩ	120 KΩ	160 KΩ

- Mic+/Mic- : differential microphone inputs.
- AGC : automatic gain control for microphone preamp circuit.
- **$\overline{\text{FT}}$** : feed-through the AnaIn signal to the speaker outputs while AnaIn is converted from MIC+.
- When both **$\overline{\text{FT}}$** and recording are active, device will record AnaIn signal into memory with AnaIn signal output to speaker simultaneously.
- SP+/SP- : Class-D PWM differential speaker drivers.
- **$\overline{\text{LED}}$** : during recording, LED is on.
- Automatically power down after each operation cycle.
- Playback takes precedence over the recording operation.
- Temperature option: 0°C to +50°C (die)
- Packaging: die only

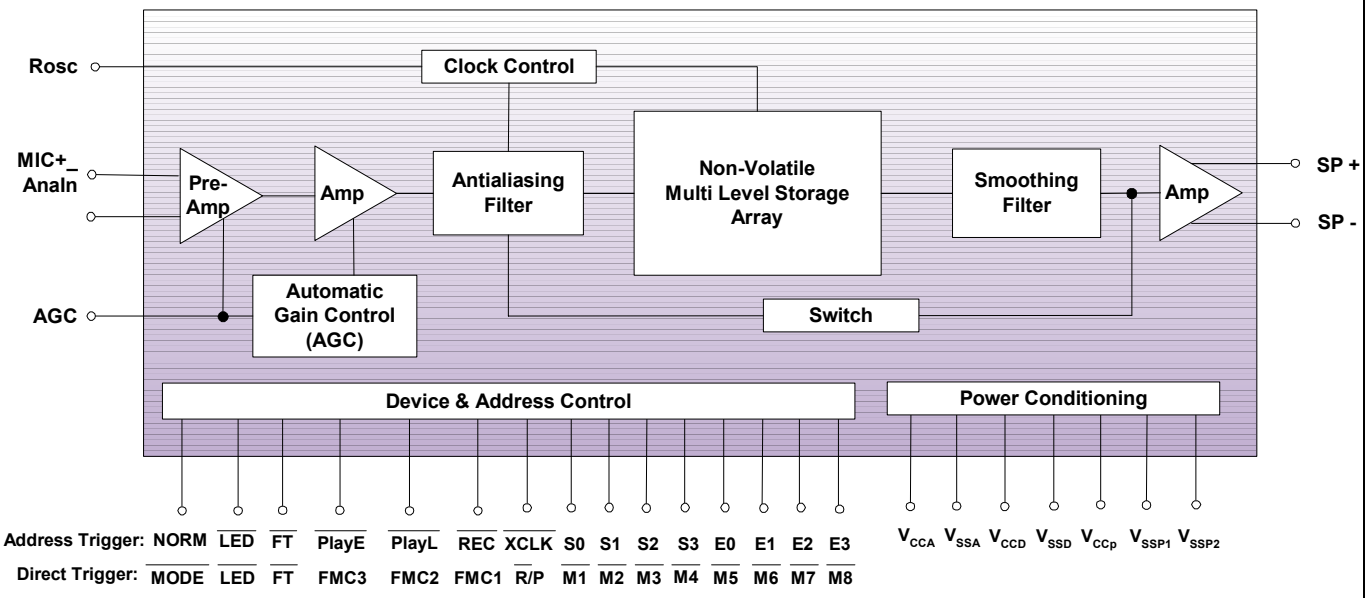
2.1. Address trigger operational mode

- While in **NORM** mode, flexible message duration is defined by start address and end address.
- Utilize four start addresses (**S0**, **S1**, **S2** & **S3**) and four end addresses (**E0**, **E1**, **E2** & **E3**) to specific the message duration.
- $\overline{\textbf{REC}}$: Level-hold or Edge-trigger (toggle on-off) recording from start to end addresses.
- $\overline{\textbf{PLAYE}}$: Edge-trigger playback from start to end addresses and stops at EOM marker, if EOM is prior to end address. Toggle on-off.
- $\overline{\textbf{PLAYL}}$: Level-hold playback from start to end addresses. Also, if constantly Low, device will loop playback from start to end addresses.

2.2. Direct trigger operational mode

- While $\overline{\textbf{MODE}}$ is active, utilizing, **FMC1**, **FMC2** & **FMC3**, the device reconfigures some pins to adapt various (1 to 8) fixed equal message configurations for random access and pre-defines the fixed message duration accordingly.
- The control pins are: $\overline{\textbf{M1}}$~$\overline{\textbf{M8}}$ (message activation) and $\overline{\textbf{R/P}}$ (record or playback selection).
- The record or playback operation is pre-defined by the $\overline{\textbf{R/P}}$ pin.
- Each message can be randomly accessed via its message control pin ($\overline{\textbf{M1}}$~$\overline{\textbf{M8}}$) and the desired operation is facilitated accordingly.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

PAD NAME	I / O	FUNCTION
V_{SSD}	I	**Digital Ground**: Ground path for digital circuits.
S0 / $\overline{\text{M1}}$	I	**S0** [1]: In **Norm** mode, Start Address Bit 0. $\overline{\text{M1}}$: When $\overline{\text{MODE}}$ is active, low active operation on 1st Message. Internal pull-up & debounce existed.
S1 / $\overline{\text{M2}}$	I	**S1** [1]: In **Norm** mode, Start Address Bit 1. $\overline{\text{M2}}$: When $\overline{\text{MODE}}$ is active, low active operation on 2nd Message. Internal pull-up & debounce existed.
S2 / $\overline{\text{M3}}$	I	**S2** [1]: In **Norm** mode, Start Address Bit 2. $\overline{\text{M3}}$: When $\overline{\text{MODE}}$ is active, low active operation on 3rd Message. Internal pull-up & debounce existed.
S3 / $\overline{\text{M4}}$	I	**S3** [1]: In **Norm** mode, Start Address Bit 3. $\overline{\text{M4}}$: When $\overline{\text{MODE}}$ is active, low active operation on 4th Message. Internal pull-up & debounce existed.
$\overline{\text{PLAYL}}$ / FMC1	I	$\overline{\text{PLAYL}}$: In **Norm** mode, low active input, Level-hold playback start to end addresses, debounce & internal pull-up existed. Holding $\overline{\text{PLAYL}}$ Low constantly will perform looping playback function from start to end addresses with insignificant dead time between messages regardless of sampling frequencies. **FMC1**: When $\overline{\text{MODE}}$ is active, **FMC1**, together with **FMC2** & **FMC3**, setup various fixed-message configurations.
E0 / $\overline{\text{M5}}$	I	**E0** [1]: In **Norm** mode, End Address Bit 0. $\overline{\text{M5}}$: When $\overline{\text{MODE}}$ is active, low active operation on 5th Message. Internal pull-up & debounce existed.
V_{SSA}	I	**Analog Ground**: Ground path for analog circuits.
E1 / $\overline{\text{M6}}$	I	**E1** [1]: In **Norm** mode, End Address Bit 1. $\overline{\text{M6}}$: When $\overline{\text{MODE}}$ is active, low active operation on 6th Message. Internal pull-up & debounce existed.
E2 / $\overline{\text{M7}}$	I	**E2** [1]: In **Norm** mode, End Address Bit 2. $\overline{\text{M7}}$: When $\overline{\text{MODE}}$ is active, low active operation on 7th Message. Internal pull-up & debounce existed.
E3 / $\overline{\text{M8}}$	I	**E3** [1]: In **Norm** mode, End Address Bit 3. $\overline{\text{M8}}$: When $\overline{\text{MODE}}$ is active, low active operation on 8th Message. Internal pull-up & debounce existed.
V_{SSP2}	I	**Ground**: Ground for negative PWM speaker driver.
SP-	O	**SP-**: Negative signal of the differential Class-D PWM speaker outputs. This output, together with the SP+, is used to drive an 8Ω speaker directly.
V_{CCP}	I	**Speaker Power Supply**: Power supply for PWM speaker drivers.
SP+	O	**SP+**: Positive signal of the differential Class-D PWM speaker outputs. This output, together with the SP-, is used to drive an 8Ω speaker directly.
V_{SSP1}	I	**Ground**: Ground for positive PWM speaker driver.
AGC	I	**Automatic Gain Control (AGC)**: The AGC adjusts the gain of the microphone preamplifier circuitry.
MIC+ / AnaIn	I	• **MIC+ :** Non-inverting input of the differential microphone signal. • **AnaIn :** When $\overline{\text{FT}}$ is selected, the MIC+ input is configured to a single-ended input with 1Vp-p maximum input amplitude and feed-through to the speaker outputs.

<table>
<tr><th>PAD NAME</th><th>I / O</th><th>FUNCTION</th></tr>
<tr><td>MIC-</td><td>I</td><td>MIC- : Inverting input of the differential microphone signal. While FT is enabled, MIC- pin is disabled and must be floated.</td></tr>
<tr><td>Rosc</td><td>I</td><td>Oscillator Resistor: Connect an external resistor from this pin to V_{SSA} to select the internal sampling frequency.</td></tr>
<tr><td>V_{CCA}</td><td>I</td><td>Analog Power Supply: Power supply for analog circuits.</td></tr>
<tr><td>LED</td><td>O</td><td>LED output: During recording, this output is Low. Also, LED pulses Low momentarily at the end of playback.</td></tr>
<tr><td>PLAYE / FMC2</td><td>I</td><td>PLAYE : In Norm mode, low active input, edge-trigger playback from start to end addresses & toggle on-off. Debounce & internal pull-up existed.
FMC2 : When MODE is active, FMC2 , together with FMC1 & FMC3 , setup various fixed-message configurations.</td></tr>
<tr><td>REC / R/P</td><td>I</td><td>REC : In Norm mode, level-hold (after 1 sec holding) or edge-trigger (toggle on-off), low active, recording from start to end addresses. Debounce & internal pull-up existed.
R/P (When MODE is active):
When R/P is set to Low, level-hold record operation is selected.
When R/P is set to High, edge-trigger & toggle on-off playback operation is selected.</td></tr>
<tr><td>XCLK / FMC3</td><td>I</td><td>External Clock: In Norm mode, low active and level-hold input. As XCLK activated, Rosc pin accepts external clock input signal, provided resistor at Rosc must be removed. Connecting this pin to High enables device running on internal clock via Rosc resistor. If not used, XCLK must be at high level.
When MODE is active, FMC3 , together with FMC1 & FMC2 , setup various fixed-message configurations.</td></tr>
<tr><td>FT</td><td>I</td><td>Feed-Through : Low active input, Level-hold, debounce & Internal pull-up required.
When FT is selected, the MIC+ input is configured to a single-ended input with 1Vp-p maximum input amplitude and feed-through to the speaker outputs.</td></tr>
<tr><td>Norm / MODE</td><td>I</td><td>Level-hold input.
Norm : When set to High, the device operates under Address trigger condition.
MODE : When set to Low, the device operates under direct trigger condition. The device reconfigures its pin definitions to fit various fixed-message configurations utilizing FMC1 , FMC2 & FMC3 pins as below table.
<table>
<tr><th>FMC3</th><th>FMC2</th><th>FMC1</th><th># of fixed messages</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>8</td></tr>
</table></td></tr>
<tr><td>V_{CCD}</td><td>I</td><td>Digital Power Supply: Power supply for digital circuits.</td></tr>
</table>

Notes: [1] : Address bits **S0** , **S1** , **S2** , **S3** , **E0** , **E1** , **E2** & **E3** are used to access the memory location.

5. FUNCTIONAL DESCRIPTION

There are two operational modes: address trigger (**NORM**) and direct trigger (**$\overline{\text{MODE}}$**). After a new condition is selected on **NORM** / **$\overline{\text{MODE}}$**, the power must be cycled to enable it.

5.1. ADDRESS TRIGGER (NORM) OPERATION

The start address bits (**S0**, **S1**, **S2** & **S3**) and end address bits (**E0**, **E1**, **E2** & **E3**) are used to access the memory location and they can divide the memory into a maximum of 16 slots. As an example of I14B20, they are defined as follows:

S3 (E3)	S2 (E2)	S1 (E1)	S0 (E0)	Row #	14B20 Duration [s]
0	0	0	0	0	0
0	0	0	1	8	1.25
0	0	1	0	16	2.50
0	0	1	1	24	3.75
0	1	0	0	32	5.00
0	1	0	1	40	6.25
0	1	1	0	48	7.50
0	1	1	1	56	8.75
1	0	0	0	64	10.00
1	0	0	1	72	11.25
1	0	1	0	80	12.50
1	0	1	1	88	13.75
1	1	0	0	96	15.00
1	1	0	1	104	16.25
1	1	1	0	112	17.50
1	1	1	1	120	18.75

5.1.1. Record ($\overline{\text{REC}}$) Operation

- Low active input, level-hold for level-trigger or falling edge for edge-trigger with debounce required.
- For 8kHz sampling frequency, if **$\overline{\text{REC}}$** is held at Low for a period equal to 1 sec or more, then level recording is activated. However, if **$\overline{\text{REC}}$** is pulsed Low for less than 1 sec, then edge-trigger recording is initiated.
- For 6.4kHz sampling frequency, if **$\overline{\text{REC}}$** is held at Low for a period equal to 1.25 sec or more, then level recording is activated. However, if **$\overline{\text{REC}}$** is pulsed Low for less than 1.25 sec, then edge-trigger recording is initiated.
- Recording begins from the start address to end address and **$\overline{\text{LED}}$** is on.
- Recording ceases whenever **$\overline{\text{REC}}$** returns to High in level-hold mode or a subsequent lower going pulse appears while in edge-trigger mode or when end address is reached. Then an EOM marker is written at the end of message. And **$\overline{\text{LED}}$** is off.
- Then the device will automatically power down.
- This pin has an internal pull-up device.
- Once **$\overline{\text{REC}}$** is active, input on **$\overline{\text{FT}}$**, **NORM** / **$\overline{\text{MODE}}$**, **S0**, **S1**, **S2**, **S3**, **E0**, **E1**, **E2** or **E3** is illegal.

Fig. 1: Record–Level (**$\overline{\text{REC}}$**) function till end address

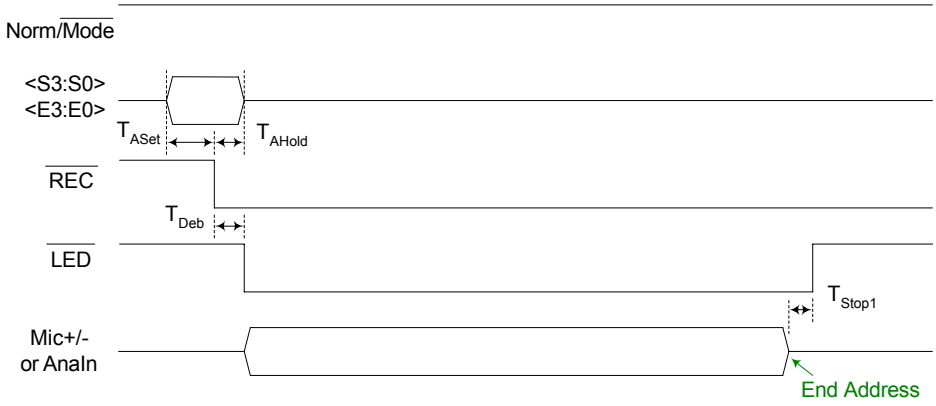


Fig. 2: Record–Level (**$\overline{\text{REC}}$**) function with start and stop actions

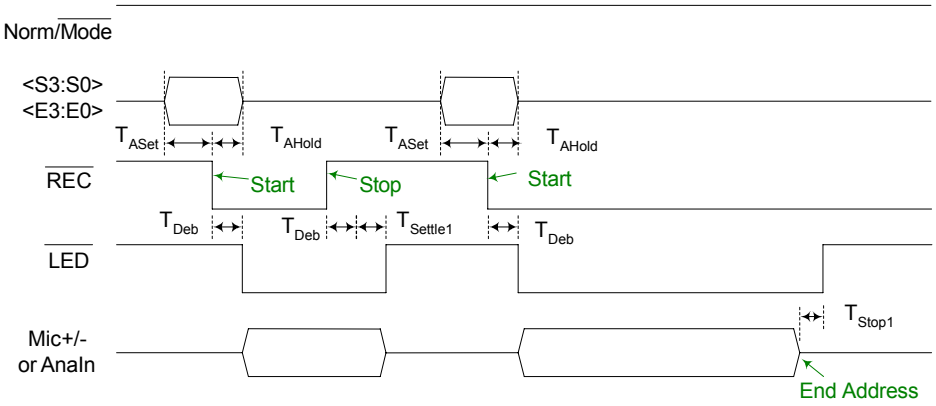
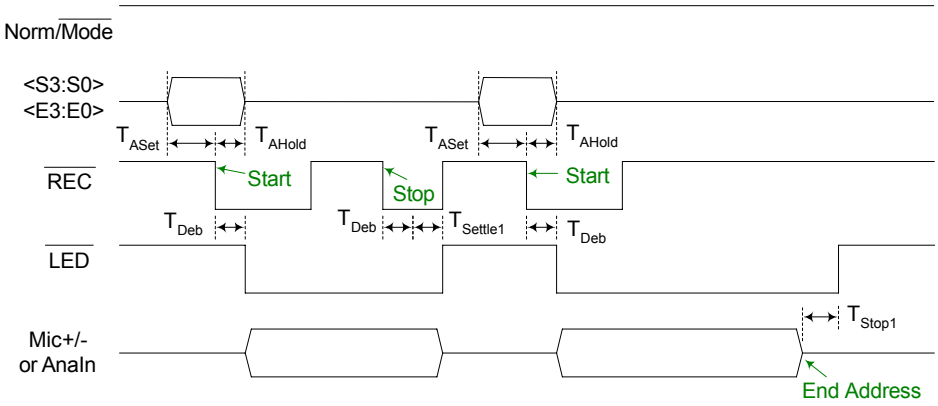


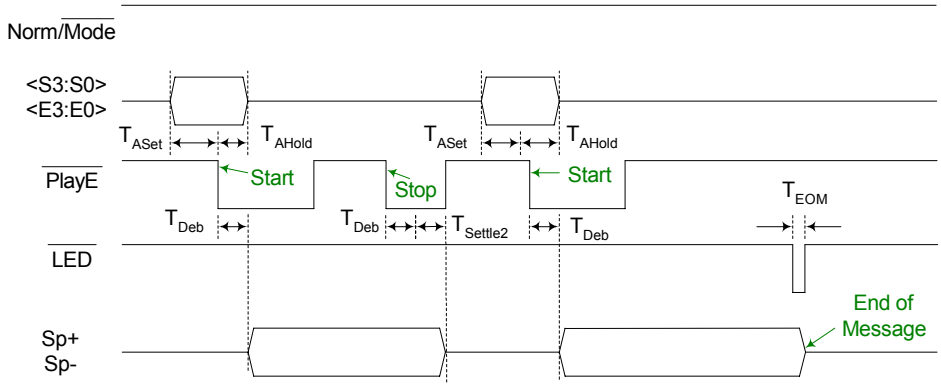
Fig. 3: Record–Edge (**$\overline{\text{REC}}$**) function with on-off



5.1.2. Edge-triggered Playback ($\overline{\text{PlayE}}$) Operation

- Low active input, edge-trigger, toggle on-off, debounce required.
- Playback begins from the start address to end address or EOM, whichever is occurred first.
- At the end of message, $\overline{\text{LED}}$ pulses Low momentarily.
- Then device will automatically power down.
- During playback, a subsequent trigger terminates the playback operation. If EOM marker is not encountered, then $\overline{\text{LED}}$ will not pulses Low momentarily.
- This pin has an internal pull-up device.
- Once $\overline{\text{PlayE}}$ is active, input on $\overline{\text{PlayL}}$, $\overline{\text{REC}}$, $\overline{\text{FT}}$, NORM / $\overline{\text{MODE}}$, S0, S1, S2, S3, E0, E1, E2 or E3 is banned.

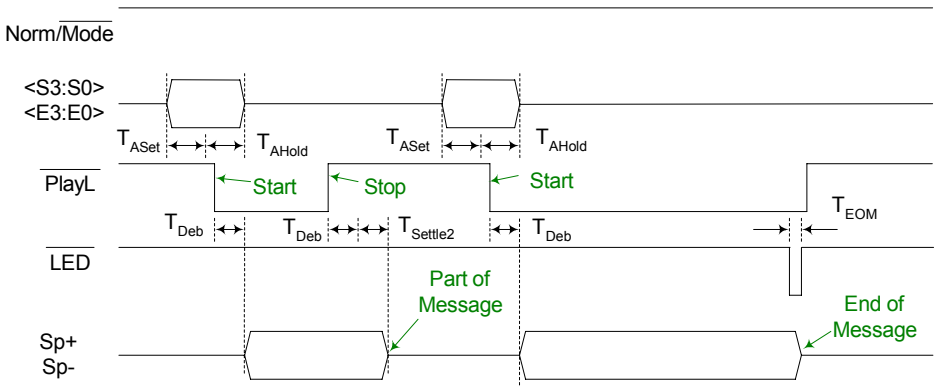
Fig. 4 : Playback–Edge ($\overline{\text{PlayE}}$) function



5.1.3. Level- triggered Playback ($\overline{\text{PlayL}}$)Operation

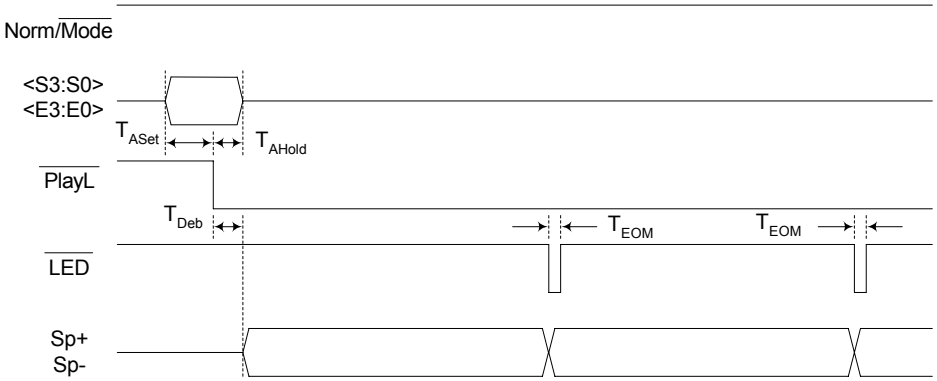
- Low active input, Level-hold, debounce required.
- Once active, playback begins from the start address and stops whenever $\overline{\text{PlayL}}$ returns to High. When an EOM is encountered, $\overline{\text{LED}}$ pulses Low momentarily.
- Then device will automatically power down.
- This pin has an internal pull-up device.
- Once $\overline{\text{PlayL}}$ is active, input on $\overline{\text{PlayE}}$, $\overline{\text{REC}}$, $\overline{\text{FT}}$, NORM / $\overline{\text{MODE}}$, S0, S1, S2, S3, E0, E1, E2 or E3 is prohibited.

Fig. 5: Playback–Level ($\overline{\text{PlayL}}$) function



- However, holding **PlayL** Low constantly will perform looping playback function, without power down, from start address to end address.

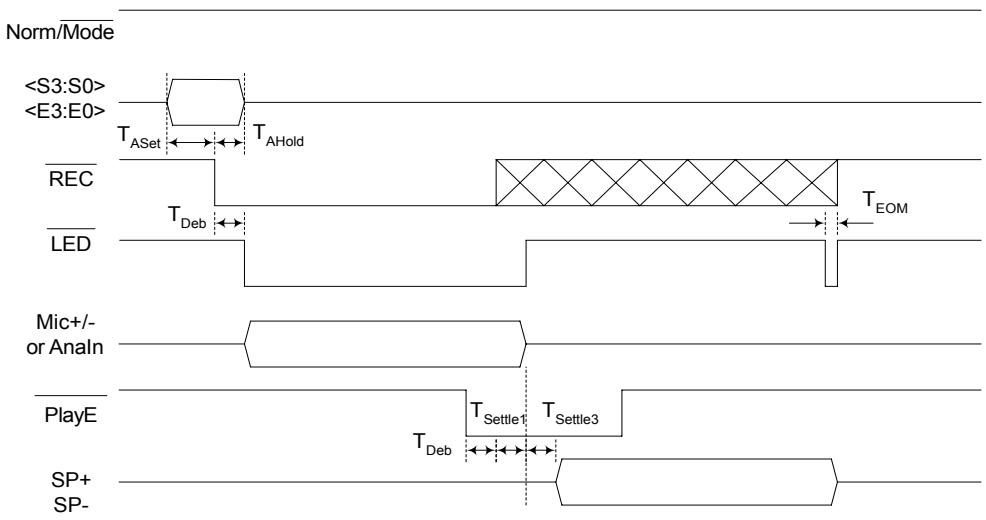
Fig. 6: Looping playback function via **PlayL**



5.1.4. Playback (Supersedes Record) Operation

- Playback takes precedence over the Recording operation.
- If either **PlayE** or **PlayL** is activated during a recording cycle, the recording immediately ceases with an EOM marker attached, and without power down, playback of the just-recorded message performs accordingly. Then device powers down.

Fig. 7: An example of Playback supersedes Record



5.1.5. XCLK Feature

- When precision sampling frequency is required, external clock mode can be activated by setting **XCLK** to Low. Under such condition, the resistor at Rosc pin must be removed and the external clock signal must be applied to the Rosc pin. These conditions must be satisfied prior to any operations.
- However, when internal clock is used, **XCLK** must be linked to High.
- The external clock frequencies required for various sampling frequencies are listed in below table.

Sampling Freq [kHz]	12	8	6.4	5.3	4
XCLK [MHz]	3.072	2.048	1.638	1.356	1.024

5.2. DIRECT TRIGGER (MODE) OPERATION

- The direct trigger is selected by the **MODE** pin. Once chosen, the supply voltage must be reset to allow the device to construct itself to the appropriate configuration by re-defining the function on the related control pins. Also, the mode change is only allowed while the device is in power down state and inhibited during an operation is in progress.
- Once direct trigger is activated, **FMC1**, **FMC2** & **FMC3** are utilized to select various (1 to 8) fixed message configurations [1]. Pending upon the arrangement on **FMC1**, **FMC2** & **FMC3**, each divided message has approximate equal length of duration, which is related to the number of rows assigned as in below table.
- The record or playback operation is pre-defined by the **R/P** pin. Setting this pin to Low allows record operation while setting it to High enables playback operation.
- Each message can be randomly accessed via its message control pin (**M1**~**M8**) and the desired operations are facilitated accordingly. Non-configured pins are automatically disabled and must be floated.

Notes: [1] : Number of fixed message arrangement with respect to **FMC1**, **FMC2** & **FMC3**.

FMC3	FMC2	FMC1	# of fixed messages [1]
0	0	0	1
0	0	1	2
0	1	0	3

0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

[2] : Number of memory **row arrangement** with respect to different number of fixed messages for ISD14B20 (128 Rows). The non-configured Message control pins (Mx) will be disabled.

# of Msg	M1	M2	M3	M4	M5	M6	M7	M8
1	128							
2	64	64						
3	44	42	42					
4	32	32	32	32				
5	26	26	26	26	24			
6	23	21	21	21	21	21		
7	20	18	18	18	18	18	18	
8	16	16	16	16	16	16	16	16

[3] : The **durations** for various fixed message configurations on I14B20 device at 8 kHz sampling frequency are shown in below table.

# of Msg	M1	M2	M3	M4	M5	M6	M7	M8
1	20							
2	10	10						
3	6.875	6.563	6.563					
4	5.0	5.0	5.0	5.0				
5	4.063	4.063	4.063	4.063	3.750			
6	3.594	3.281	3.281	3.281	3.281	3.281		
7	3.125	2.813	2.813	2.813	2.813	2.813	2.813	
8	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

Example of four Fixed-Message Configuration:

Fig. 8: Record Operation under FMC mode

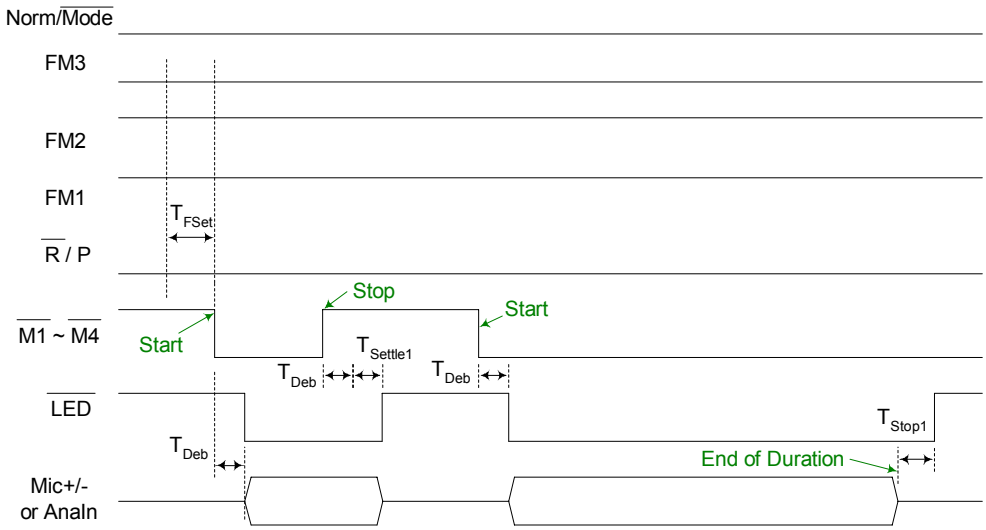
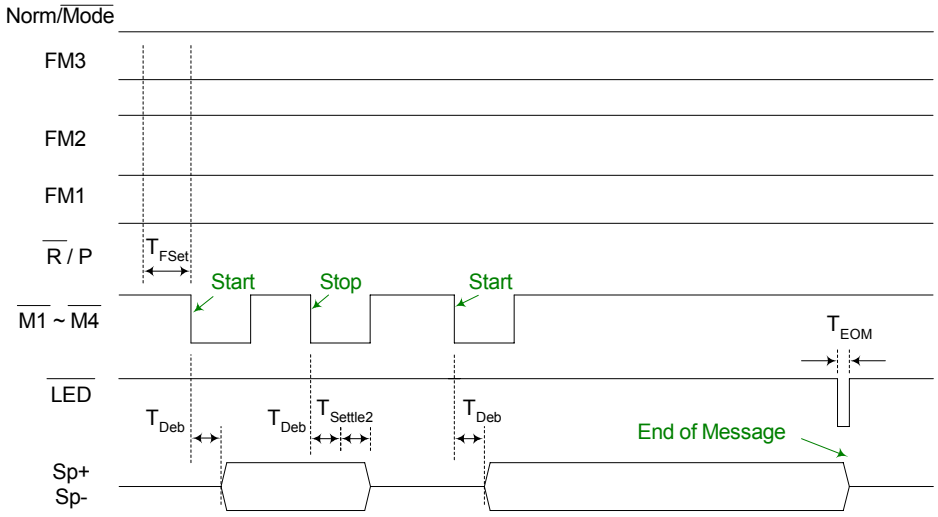


Fig. 9: Playback Operation under FMC mode



5.3. OTHER OPERATIONS

5.3.1. Rosc Operation

- When the R_{OSC} varies from 53.3 KΩ to 160 KΩ, the sampling frequency changes from 12 to 4 kHz accordingly.

- When R_{OSC} resistor value is changed during playback, the tone of a recorded message will alter either faster or slower.
- If the ground side of R_{OSC} resistor is floated or tied to V_{CC}, then the current operation will be freezed.
- The operation will resume when the resistor is connected back to ground.

5.3.2. $\overline{\text{LED}}$ Operation

- $\overline{\text{LED}}$ turns on during recording. Also, $\overline{\text{LED}}$ pulses Low at the end of message. The Low period must be sufficiently greater than debounce time.

5.3.3. Feed-Through mode Operation

- As $\overline{\text{FT}}$ is held Low, the Mic+ pin will be reconfigured as AnaIn input then the AnaIn signal will be transmitted to the speaker outputs. Under this mode, Mic- pin is not used (must be floated).
- After $\overline{\text{FT}}$ is enabled, If $\overline{\text{REC}}$ is triggered, then AnaIn signal will be recorded into memory while the Feed-Through path remains on.
- If $\overline{\text{FT}}$ is already enabled, activating either $\overline{\text{PlayE}}$ or $\overline{\text{PlayL}}$ will first disable the FT path then play the recorded message. Once playback completes, FT path will be resumed.
- During an operation, activating the $\overline{\text{FT}}$ pin is not allowed.

5.3.4. Power-On Playback Operation

- If $\overline{\text{PlayE}}$ is kept at Low during power turns on, the device plays message once, then powers down.
- If $\overline{\text{PlayL}}$ is held at Low during power turns on and constantly maintained at Low, the device will play the message repeatedly, with insignificant dead time between messages regardless of sampling frequencies. This status will sustain unless power is turned off or $\overline{\text{PlayL}}$ somehow returns to High.

5.3.5. Automatic Single Message Playback

- If $\overline{\text{LED}}$ is connected to $\overline{\text{PlayE}}$, once $\overline{\text{PlayE}}$ is triggered, then the device plays message repeatedly without power down between the looping playback. However, if $\overline{\text{PlayE}}$ is triggered again during playback, then playback will stop.

5.3.6. Power is interrupted Abruptly

- During the device is in operation, it is strongly recommended that the supply power cannot be interrupted. Otherwise, it may cause the device to become malfunctioning.

6. ABSOLUTE MAXIMUM RATINGS [1]

ABSOLUTE MAXIMUM RATINGS

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pins	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to Input pins (current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Voltage applied to output pins (current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
V_{CC} – V_{SS}	-0.3V to +7.0V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS

CONDITION	VALUE
Operating temperature range	0°C to +50°C
Operating voltage (V_{CC}) [1]	+2.4V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

7. ELECTRICAL CHARACTERISTICS

7.1. DC PARAMETERS

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.3xVcc	V	
Input High Voltage	V_{IH}	0.7xVcc			V	
Output Low Voltage	V_{OL}			0.3xVcc	V	I_{OL} = 4.0 mA[3]
Output High Voltage	V_{OH}	0.7xVcc			V	I_{OH} = -1.6 mA[3]
Standby Current	I_{STBY}		1	10	µA	[4] [5]
Record Current	I_{REC}		20	30	mA	V_{CC} = 5.5V [4] [5]
Playback Current	I_{PLAY}		20	30	mA	V_{CC} = 5.5V, no load [4] [5]
Pull-up device for **REC**, **PlayE**, **PlayL**, **FT** & **M1**~**M8** pins	R_{PU1}		600		kΩ	
MIC+ Input Resistance	R_{MICP}		18		KΩ	
MIC- Input Resistance	R_{MICN}		18		KΩ	
AnaIn Input Resistance	R_{ANAIN}		42		KΩ	
MIC Differential Input	V_{IN1}	15		300	mV	Peak-to-peak
AnaIn Input	V_{IN2}			1	V	Peak-to-peak
Gain from MIC to SP+/-	A_{MSP}		6~40		dB	V_{IN} = 15~300 mVp-p, AGC = 4.7 µF, V_{CC} = 2.4V~5.5V
Output Load Impedance	R_{SPK}	8			Ω	Speaker load
Speaker Output Power	Pout		313		mW	V_{DD} = 4.4 V 1Vp-p, 1 kHz sine wave at AnaIn. R_{SPK} = 8 Ω
Speaker Output Voltage	V_{OUT1}		V_{DD}		V	R_{SPK} = 8Ω Speaker, Typical buzzer

Notes: [1] Typical values @ V_{CC} = 5.5V, T_A = 25° and sampling frequency (Fs) at 8 kHz, unless stated.

[2] Not all specifications are 100 percent tested. All Min/Max limits are guaranteed by Winbond via design, electrical testing and/or characterization.

[3] LED output during recording.

[4] V_{CCA}, V_{CCD} and V_{CCP} are connected together. Also, V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} are linked together.

[5] All required control pins must be at appropriate status. External components are biased under a separated power supply.

7.2. AC PARAMETERS

CHARACTERISTIC [1]	SYMBOL	MIN[2]	TYP	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	Fs	4		12	kHz	[3]
Record Duration	T_{REC}	10.6		32	sec	[3]
Playback Duration	T_{PLAY}	10.6		32	sec	[3]
Debounce Time	T_{Deb}	225k/Fs			msec	[3] [4]
Address Setup Time	T_{ASet}	30			nsec	
Address Hold Time	T_{AHold}	225k/Fs			msec	[3] [4]
FMC Setup Time	T_{FSet}	30			nsec	
Record Settle Time	$T_{Settle1}$		32k/Fs		msec	[3] [4]
Play Settle Time	$T_{Settle2}$		256k/Fs		msec	[3] [4]
Delay from Record to Play	$T_{Settle3}$		128k/Fs		msec	[3] [4]
Record Stop Time	T_{Stop1}	30			nsec	
LED Pulse Low Time	T_{EOM}		256k/Fs		msec	[3] [4]

Notes:

[1] Conditions are V_{CC} = 5.5V, T_A = 25°C and sampling frequency (F_S) at 8kHz, unless specified.

[2] Not all specifications are 100 percent tested. All Min/Max limits are guaranteed by Winbond via design, electrical testing and/or characterization.

[3] When different F_S is applied, the value will change accordingly. Also, stability of internal oscillator may vary as much as ±10% over the operating temperature and voltage ranges.

[4] k = 1000.

8.

8. TYPICAL APPLICATION CIRCUIT

The following typical application examples on ISD14B20 series are for references only. They make no representation or warranty that such applications shall be suitable for the use specified. It's customer's obligation to verify the design in its own system for the functionalities, voice quality, current consumption, and etc.

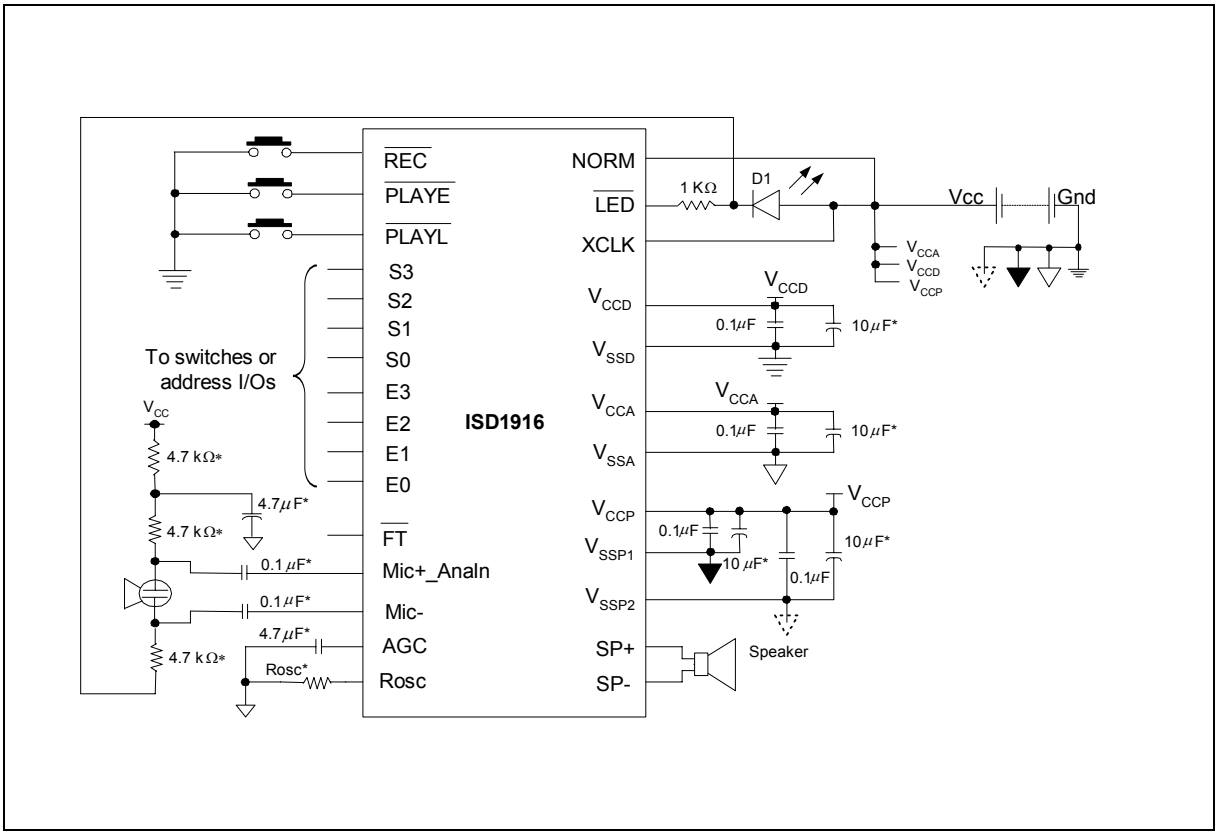
In addition, the below notes apply to the following application examples:

* The suggested values are for references only. Depending on system requirements, they can be adjusted for functionalities, voice quality and degree of performance.

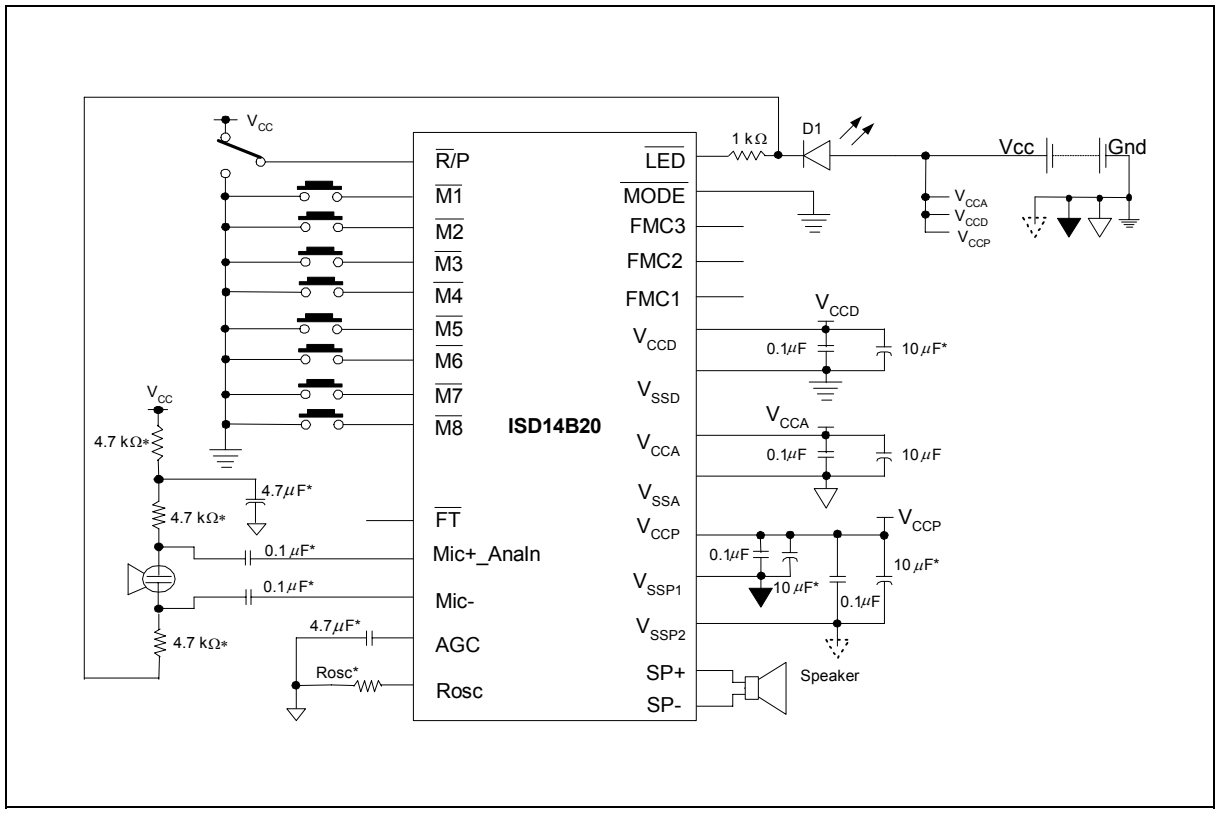
It is important to have a separate path for each ground and power back to the related terminals to minimize the noise. Besides, the power supplies should be decoupled as close to the device as possible.

Also, it is crucial to follow good audio design practices in layout and power supply decoupling. See recommendations in Application Notes from our websites.

Example #1: Operations via start and end addresses under address trigger mode (**NORM**)



Example #2: Fixed Message Configuration Operations under direct trigger mode (**MODE**)



Good Audio Design Practices

Winbond's ChipCorder are very high-quality single-chip voice recording and playback devices. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling are followed. See Application Information links below for details.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

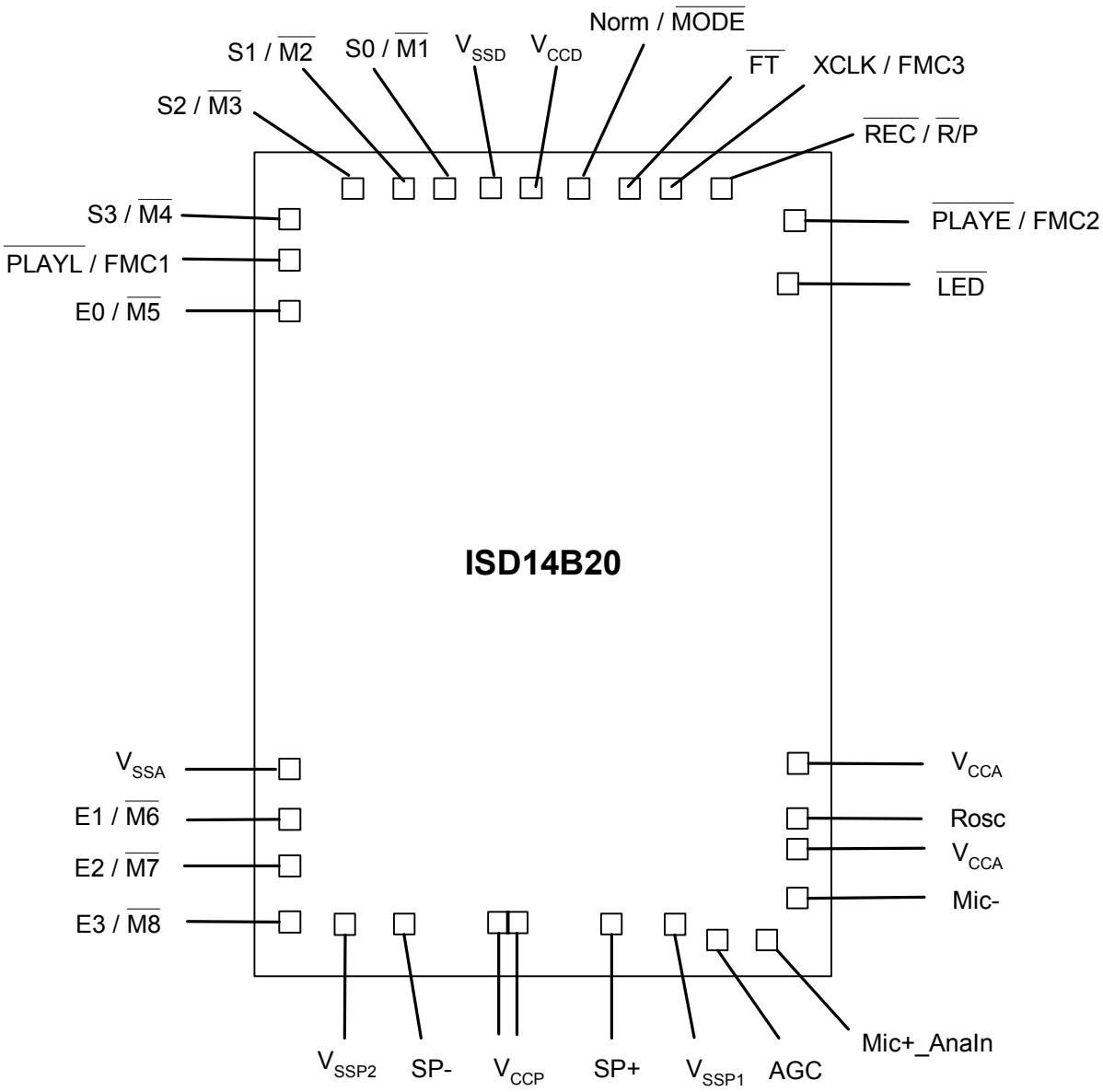
Single-Chip Board Layout Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

It is strongly recommended that before any design or layout project starts, the designer should contact Winbond Sales Rep for the most update technical information and layout advice.

9. PACKAGING

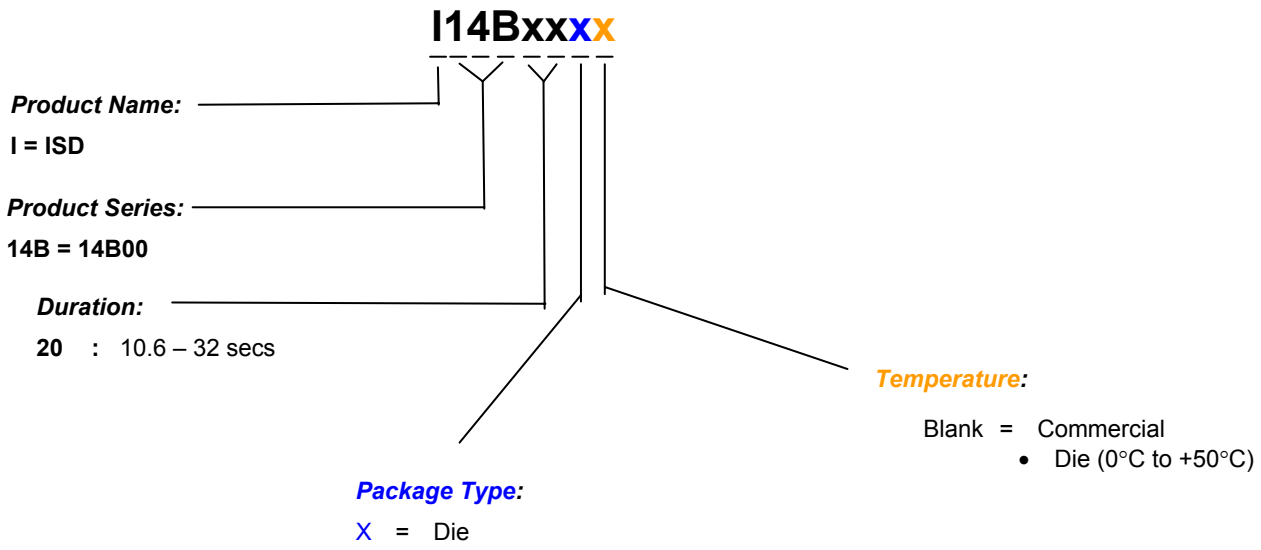
9.1 DIE INFORMATION



Contact Winbond Sales Representatives for other information.

10. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD14B20 devices, please refer to the above ordering scheme. Contact the local Winbond Sales Representatives for any questions and the availability.

For the latest product information, please contact the Winbond Sales/Rep or access Winbond's worldwide web site at http://www.winbond-usa.com

11. VERSION HISTORY

VERSION	DATE	DESCRIPTION
0	Oct 9, 2007	Initial revision

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Winbond makes no representation or warranty that such applications shall be suitable for the use specified.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Winbond Reliability Report, and are neither warranted nor guaranteed by Winbond. This product incorporates SuperFlash®.

Information contained in this ISD® ChipCorder® datasheet supersedes all data for the ISD ChipCorder products published by ISD® prior to August, 1998.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.