



# STV160NF03L

## N-CHANNEL 30V - 0.0019Ω - 160A PowerSO-10 STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STV160NF03L	30 V	< 0.0028 Ω	160 A

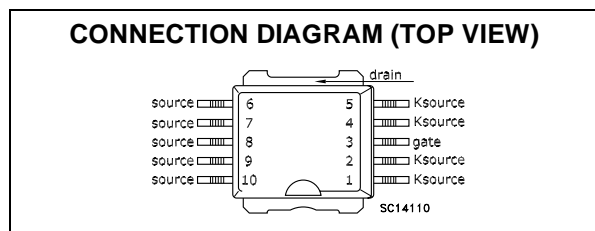
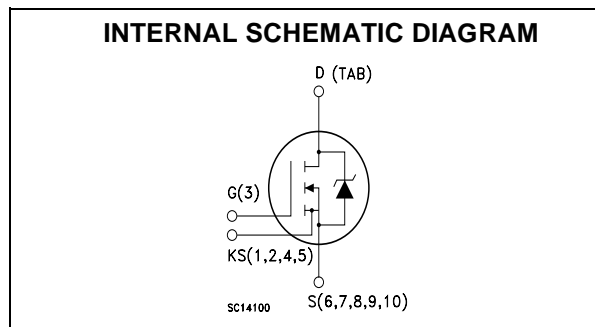
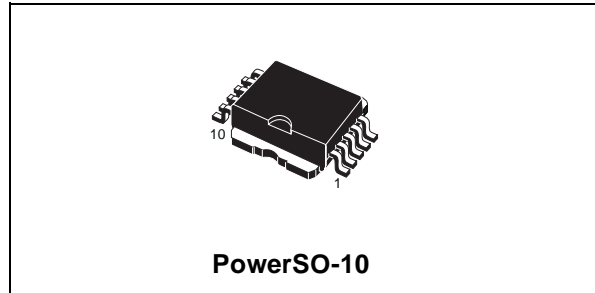
- TYPICAL R<sub>DS(on)</sub> = 0.0019 Ω
- LOW THRESHOLD DRIVE
- ULTRA LOW ON-RESISTANCE
- ULTRA FAST SWITCHING
- 100% AVALANCHE TESTED
- VERY LOW GATE CHARGE
- LOW PROFILE, VERY LOW PARASITIC INDUCTANCE PowerSO-10 PACKAGE

### DESCRIPTION

The **STV160NF03L** represents the second generation of Application Specific STMicroelectronics well established STripFET™ process based on a very unique strip layout design. The resulting MOSFET shows unrivalled high packing density with ultra low on-resistance and superior switching characteristics. Process simplification also translates into improved manufacturing reproducibility. This device is particularly suitable for high current, low voltage switching application where efficiency is crucial

### APPLICATIONS

- BUCK CONVERTERS IN HIGH PERFORMANCE TELECOM AND VRMs DC-DC CONVERTERS



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate- source Voltage	± 15	V
I <sub>D</sub> (**)	Drain Current (continuous) at T <sub>C</sub> = 25°C	160	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	113	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	640	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	210	W
	Derating Factor	1.4	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	1	J
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Starting T<sub>j</sub>=25°C, I<sub>D</sub> = 80A, V<sub>DD</sub> = 20V

(\*\*) Limited only maximum junction temperature allowed by PowerSO-10

## STV160NF03L

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.71	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 15 V			±100	nA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 45 A V <sub>GS</sub> = 8 V, I <sub>D</sub> = 80 A V <sub>GS</sub> = 5 V, I <sub>D</sub> = 40 A V <sub>GS</sub> = 10 V, I <sub>D</sub> =80 A; T <sub>J</sub> = 175 °C V <sub>GS</sub> = 8 V, I <sub>D</sub> =80 A; T <sub>J</sub> = 175 °C V <sub>GS</sub> = 5 V, I <sub>D</sub> =40 A; T <sub>J</sub> = 175 °C		1.9 1.86 2 4	2.8 2.8 3.8 6.7 6.4 7.8 12.8	mΩ mΩ mΩ mΩ mΩ mΩ mΩ
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10V	160			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 80 A		210		S
R <sub>g</sub>	Gate resistance	V <sub>DS</sub> = 0 V, f = 1 MHz, V <sub>GS</sub> = 0		0.5		Ω
C <sub>iSS</sub> C <sub>oSS</sub> C <sub>rSS</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		4700 1580 240		pF pF pF
C <sub>iSS</sub> C <sub>oSS</sub> C <sub>rSS</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 0 V, f = 1 MHz, V <sub>GS</sub> = 0		6500 9500 4000		pF pF pF
L <sub>S</sub>	Internal Source Inductance	From the Lead End (6mm from Package Body) to the Die Center		4		nH
L <sub>D</sub>	Internal Drain Inductance		Not Available on Surface Mounting Package			

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 80\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		30		ns
$t_r$	Rise Time			380		ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ , $I_D = 160\text{ A}$ , $V_{GS} = 10\text{ V}$		103	140	nC
$Q_{gs}$	Gate-Source Charge			21		nC
$Q_{gd}$	Gate-Drain Charge			38		nC

**SWITCHING OFF**

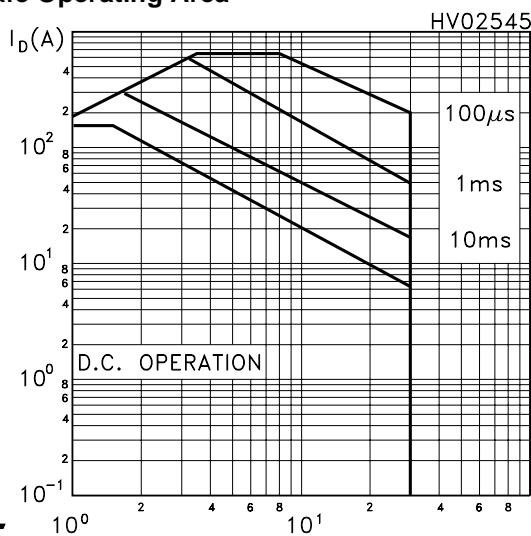
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 80\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		80		ns
$t_f$	Fall Time			170		ns
$t_{d(off)}$	Turn-off Delay Time	$V_{clamp} = 24\text{ V}$ , $I_D = 40\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$		75		ns
$t_{r(Voff)}$	Off-voltage Rise Time			25		ns
$t_f$	Fall Time			90		ns
$t_c$	Cross-over Time			125		ns

**SOURCE DRAIN DIODE**

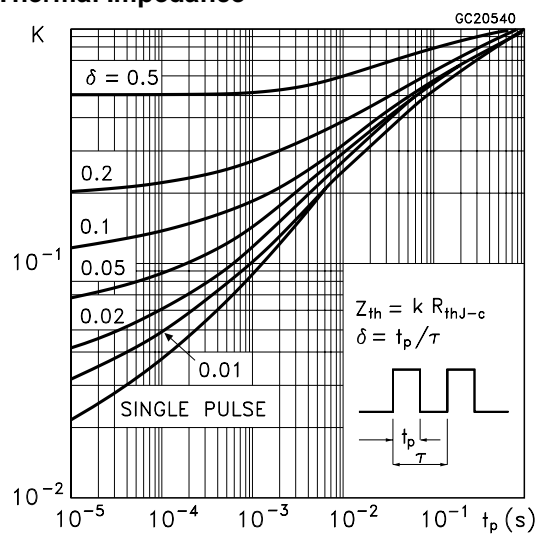
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				160	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				640	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 160\text{ A}$ , $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 80\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 15\text{ V}$ , $T_j = 25^\circ\text{C}$ (see test circuit, Figure 5)		80		ns
$Q_{rr}$	Reverse Recovery Charge			180		nC
$I_{RRM}$	Reverse Recovery Current			4.5		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

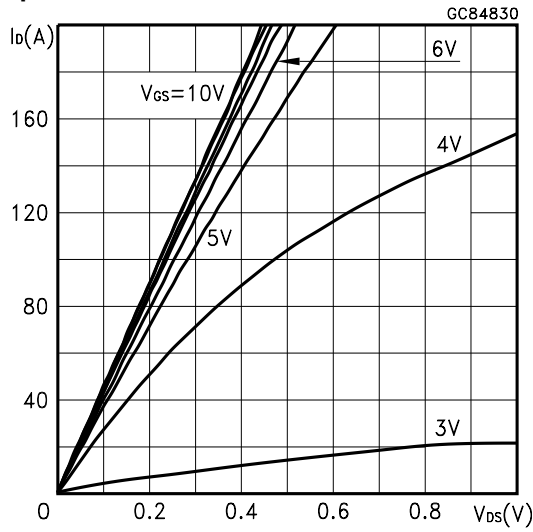
**Safe Operating Area**



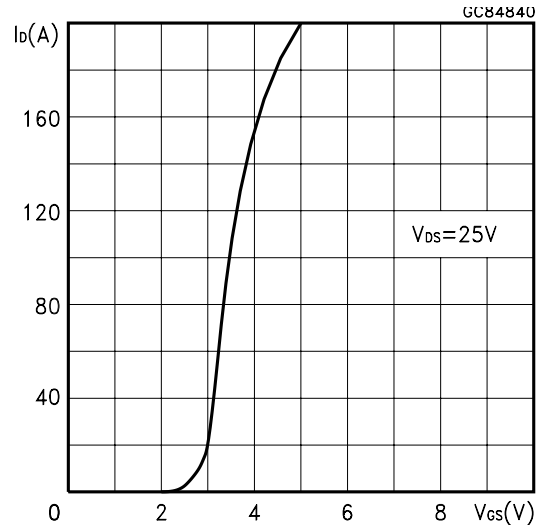
**Thermal Impedance**



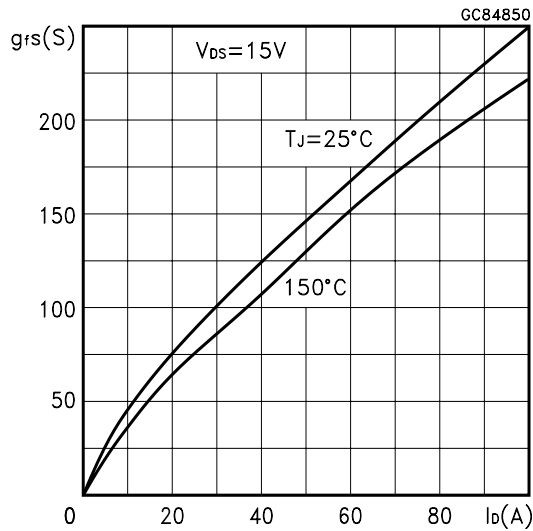
Output Characteristics



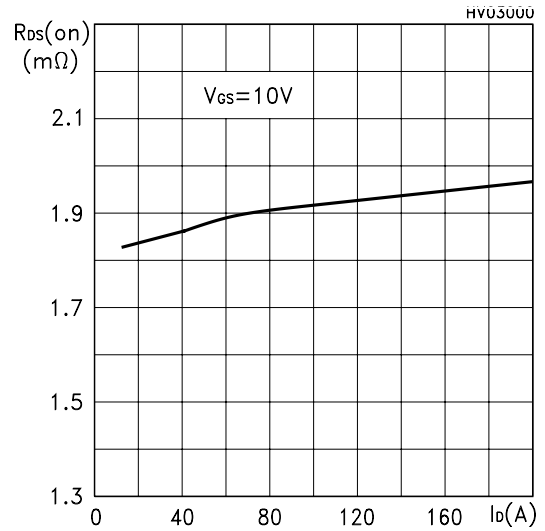
Transfer Characteristics



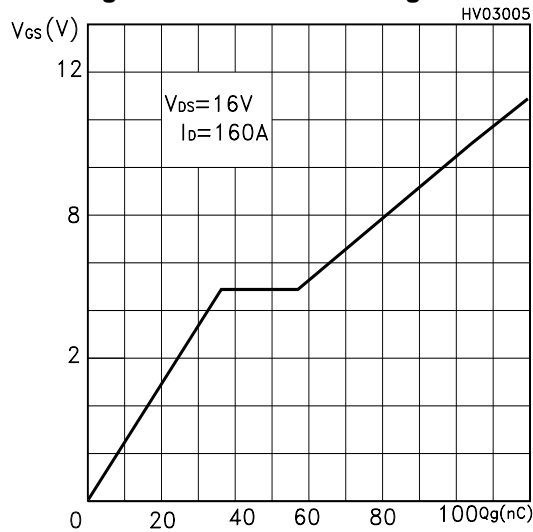
Transconductance



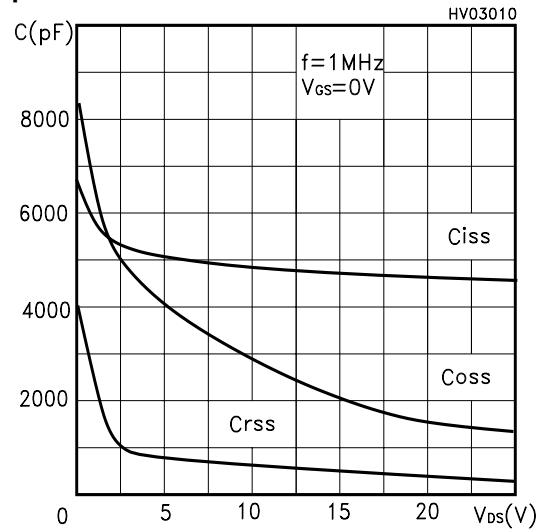
Static Drain-Source On Resistance



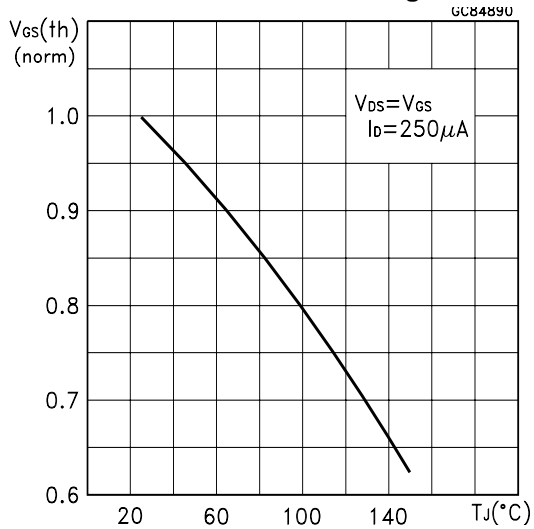
Gate Charge vs Gate-source Voltage



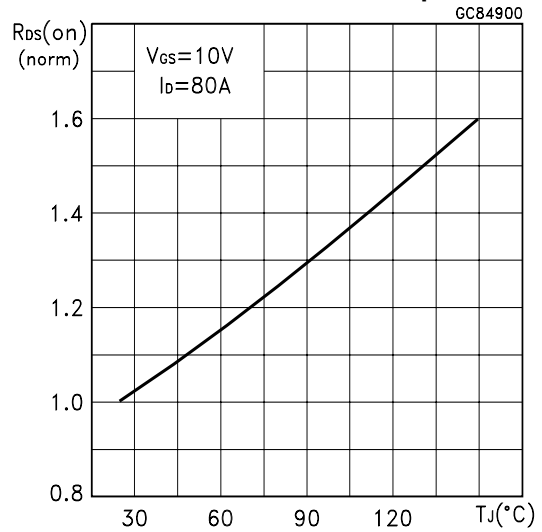
Capacitance Variations



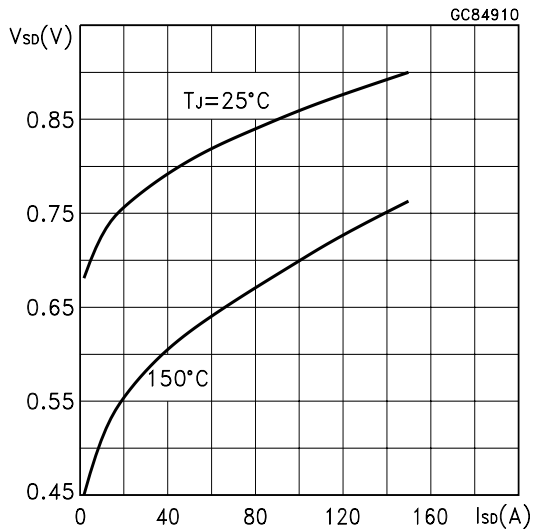
Normalized Gate Threshold Voltage vs Temp.



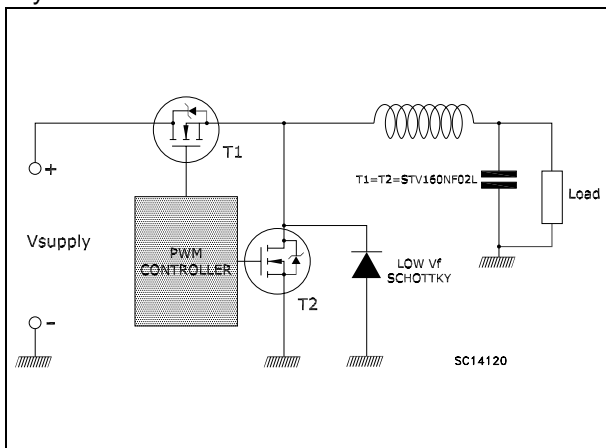
Normalized On Resistance vs Temperature



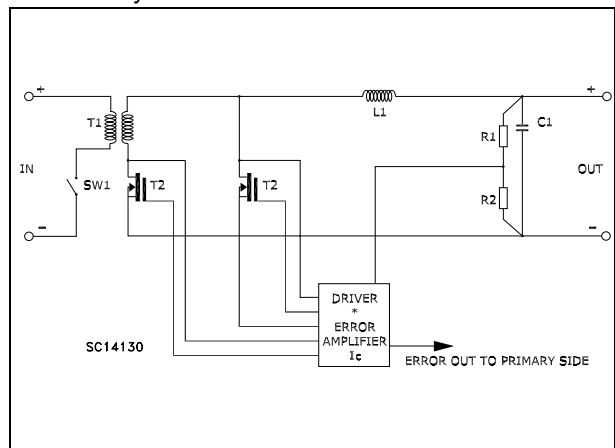
Source-drain Diode Forward Characteristics



Basic Schematic For Motherboard VRM With Synchronous Rectification

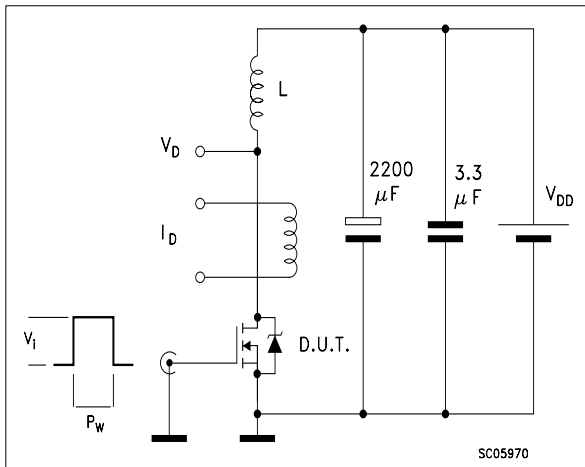


Basic Schematic Mosfets Switch Used In Secondary Side Of a Froward Convert

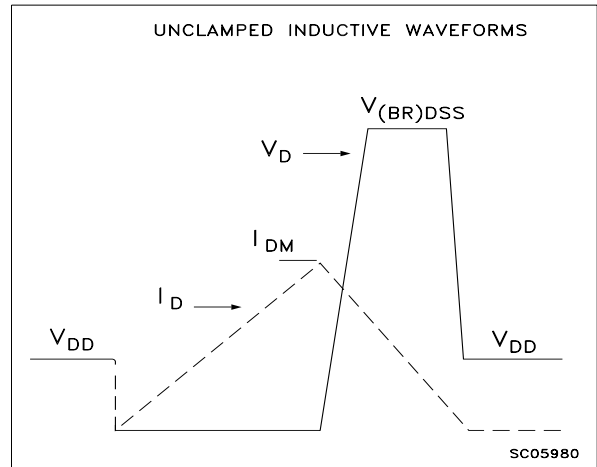




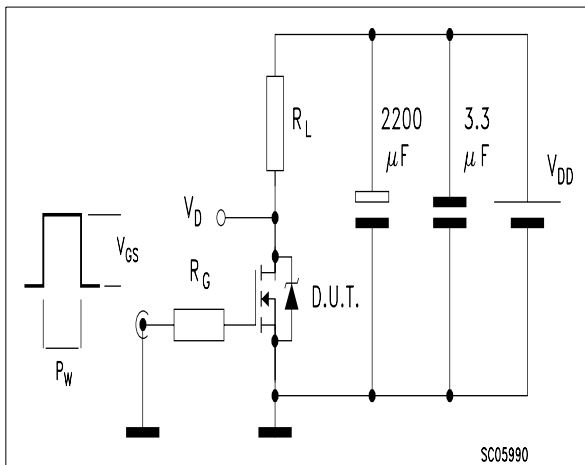
**Fig. 1: Unclamped Inductive Load Test Circuit**



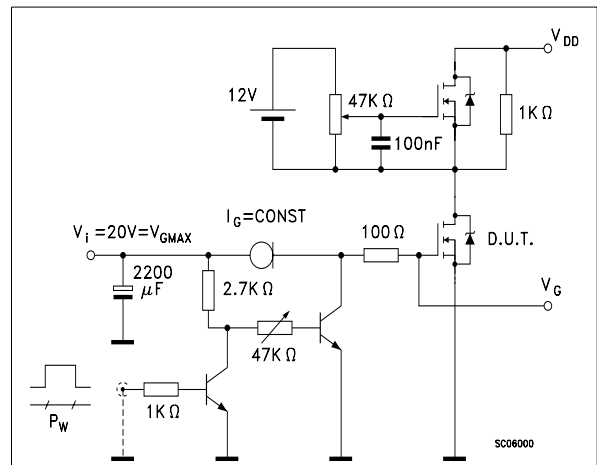
**Fig. 2: Unclamped Inductive Waveform**



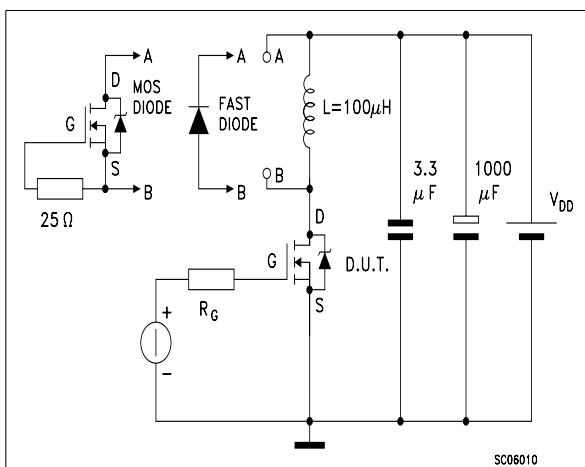
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

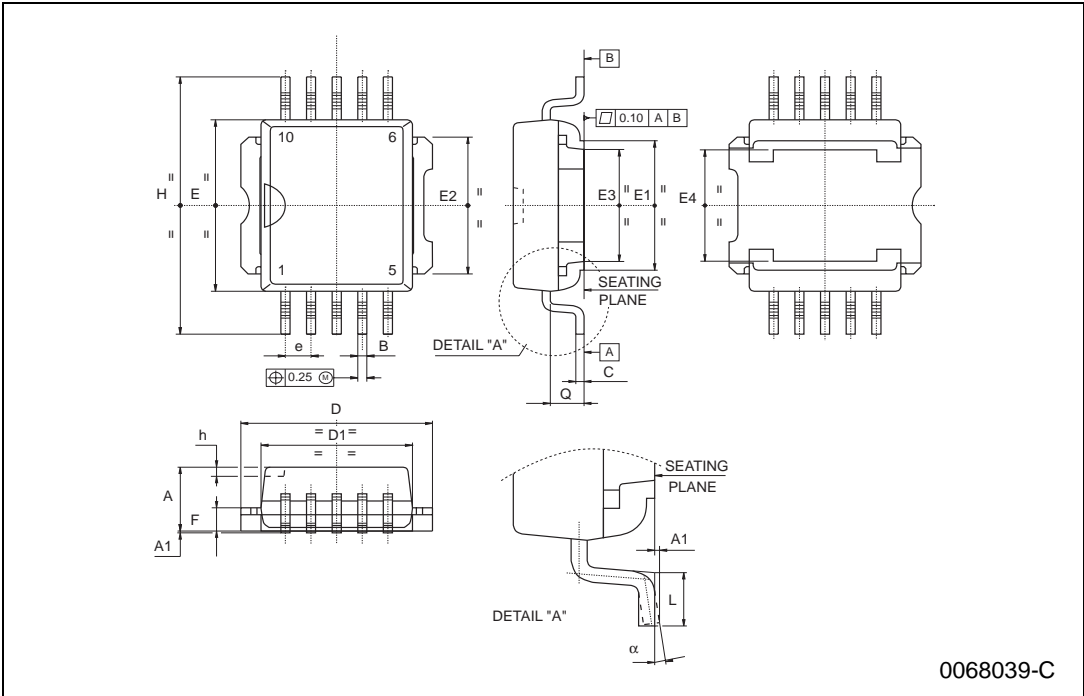


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**PowerSO-10 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
$\alpha$	0°		8°			





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