



STP80NS04ZB

N-CHANNEL CLAMPED 7.5mΩ - 80A TO-220 FULLY PROTECTED MESH OVERLAY™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP80NS04ZB	CLAMPED	<0.008 Ω	80 A

- TYPICAL R_{DS(on)} = 0.0075 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 °C MAXIMUM JUNCTION TEMPERATURE

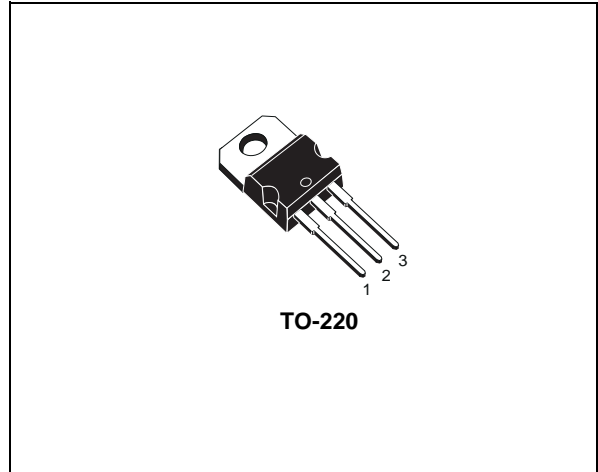
DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout.

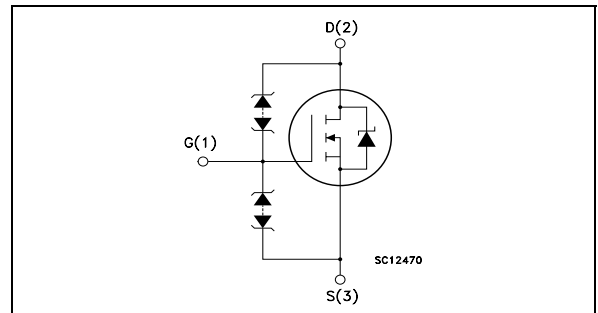
The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS, SOLENOID DRIVERS
- MOTOR CONTROL
- DC-DC CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	CLAMPED	V
V _{DG}	Drain-gate Voltage	CLAMPED	V
V _{GS}	Gate- source Voltage	CLAMPED	V
I _D	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	60	A
I _{DG}	Drain Gate Current (continuous)	± 50	mA
I _{GS}	Gate Source Current (continuous)	± 50	mA
I _{DM} (●)	Drain Current (pulsed)	320	A
P _{tot}	Total Dissipation at T _C = 25°C	200	W
	Derating Factor	1.33	W/°C
V _{ESD(G-S)}	Gate-Source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
V _{ESD(G-D)}	Gate-Drain ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
V _{ESD(D-S)}	Drain-source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	-40 to 175	°C

(●) Pulse width limited by safe operating area.

STP80NS04ZB

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.75	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	80	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 30 V)	500	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Clamped Voltage	I _D = 1 mA, V _{GS} = 0 -40 < T _J < 175 °C	33			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 16 V T _C =25 °C V _{DS} = 16 V T _J =150 °C V _{DS} = 16 V T _J =175 °C			10 50 100	μA μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 10 V T _J =175 °C V _{GS} = ± 16 V T _J =175 °C			50 150	μA μA
V _{GSS}	Gate-Source Breakdown Voltage	I _{GS} = 100 μA	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 1 mA -40 < T _J < 150 °C	1.7	3	4.2	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 40 A V _{GS} = 16 V I _D = 40 A		8 7.5	9 8	mΩ mΩ
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} , V _{GS} = 10V	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 40A	30	50		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2700	3300	pF
C _{oss}	Output Capacitance			1275	1600	pF
C _{rss}	Reverse Transfer Capacitance			285	350	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Q_g	Total Gate Charge	$V_{DD} = 20\text{ V}$ $I_D = 80\text{ A}$ $V_{GS} = 10\text{ V}$		80	105	nC
Q_{gs}	Gate-Source Charge			20		nC
Q_{gd}	Gate-Drain Charge			27		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 30\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (Inductive Load, Figure 5)		115	150	ns
t_f	Fall Time			80	105	ns
t_c	Cross-over Time			210	280	ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				320	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 80\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		90		ns
Q_{rr}	Reverse Recovery Charge			0.18		μC
I_{RRM}	Reverse Recovery Current			4		A

(\ast) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

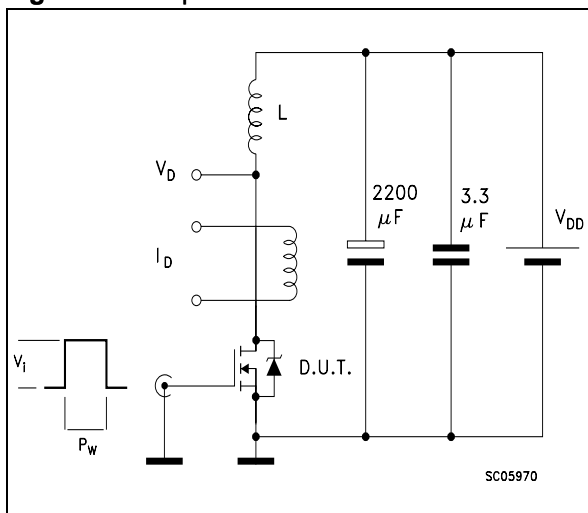


Fig. 2: Unclamped Inductive Waveform

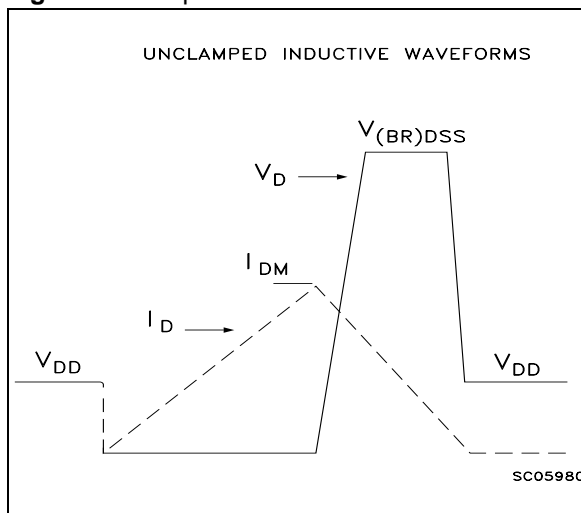


Fig. 3: Switching Times Test Circuits For Resistive Load

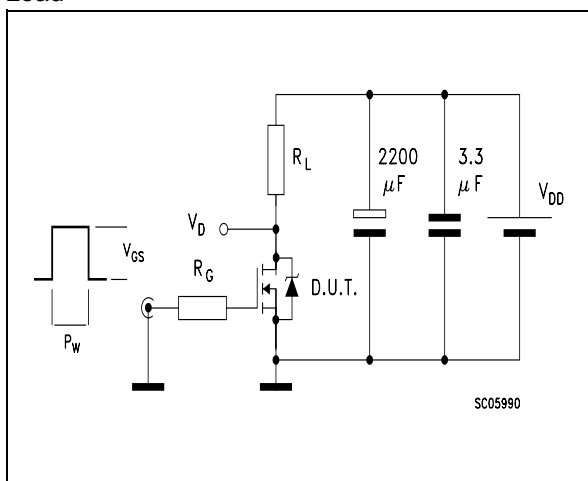


Fig. 4: Gate Charge test Circuit

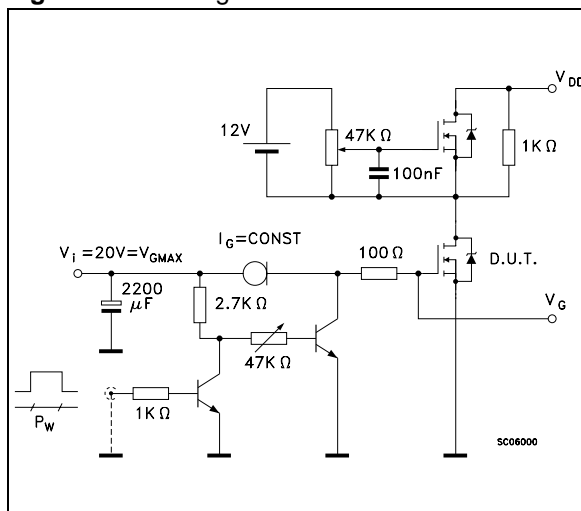
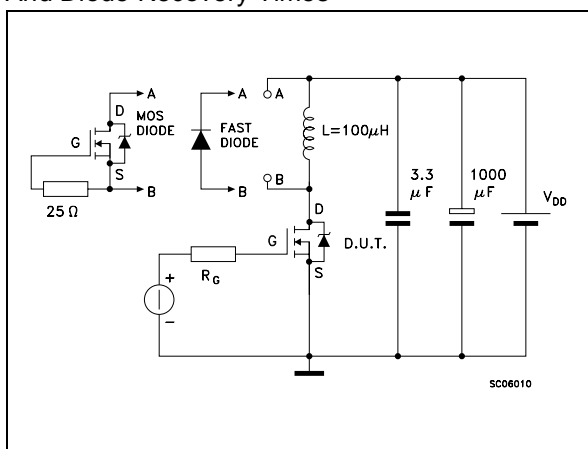
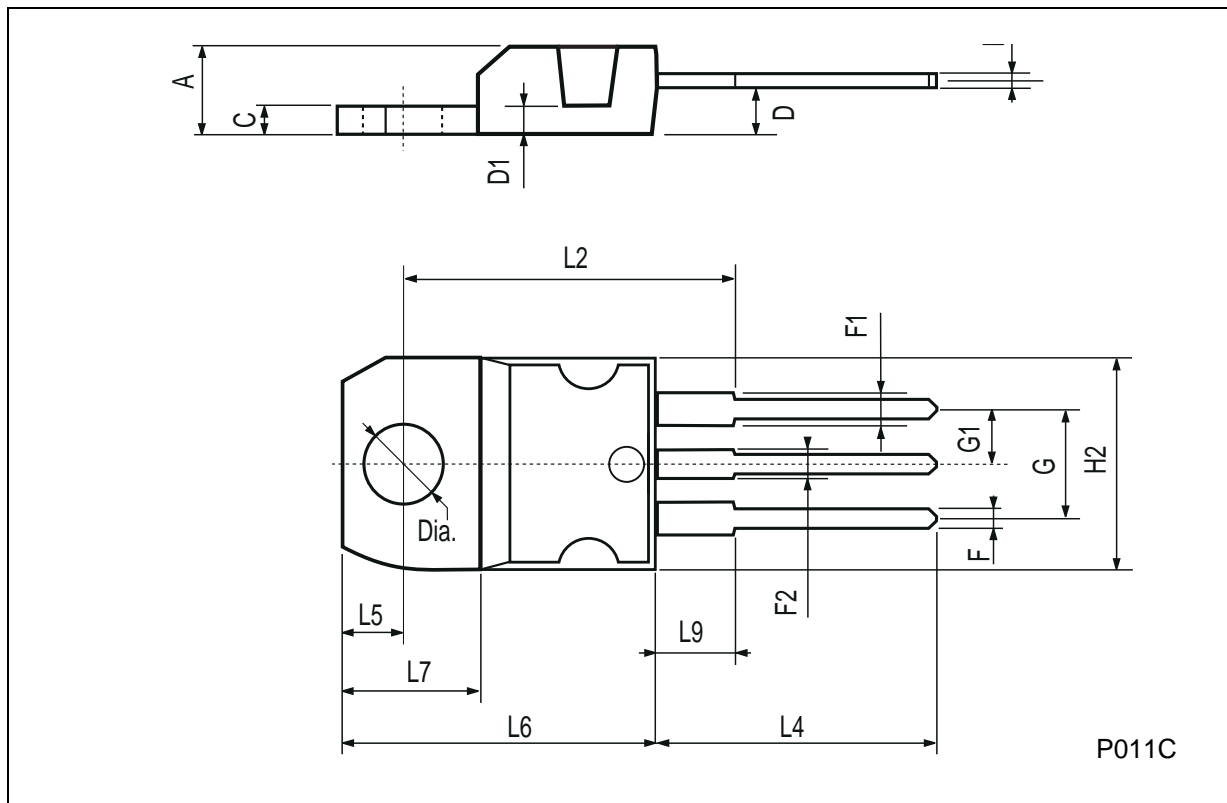


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
© 2003 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>