



## STP62NS04Z

N-channel clamped 12.5mΩ - 62A - TO-220  
Fully protected MESH OVERLAY™ Power MOSFET

### General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>
STP62NS04Z	Clamped	<0.015Ω	62A

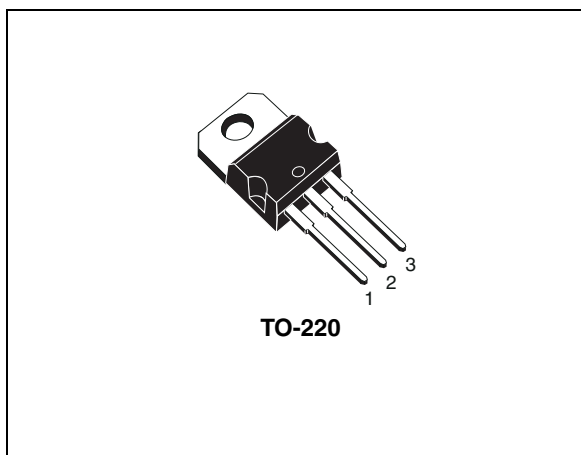
- 100% avalanche tested
- Low capacitance and gate charge
- 175° C maximum junction temperature

### Description

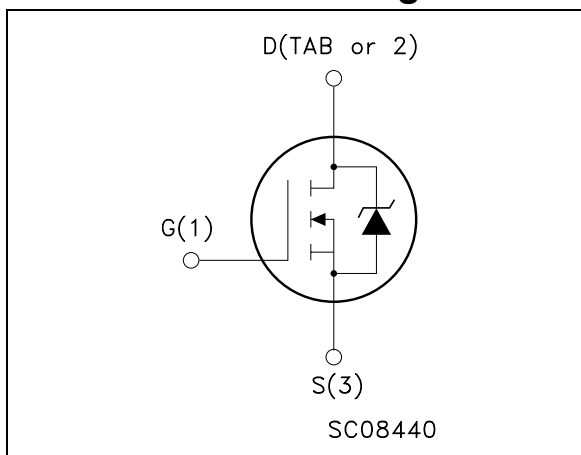
This fully clamped MOSFET is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STP62NS04Z	P62NS04Z	TO-220	Tube

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	Clamped	V
$V_{GS}$	Gate-source voltage	Clamped	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	62	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	37.5	A
$I_{DG}$	Drain gate current (continuous)	$\pm 50$	
$I_{GS}$	Gate source current (continuous)	$\pm 50$	
$I_{DM}^{(1)}$	Drain current (pulsed)	248	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.74	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	8	V/ns
$E_{AS}^{(3)}$	Single Pulse Avalanche Energy	500	mJ
$V_{ESD}$	ESD (HBM - C = 100pF, R = 1.5 k $\Omega$ )	8	V
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 40\text{A}$ ,  $di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$
3. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 20\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	1.36	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	33			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 16V$			10	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 10V$			10	$\mu A$
$V_{GSS}$	Gate-Source Breakdown Voltage	$I_{GS} = 100 \mu A$	18			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$		12.5	15	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 30A$		20		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$		1330		pF
$C_{oss}$	Output capacitance			420		pF
$C_{rss}$	Reverse transfer capacitance			135		pF
$Q_g$	Total gate charge	$V_{DD} = 20V, I_D = 40A, V_{GS} = 10V$		34	47	nC
$Q_{gs}$	Gate-source charge			10		nC
$Q_{gd}$	Gate-drain charge			11.5		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20V, I_D = 20A, R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		13		ns
$t_r$	Rise time			104		ns
$t_{d(off)}$	Turn-off delay time			41		ns
$t_f$	Fall time			42		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{clamp} = 30V, I_D = 40A, R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		30		ns
$t_f$	Fall time			54		ns
$t_c$	Cross-over time			90		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				62	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				248	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 62A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 40A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 20V, T_J = 150^\circ C$ <i>Figure 15 on page 8</i>		45		ns
$Q_{rr}$	Reverse recovery charge			65		$\mu C$
$I_{RRM}$	Reverse recovery current			2.9		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

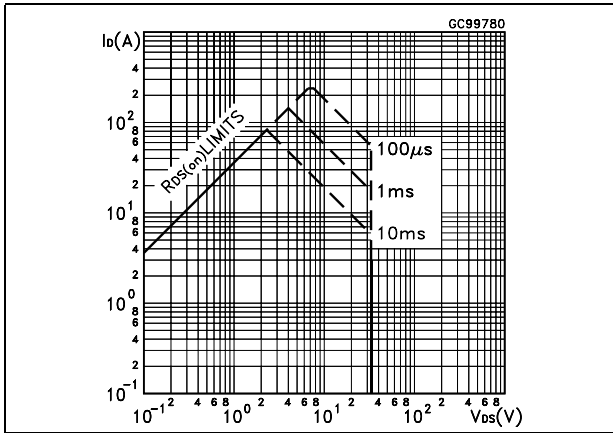


Figure 2. Thermal impedance

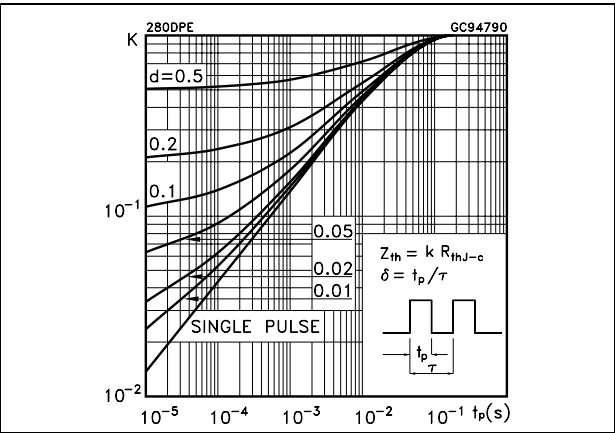


Figure 3. Output characteristics

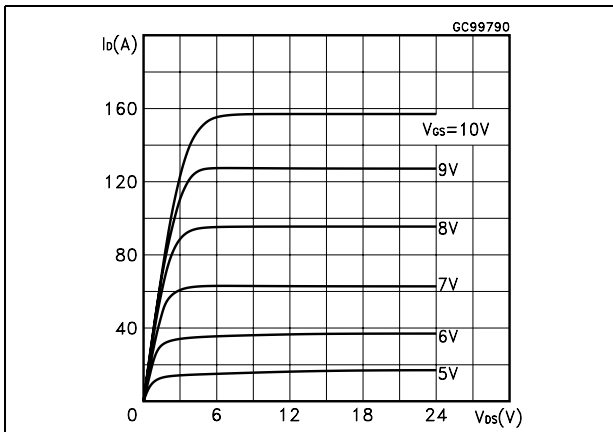


Figure 4. Transfer characteristics

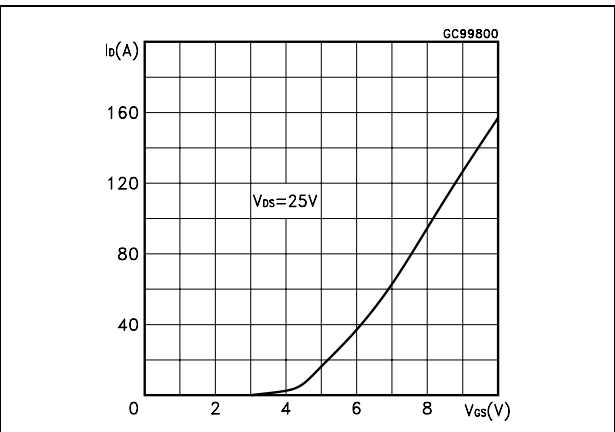


Figure 5. Transconductance

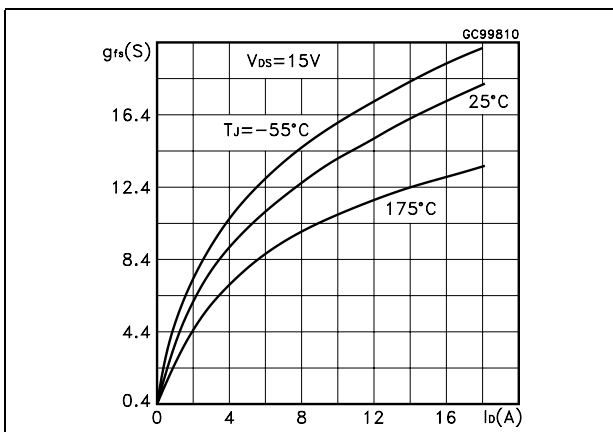


Figure 6. Static drain-source on resistance

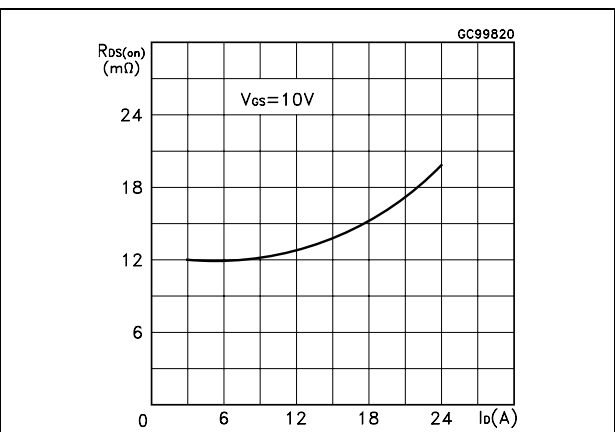


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

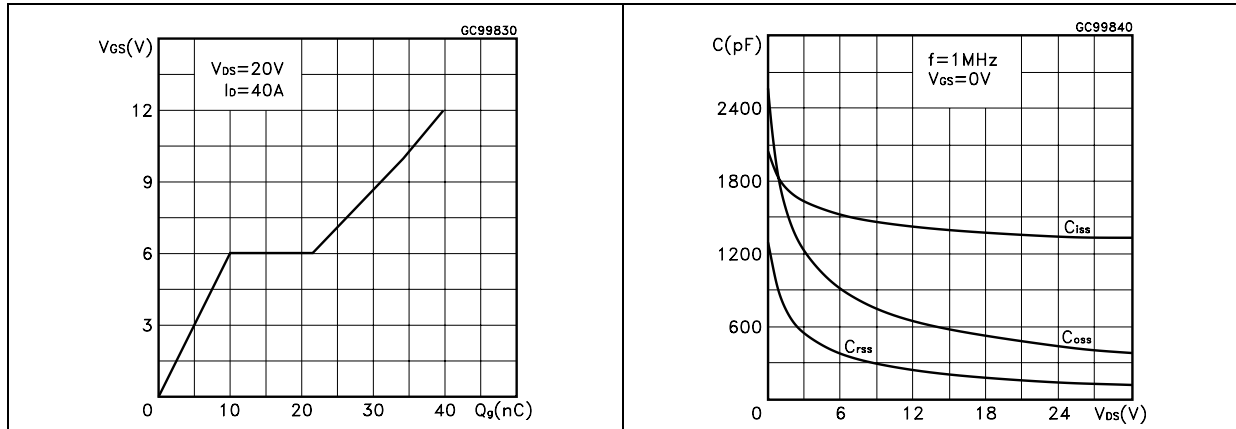


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

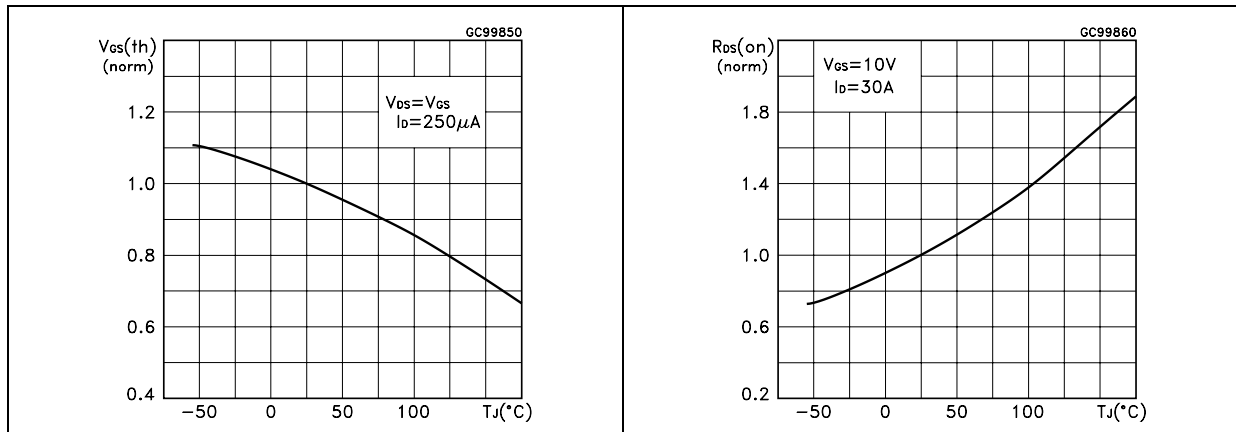
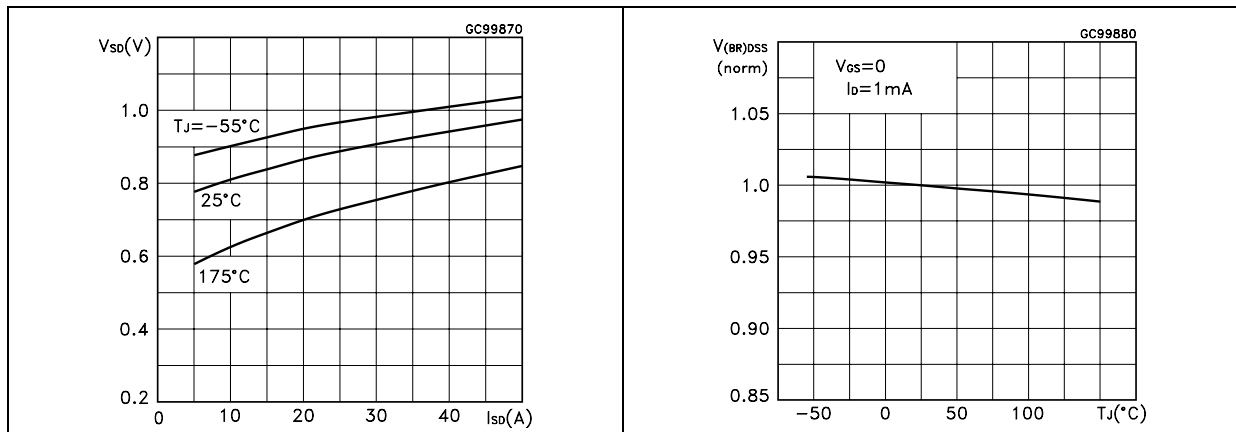


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized  $B_{V_{DS}}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

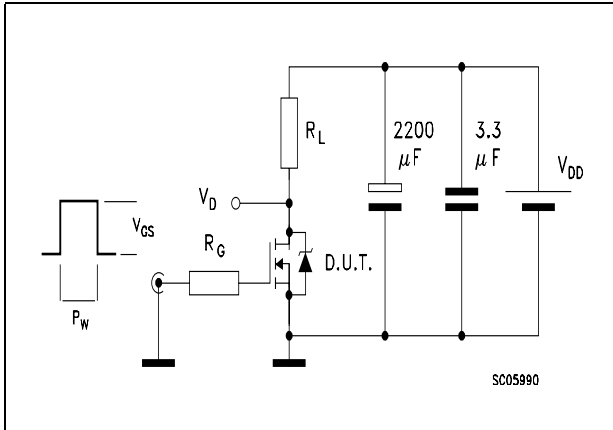


Figure 14. Gate charge test circuit

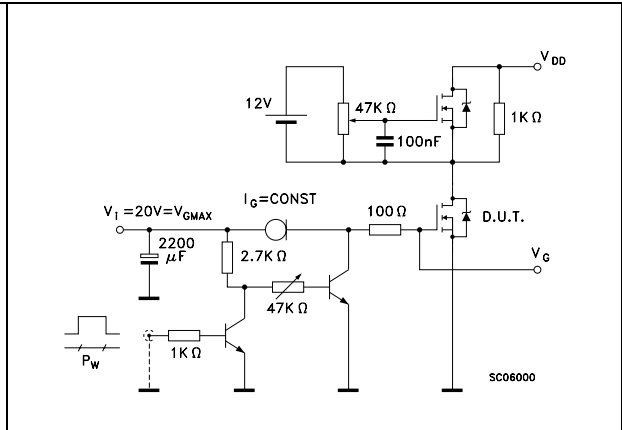


Figure 15. Test circuit for inductive load switching and diode recovery times

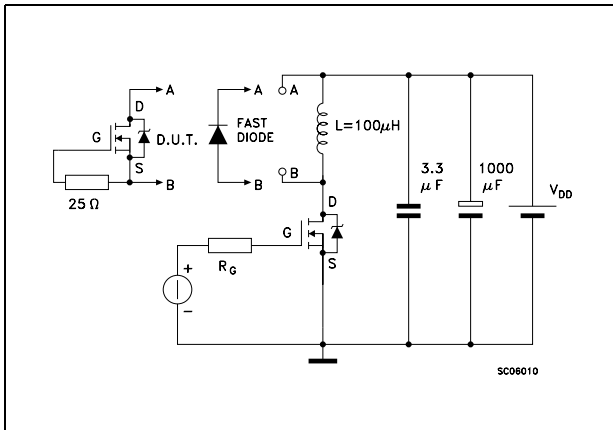


Figure 16. Unclamped Inductive load test circuit

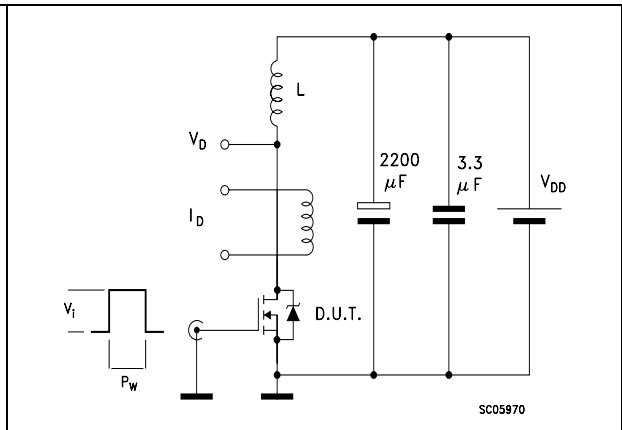
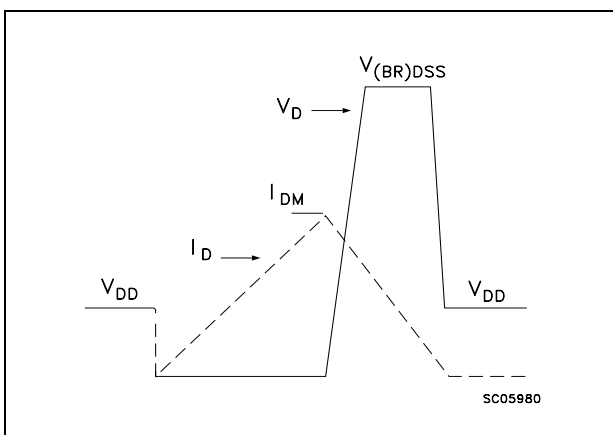


Figure 17. Unclamped inductive waveform



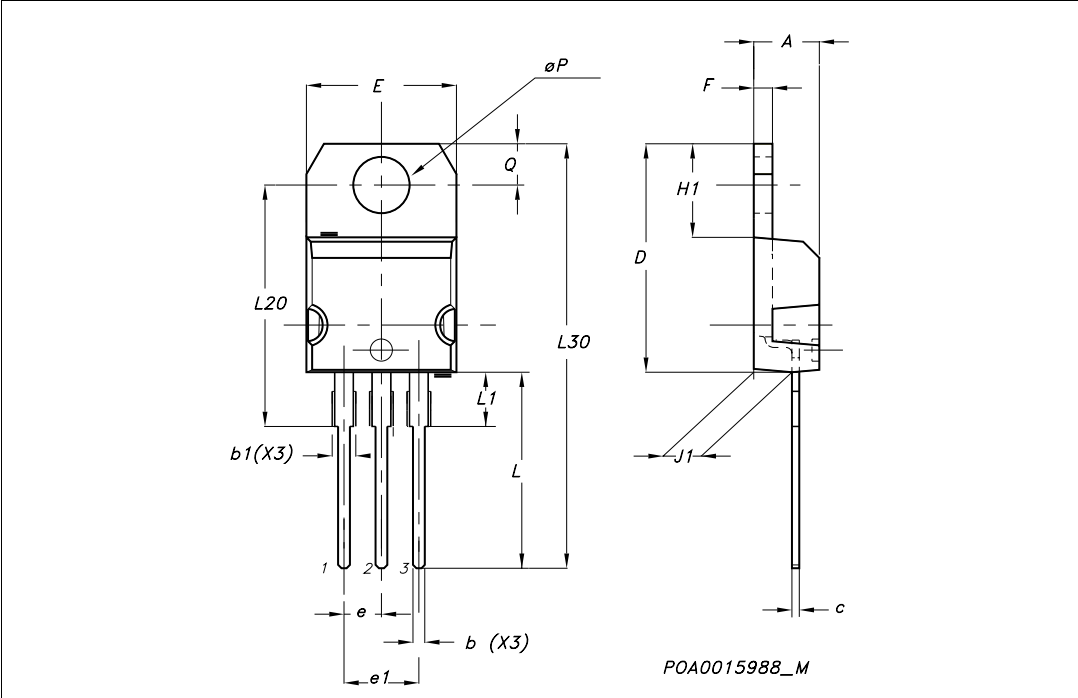


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 7. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
21-Jun-2004	2	Preliminary datasheet
22-Aug-2005	3	Complete document with curves
21-Jan-2006	4	New ECOPAK label
02-Oct-2006	5	New template, no content change

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