
Errata: EP9301

Reference EP9301 Data Sheet revision DS636PP1 dated January 04

Ethernet

Description 1

The Ethernet controller does not correctly receive frames that have a size of 64 bytes.

Workaround

In order to receive frames of 64 bytes, enable the RCRC bit in RxCTL. This will allow the Ethernet controller to ignore the CRC information and not discard the frames.

HDLC

Description 1

When the final byte of a received packet is read into the DMA controller's buffer, the software will be notified by an HDLC RFC interrupt. However, the DMA controller may not have written the currently buffered part of the packet to memory, so that the last one to fifteen bytes of a packet may not be accessible.

Workaround

To insure that the DMA channel empties the buffer, do the following (in the HDLC interrupt handler, for example):

1. Note the values in the MAXCNTx and REMAIN registers for the DMA channel. The difference is the number of bytes read from the UART/HDLC, which is the size of the HDLC packet. Call this number N. Note that the BC field of the UART1HDLCCRInfoBuf register should also be N.
2. Temporarily disable the UART DMA RX interface by clearing the RXDMAE bit in the UART1DMACtrl register.
3. Wait until the difference between the CURRENTx and BASEx registers in the DMA channel is equal to N + 1.

At this point, the rest of the packet is guaranteed to have been written to memory. Using this method will cause an extra byte to be read from the UART by the DMA channel and also written to memory. This last byte should be ignored.

Description 2

A synchronous HDLC frame consists of at least one opening flag, a series of bits, and at least one closing flag. The series of bits may consist of an address, control field, payload data, and a CRC.

Any time the HDLC has to transmit five consecutive one bits, it must append an extra zero bit, referred to as bit stuffing. For example, if ten consecutive ones appear, a zero is stuffed after the first five, and again after the second five.

This should also occur even if the series of ones appears at the end of a packet (possibly wholly within the CRC). The HDLC in the EP9301 implementation fails to stuff this extra zero bit at the end of a packet. The receiver will expect a stuffed zero bit, and ignore the bit transmitted after the last bit of the packet. This will be the first bit of the closing flag; the next six bits of the closing flag are all ones. The receiver will see them

not as part of a flag, but as part of the packet. This will cause the receiver to abort reception, because six ones cannot occur legally in a HDLC packet.

Workaround

The software workaround for this issue it is not trivial. The only way to circumvent this erratum is to avoid sending a packet with these properties:

1. The last N bits transmitted in the packet are ones, where N is a multiple of 5.
2. The preceding bit is zero. This could even be the final bit of the opening flag.

It is possible to examine any packet prior to transmission, calculating and appending the CRC if applicable, to determine the series of bits that will be transmitted. If the above property is satisfied, then the packet should be modified in some way (adding a byte, for example) prior to being sent.

ADC

Description 1

Pins ADC[3:1] have reduced dynamic range and are unusable.

Workaround

Currently, there is no workaround.

Description 2

ADC pins input impedance varies non-linearly with respect to voltage.

Workaround

Depending on the application, it may be necessary to use analog buffers to provide enough source current for each input pin to get correct readings from the ADC.

SDRAM Controller

Description 1

Using the EP9301 SDRAM controller in auto-precharge mode will produce system instability at external bus speeds greater than 50MHz.

Workaround

Do not turn on the auto-precharge feature of the EP9301 SDRAM controller if the external bus speed will be greater than 50 MHz.



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Contacting Cirrus Logic Support

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