PIC24FJ256GA110

PIC24FJ256GA110 Family Rev. A3 Silicon Errata

The PIC24FJ256GA110 Family Rev. A3 parts you have received conform functionally to the Device Data Sheet (DS39905**B**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC24FJ256GA110 Family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC24FJ256GA110 devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC24FJ256GA110	101Eh	01h
PIC24FJ192GA110	1016h	01h
PIC24FJ128GA110	100Eh	01h
PIC24FJ256GA108	101Ah	01h
PIC24FJ192GA108	1012h	01h
PIC24FJ128GA108	100Ah	01h
PIC24FJ256GA106	1018h	01h
PIC24FJ192GA106	1010h	01h
PIC24FJ128GA106	1008h	01h

The Device IDs (DEVID and REVID) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format “DEVID REVID”.

1. Module: Core (RAM Operation)

If a RAM read is performed on the instruction immediately prior to enabling Doze mode, an extra read event may occur when Doze mode is enabled. This has no effect on most SFRs and on user RAM space. However, this could cause registers which also perform some action on a read (such as auto-incrementing a pointer or removing data from a FIFO buffer) to repeat that action, possibly resulting in lost data or unexpected operation.

Work around

Avoid reading registers which perform a secondary action (e.g., UART and SPI FIFO buffers, and the RTCVAL registers) immediately prior to entering Doze mode.

If this cannot be avoided, execute a NOP instruction before entering Doze mode.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Core (BOR)

When the on-chip regulator is enabled (ENVREG tied to VDD), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and either:
- the internal band gap reference is being used as a reference with the A/D converter (AD1PCFGH<1> or <0> = 0) or comparators (CMxCON<1:0> = 11); or
- the CTMU module is enabled.

Work around

Limit the following activities to only those times when the on-chip regulator is not in Tracking mode (LVDIF (IFS4<8>) = 0):

- enabling the CTMU module;
- selecting the internal band gap as a reference for the A/D converter or the comparators.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: JTAG (Device Programming)

The JTAGEN Configuration bit can be programmed to ‘0’ while using the JTAG interface for device programming. This may cause a situation where JTAG programming can lock itself out of being able to program the device.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4 Module: UART

When the UART is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: I/O (PORTB)

When RB5 is configured as an open-drain output, it remains in a high-impedance state. The settings of LATB5 and TRISB5 have no effect on the pin's state.

Work around

If open-drain operation is not required, configure RB5 as a regular I/O (ODCB<5> = 0).

If open-drain operation is required, there are two options:

- select a different I/O pin for the open-drain function; or
- place an external transistor on the pin, and configure the pin as a regular I/O.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: SPI (Master Mode)

In Master mode, both the SPI interrupt flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0); and
- the module is configured for serial data output changes on transition from clock active to clock idle state (CKE = 1)

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPI buffer, check the SCK pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this; in this example, pin RD1 functions as the SPI clock SCK, which is configured as idle-low.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: CTMU

When the CTMU module is selected as the trigger source (SYNCSEL4:SYNCSEL0 = 11000), the input capture and/or output compare trigger may not work.

Work around

Manually trigger the input capture and/or output compare module(s) after a CTMU event is received. Be certain to compensate for any time latency that results from manually triggering the module.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPI CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

8. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 9.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or ¾ full (UxSTA<7:6> = 1x), and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes with a parity or framing error will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: SPI (Enhanced Buffer Modes)

If the SPI event interrupt is configured to occur when the enhanced FIFO buffer is full (SISEL2:SISEL0 = 111), the interrupt may actually occur when the 7th byte is written to the buffer, instead of the 8th byte. The other enhanced buffer interrupts function as previously described.

Work around

Do not use the Full Buffer Interrupt mode. The SPITBF bit (SPIxSTAT<1>) reliably indicates when the enhanced FIFO buffer is full, and can be polled instead of using the Full Buffer Interrupt mode.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: UART (IrDA®)

When the UART is operating in 8-bit mode (PDSEL1:PDSEL0 = 0x) and using the IrDA endec (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around:

None.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: UART (IrDA)

When the UART is operating in 8-bit mode (PDSEL1:PDSEL0 = 0x) and using the IrDA endec (IREN = 1), a framing error may occur when transmitting a data payload of 00h.

Work around:

None.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: UART (IrDA)

When the UART is operating in 9-bit mode (PDSEL1:PDSEL0 = 1x) and using the IrDA endec (IREN = 1), the module will incorrectly transmit 10 bits when transmitting data payloads of 00h or 80h.

Work around:

None.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: Core (Instruction Set)

If an instruction producing a Read-After-Write stall condition is executed inside a REPEAT loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 15 times.

Work around

Avoid using REPEAT to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches. The MPLAB C Compiler will not generate REPEAT loops that cause this erratum.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit `MOV` instruction is used to read the data at location 8000h. The MPLAB C Compiler (v3.11 or later) supports the option "`-merrata=psv_trap`" to prevent it from generating code that would cause this erratum.

Work around

Do not use the first location of the a PSV page (address 8000h).

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: ICSP™

The ICSP/ICD port pair PGEC3/PGED3 (RB5/RB4) cannot be used to read or program the device.

Work around

Use either PGEC2/PGED2 or PGEC1/PGED1.

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR, and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: I^2C Module (Master Mode)

Under certain circumstances, a module operating in Master mode may acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-bit Addressing mode is used (A10M = 1), and:
- the I^2C Master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the Master also acknowledges the address command and generates an erroneous I^2C Slave interrupt, as well as the I^2C Master interrupt.

Work around

Several options are available:

- When using 10-bit Addressing mode, make certain that the Master and Slave devices do not share the same 2 MSBs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = `0`) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a Slave I^2C interrupt occurs on the Master module.

Date Codes that pertain to this issue:

All engineering and production devices.

I^2C Module (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I^2C protocol. This happens when the following occurs:

- 10-bit Addressing mode is used (A10M = 1), and:
- bits A7:A1 of the Slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges '`1111xxx`' or '`0000xxx`'.

In these cases, the Slave module acknowledges the command and triggers an I^2C Slave interrupt; it does *not* copy the data into the I2CxRCV register, or set the RBF bit.

Work around

Do not set bits A7:A1 of the module's Slave address equal to '`1111xxx`' or '`0000xxx`'.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: I²C Module (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-bit Addressing mode is used (A10M = 1), and
- bits A7:A1 of the Slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges '1111xxx' or '0000xxx'.

In these cases, the Slave module acknowledges the command and triggers an I²C Slave interrupt; it does not copy the data into the I2CxRCV register, or set the RBF bit.

Work around

Do not set bits A7:A1 of the module's Slave address equal to '1111xxx' or '0000xxx'.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: A/D Converter

When using PGEC1 and PGED1 to debug an application on any 64-pin devices in this family, all voltage references will be disabled. This includes Vref+, Vref-, AVdd, and AVss. Any A/D conversion will always equal 0x3FF.

Note:	This issue applies only 64-pin devices in this family (PIC24FJ256GA106, PIC24FJ192GA106, and PIC24FJ128GA106).

Work around

Use PGEC2 and PGED2 to debug any A/D functionality.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (2/2008)

First revision of this document. Includes silicon issues 1 (Core, RAM Operation), 2 (Core, BOR), 3 (JTAG, Programming), 4 (UART), 5 (I/O, PORTB), 6 (SPI) and 7 (Input Capture).

Rev B Document (4/2008)

Revised silicon issues 7 to clarify the requirement for latency compensation. Added silicon issues 8 (UART – UERIF Interrupt), 9 (UART – FIFO Error Flags) and 10 (SPI – Enhanced Buffer Modes).

Rev C Document (7/2008)

Revised silicon issues 4 (UART) and 6 (SPI, Master Mode) to reflect updated definition of issues. Added silicon issues 11 through 13 (UART, IrDA), 14 (Core, Instruction Set), 15 (Memory, Program Space Visibility), 16 (ICSP), 17 (RTCC), 18 (I^2C, Master Mode), 19 (I2C Module (Slave Mode) and 20 (A/D Converter).

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