PIC24FJ64GA004 Family Rev. B4 Silicon Errata

The PIC24FJ64GA004 Family parts you have received conform functionally to the Device Data Sheet (DS39881**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC24FJ64GA004 Family will be reported in a separate. Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC24FJ64GA family devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC24FJ16GA002	00444h	3042h
PIC24FJ32GA002	00445h	3042h
PIC24FJ48GA002	00446h	3042h
PIC24FJ64GA002	00447h	3042h
PIC24FJ16GA004	0044Ch	3042h
PIC24FJ32GA004	0044Dh	3042h
PIC24FJ48GA004	0044Eh	3042h
PIC24FJ64GA004	0044Fh	3042h

1. Module: Core (BOR)

When the on-chip regulator is enabled (DISVREG tied to VSS), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and
- the internal band gap reference is being used as a reference with the A/D converter (AD1PCFG<15> = 0)

Work around

Do not select the internal band gap as a reference for the A/D converter when the on-chip regulator is in Tracking mode (LVDIF (IFS4<8>) = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit MOV instruction is used to read the data at location 8000h.

Work around

Do not use the first location of the a PSV page (address 8000h).

The MPLAB C Compiler (v3.11 or later) supports the option, `-merrata=psv_trap`, to prevent it from generating code that would cause this erratum.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/ BOR and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: I²C (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- the I²C master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the master also Acknowledges the address command and generates an erroneous I²C slave interrupt, as well as the I²C master interrupt.

Work around

Several options are available:

- When using 10-bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSbs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = 0) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I²C interrupt occurs on the master module.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: I²C (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- bits, A7:A1, of the slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges '1111xxx' or '0000xxx'.

In these cases, the slave module Acknowledges the command and triggers an I²C slave interrupt; it does *not* copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A7:A1, of the module's slave address equal to '1111xxx' or '0000xxx'.

Date Codes that pertain to this issue:

All engineering and production devices.

6 Module: UART

When the UART is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 8.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or 3/4 full (UxSTA<7:6> = 1x), and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes, with a parity or framing error, will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (7/2008)

First version of this document. Silicon issues 1 (Core – BOR), 2 (Memory – Program Space Visibility), 3 (RTCC), 4 (I^2C – Master Mode), 5 (I^2C – Slave Mode) and 6-8 (UART).

NOTES:

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