PIC24FJ64GA004 Family Rev. A3 Silicon Errata

The PIC24FJ64GA004 Family parts you have received conform functionally to the Device Data Sheet (DS39881**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC24FJ64GA004 Family will be reported in a separate. Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC24FJ64GA family devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC24FJ16GA002	00444h	3003h
PIC24FJ32GA002	00445h	3003h
PIC24FJ48GA002	00446h	3003h
PIC24FJ64GA002	00447h	3003h
PIC24FJ16GA004	0044Ch	3003h
PIC24FJ32GA004	0044Dh	3003h
PIC24FJ48GA004	0044Eh	3003h
PIC24FJ64GA004	0044Fh	3003h

1. Module: JTAG

When the JTAG is disabled, the pull-up resistor on the TDI pin (pin 35/RA9) will stay enabled on the 44-pin variants of the device. This can cause the device to draw extra current when asleep if the pin is used as an input and held low.

Work around:

The pin will not draw extra current if any of the following work around techniques are used:

- The pin is used as an output.
- The pin is driven high as an input.
- JTAG is enabled.

Date Codes that pertain to this issue:

All PIC24FJ16GA004, PIC24FJ32GA004, PIC24FJ48GA004 and PIC24FJ64GA004 engineering and production devices.

2. Module: Low-Voltage Detect

The Low-Voltage Detect interrupt will not occur if the device comes out of Reset in a low-voltage state. To trigger an interrupt, the voltage must decrease to a low-voltage range while the device is running.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Core

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled), the user software should check the status of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform an appropriate clock switch operation.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Core

If a RAM read is performed on the instruction immediately prior to enabling Doze mode, then an extra read event will occur when Doze mode is enabled. On most SFRs and on user RAM space, this will have no visible effect. However, this can cause registers which perform actions on reads, such as auto-incrementing or decrementing a pointer or removing data from a FIFO buffer, to repeat that action, possibly resulting in lost data.

Work around

On the instruction prior to entering Doze mode, be sure not to read a register which performs a secondary action. Examples of this would be UART and SPI FIFO buffers, and the RTCVAL registers. The easiest way to ensure this does not occur is to execute a NOP instruction before entering Doze mode.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Core

On a Brown-out Reset, both the BOR and POR bits may be set. This may cause the Brown-out Reset condition to be indistinguishable from the Power-on Reset.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Core

The PIC24FJ16GA002 and PIC24FJ16GA004 devices have 8K of data RAM implemented instead of 4K. This will cause the address error trap not to function for addresses between 2000h and 27FFh.

Work around

Do not access RAM beyond address 17FFh to maintain software compatibility with future device revisions.

Date Codes that pertain to this issue:

All PIC24FJ16GA002 and PIC24FJ16GA004 engineering and production devices.

7. Module: A/D

The AD1PCFG and AD1CHS registers allow unimplemented channels to be selected. If these channels are selected, they will read as if tied to VSS. These channels should be disabled.

Work around

Disable channels AN13 and AN14 in the AD1PCFG register by ensuring that bits 13 and 14 are cleared.

Ensure that bits 5 and 12 of AD1CHS are maintained cleared. If these bits are set, it will cause the ADC to reference channels AN16-31.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: A/D

The A/D module will not generate code 511. Any conversion which should result in 511 normally, will instead generate 510 or 512.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: A/D

With the External Interrupt 0 (INT0) selected to start an A/D conversion (SSRC<2:0> = 001), the device may not wake-up from Sleep or Idle mode if more than one conversion is selected per interrupt (SMPI<3:0> <> 0000). Interrupts are generated correctly if the device is not in a Sleep or Idle mode.

Work around

Configure the A/D to generate an interrupt after every conversion (SMPI<3:0> = 0000). Use another wake-up source, such as the WDT or another interrupt source, to exit the Sleep or Idle mode. Alternatively, perform A/D conversions in Run mode.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: I²C™ (I2C1, SDA Line State)

When using I2C1, the SDA1 line state may not be detected properly unless it is first held low for 150 ns after enabling the I²C module.

In Master mode, this error may cause a bus collision to occur instead of a Start bit transmission. Transmissions after the SDA1 pin has been held low will occur correctly.

In Slave mode, the device may not Acknowledge the first packet sent after enabling the I²C module. In this case, it will return a NACK instead of an ACK. The device will correctly respond to packets after detecting a low level on the line for 150 ns.

The I2C2 module operates as expected and does not exhibit this issue.

Work around

Using an external device or another I/O pin from the microcontroller, drive the SDA1 pin low.

If no external devices or additional I/O pins are available, it is sometimes possible to perform the work around internally, using the following steps:

- With the module in Master mode, configure the RB9 pin as an output;
- Clear the LATB9 bit (for the default I2C1 assignment) or LATB5 (for the alternate I2C1 assignment) to drive the pin low;
- Enable I2C1 by setting the I2CEN bit (I2C1CON<15>).

Note that this action could appear to be a Start bit to an I²C slave device on the bus if the RB8/SCL1 pin is not driven low prior to driving RB9/SDA1 low. It may be necessary to add additional capacitance to the SDA1 bus in order to maintain the low logic level long enough for the module to detect the low logic level. Make sure that when adding capacitance, that the application does not violate the I²C timing specifications.

In Slave mode, the I²C master device on the bus either must pull the SDAx line low, then high again, prior to sending the first packet to the device, or must resend the first packet.

Note that 150 ns is the *absolute maximum* time required to avoid the issue. It is possible to work around the issue using a shorter delay in some devices.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: UART

When the UART is in High-Speed mode, BRGH (UxMODE<3>) is set, some optimal UxBRG values can cause reception to fail.

Work around

Test UxBRG values in the application to find a UxBRG value that works consistently for more high-speed applications. The user should verify that the UxBRG baud rate error does not exceed the application limits. If possible, it is recommended to use a comparable baud rate in Low-Speed mode.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: UART

When the UART is in High-Speed mode (BRGH = 1), the auto-baud sequence can calculate the baud rate as if it were in Low-Speed mode.

Work around

The calculated baud rate can be modified by the following equation:

New BRG Value = (Auto-Baud BRG + 1) * 4 – 1

The user should verify that the baud rate error does not exceed application limits.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If a receive interrupt occurs, check the URXDA bit (UxSTA<0>) to ensure that valid data is available. On the first interrupt, no data will be present. The second interrupt will have the Sync field character (55h) in the receive FIFO.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: UART

With the auto-baud feature selected, the Sync field character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync field character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: UART

The auto-baud may miscalculate for certain baud rates and clock speed combinations, resulting in a BRG value that is 1 greater or less than the expected value. When UxBRG is less than 50, this can result in transmission and reception failures due to introducing error greater than 1%.

Work around

Test auto-baud calculations at various clock speed and baud rate combinations that would be used in applications. If an inaccurate UxBRG value is generated, manually correct the baud rate in user code.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: Output Compare

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle) and the OCxRS register is updated with a value of 0x0001. The compare event is only missed the first time a value of 0x0001 is written to OCxRS, and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002. In this case, however, the duty cycle will be slightly different from the desired value.

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: SPI

When using Enhanced Buffer mode, some indicator bits may be set at incorrect times:

- For slave transfers, the SRMPT bit (SPIxSTAT<7>) is set early, after only 7 SCK periods
- For Slave Interrupt modes, SISELx = 5, there is a one SCK period delay between the interrupt event and the SPIxIF bit being set
- There may be a several instruction cycle delay between the FIFO full or FIFO empty events and the interrupt flags or indicator bits being set

Work around

None at this time.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: SPI

In SPI Slave mode (MSTEN = 0), with the slave select option enabled (SSEN = 1), the peripheral may accept transfers regardless of the $\overline{SS}$x pin state. The received data in SPIxBUF will be accurate but not intended for the device.

Work around

There is a work around using the peripheral pin select feature. One of the external interrupts (INT1 or INT2) can be mapped to the same pin as the $\overline{SS}$x signal or the $\overline{SS}$x signal can be mapped to a pin with interrupt-on-change (CNx) functionality. If the $\overline{SS}$x signal changes to low (active), the interrupt flag will be set.

When an SPI data received interrupt occurs, the interrupt flag can be tested. If the interrupt mapped to $\overline{SS}$x did not occur, discard the data.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: SPI

When using Enhanced Buffer mode, an interrupt will not occur if the following conditions exist:

- SPI Buffer Interrupt mode, SISEL<2:0> (SPIxSTAT<4:2>), is set to interrupt when the Shift register is empty (SISEL<2:0> = 101)
- Slave Select mode is enabled (SSEN = 1)

This only occurs when Enhanced mode, Slave Select mode and interrupt on Shift register empty are all enabled. In other modes, the interrupt will work correctly.

Work around

When Slave Select mode is enabled, interrupting on SPIxSR empty and TX empty will occur at the same time. Therefore, interrupting on TX FIFO empty (SISEL<2:0> = 110) can be used as an alternative to interrupting when the Shift register is empty (SISEL<2:0> = 101).

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: I/O Ports

The I/O pin outputs, V_{OL} and V_{OH}, meet the specifications in Table 1 below.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	V_{OL}	**Output Low Voltage**					
DO10		All I/O Pins	—	—	.55	V	I_{OL} = 8.5 mA, V_{DD} = 3.6V
			—	—	.4	V	I_{OL} = 7.8 mA, V_{DD} = 3.6V
			—	—	.55	V	I_{OL} = 6.0 mA, V_{DD} = 2.0V
			—	—	.4	V	I_{OL} = 5.0 mA, V_{DD} = 2.0V
	V_{OH}	**Output High Voltage**					
DO20		All I/O Pins	3.0	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
			2.4	—	—	V	I_{OH} = -6.0 mA, V_{DD} = 3.6V
			1.65	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 2.0V
			1.4	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 2.0V

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

21. Module: I/O Ports

During Power-on Reset (POR), the device may drive the OSCO/RA3 pin as a clock out output for approximately 20 μS. During this time, the pin will be driven high and low rather than being set to high-impedance. This may cause issues on designs that use the pin as a general purpose I/O.

Designs should be reviewed to ensure that their intended operation will not be disrupted if the pin is driven during POR.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: JTAG

When entering the SHIFT_DR state while in ICSP™ Communications mode, an extra clock edge may be generated, causing JTAG and ICSP communications to lose synchronization. This prevents device programming using ICSP over JTAG. JTAG boundary scan is not affected and operates as expected.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: RTCC

When performing writes to the ALCFGRPT register, some bits may become corrupted. The error occurs because of desynchronization between the CPU clock domain and the RTCC clock domain.

The error causes data, from the instruction *following* the ALCFGRPT instruction, to overwrite the data in ALCFGRPT.

Work around

Always follow writes to the ALCFGRPT register with an additional write of the same data to a dummy location. These writes can be performed to RAM locations, W registers or unimplemented SFR space.

The optimal way to perform the work around:

1. Read ALCFGRPT into a RAM location.
2. Modify the ALCFGRPT data, as required, in RAM.
3. Move the RAM value into ALCFGRPT, and a dummy location, in back-to-back instructions.

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: I^2C

When the I^2C module is operating in Slave mode, after the ACKSTAT bit is set when receiving a NACK from the master, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK from the master.

Date Codes that pertain to this issue:

All engineering and production devices.

25. Module: I^2C

Bit and byte-based operations may not have the intended affect on the I2CxSTAT register. It is possible for bit and byte operations performed on the lower byte of I2CxSTAT to clear the BCL bit (I2CxSTAT<10>). Bit and byte operation performed on the upper byte of I2CxSTAT, or on the BCL bit directly, may not be able to clear the BCL bit.

Work around

Modifications to the I2CxSTAT register should be done using word writes only. This can be done in C by always writing to the register itself and not the individual bits. For example, the code, `I2C1STAT &= 0xFBFF`, will force the compiler to use a word-based operation to clear the BCL bit. In assembly, it is done by not using `BSET` or `BCLR` instructions or instructions with the `.b` modifier.

Date Codes that pertain to this issue:

All engineering and production devices.

26. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = `11`), the 16x baud clock signal on the BCLK pin will only be present when the module is transmitting. The pin will be Idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Date Codes that pertain to this issue:

All engineering and production devices.

27. Module: I/O (Peripheral Pin Select)

The remappable pin functions multiplexed to some pins do not have a higher priority than fixed digital signals assigned to those pins. By design, a remapped digital function should always have priority over any other fixed digital function on the same pin.

Using these remappable and specific fixed digital functions at the same time may cause conflicts and unexpected results on:

- RP12 and PMD0
- RP18 and PMA2 (40-pin and 44-pin devices only)

No other fixed digital functions are affected.

Work around

On the affected pins, enable either the remappable peripherals, or the specific fixed digital peripherals, but not both at the same time.

Date Codes that pertain to this issue:

All engineering and production devices.

28. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 29.

Date Codes that pertain to this issue:

All engineering and production devices.

29. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or 3/4 full (UxSTA<7:6> = 1x), and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes, with a parity or framing error, will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

30. Module: Core (BOR)

When the on-chip regulator is enabled (DISVREG tied to VSS), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and
- the internal band gap reference is being used as a reference with the A/D converter (AD1PCFG<15> = 0)

Work around

Do not select the internal band gap as a reference for the A/D converter when the on-chip regulator is in Tracking mode (LVDIF (IFS4<8>) = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

31. Module: Core (Instruction Set)

If an instruction producing a read-after-write stall condition is executed inside a REPEAT loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 16 times.

Work around

Avoid using REPEAT to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches.

The MPLAB® C Compiler will not generate REPEAT loops that cause this erratum.

Date Codes that pertain to this issue:

All engineering and production devices.

32. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit MOV instruction is used to read the data at location 8000h.

Work around

Do not use the first location of the a PSV page (address 8000h).

The MPLAB C Compiler (v3.11 or later) supports the option, `-merrata=psv_trap`, to prevent it from generating code that would cause this erratum.

Date Codes that pertain to this issue:

All engineering and production devices.

33. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Date Codes that pertain to this issue:

All engineering and production devices.

34. Module: SPI (Master Mode)

In Master mode, the SPI Interrupt Flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may both become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0); and
- the module is configured for serial data output changes on transition from clock active to clock Idle state (CKE = 1)

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPI buffer, check the SCK pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this. In this example, the RD1 pin functions as the SPI clock SCK, which is configured as Idle low.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPI CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

35. Module: I²C (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- the I²C master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the master also Acknowledges the address command and generates an erroneous I²C slave interrupt, as well as the I²C master interrupt.

Work around

Several options are available:

- When using 10-Bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSbs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = 0) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I²C interrupt occurs on the master module.

Date Codes that pertain to this issue:

All engineering and production devices.

36. Module: I²C (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- bits, A7:A1, of the slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges '1111xxx' or '0000xxx'.

In these cases, the Slave module Acknowledges the command and triggers an I²C slave interrupt; it does *not* copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A7:A1, of the module's slave address equal to '1111xxx' or '0000xxx'.

Date Codes that pertain to this issue:

All engineering and production devices.

37. Module: I²C

The Transmit Buffer Full flag, TBF (I2CxSTAT<0>), may not be cleared by hardware if a collision on the I²C bus occurs before the first falling clock edge during a transmission.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

38 Module: UART

When the UART is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

39 Module: Oscillator (SOSC)

The low-power secondary oscillator option, selected by the SOSCSEL Configuration bits (CW2<12:11>), is not available in this silicon revision. The oscillator in all devices functions in the Default (high-gain) mode only.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

40 Module: Voltage Regulator

The Standby mode wake-up option, selected by the WUTSEL Configuration bits (CW2<14:13>), is not available in this silicon revision. All devices use the default regulator wake-up time of 190 μs.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (3/2007)

First version of this document. Silicon issues 1 (Core), 2 (Core – Interrupt), 3-6 (Core), 7-9 (A/D), 10 (PMP), 11 (I^2C), 12-16 (UART), 17 (Output Compare), 18-20 (SPI), 21 (RTCC), 22 (CRC) and 23 (I/O Pins).

Rev B Document (7/2007)

Removed silicon issue 3 (Core) and 21 (RTCC). Reworded silicon issue 11 (1^2C). Added silicon issues 4 (Core), 23 (Core), 24 (JTAG) and 25 (RTCC).

Rev C Document (9/2007)

Modified silicon issues 8 (A/D), 11 (I^2C) and 22 (I/O Ports), added silicon issues 25-26 (I^2C), removed silicon issue 21 (CRC) and corrected revision history for Revision B.

Rev D Document (9/2007)

Modified silicon issue 11 (I^2C).

Rev E Document (10/2007)

Modified silicon issues 1 (JTAG) and 2 (Low-Voltage Detect). Removed silicon issue 10 (PMP), renumbering subsequent silicon issues as 10 through 25. Added new silicon issue 26 (UART).

Rev F Document (3/2008)

Modified silicon issues 10 (I^2C – I2C1, SDA Line State) to reflect more specific information since its previous update in Revision E. Added silicon issues 27 (I/O – Peripheral Pin Select), 28 (Oscillator – OSCO Pin and SOSC), 29 (UART – UERIF Interrupt), 30 (UART – FIFO Error Flags) and 31 (Core – BOR). Corrected revision history to reflect renumbering that occurred with Revision F.

Rev G Document (7/2008)

Removed silicon issue 28 (Oscillator – OSCO Pin and SOSC), renumbered subsequent issues as 28 through 30. Added silicon issues 31 (Core – Instruction Set), 32 (Memory – Program Space Visibility), 33 (RTCC), 34 (SPI – Master Mode), 35 through 37 (I^2C), 38 (UART), 39 (Oscillator – SOSC) and 40 (Voltage Regulator).

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