# PIC24FJ64GA004 Family Data Sheet Errata

In the PIC24FJ64GA004 Family Device Data Sheet (DS39881**C**), the following clarifications and corrections should be noted. Any silicon issues related to these devices will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

## 1. Module: Electrical Characteristics

In **Section 26.1 "DC Characteristics",** the values for parameters DC51b and DC51c (Idle Current) are reported incorrectly. The correct values are shown in the extract from Table 26-5 below (changes in **bold**).

**TABLE 26-5: DC CHARACTERISTICS: IDLE CURRENT ($I_{IDLE}$) (PARTIAL REPRESENTATION)**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Conditions** | | |
| **Idle Current ($I_{IDLE}$): Core Off, Clock On Base Current, PMD Bits are Set(2)** | | | | | | |
| DC51 | 4 | 6 | µA | -40°C | 2.0V(3) | LPRC (31 kHz) |
| DC51a | 4 | 6 | µA | +25°C | | |
| DC51b | **8** | **16** | µA | +85°C | | |
| DC51c | **20** | **50** | µA | +125°C | | |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** Base $I_{IDLE}$ current is measured with core off, clock on, all modules off and all of the Peripheral Module Disable (PMD) bits are set.

**3:** On-chip voltage regulator disabled (DISVREG tied to $V_{DD}$).

**2. Module: 10-Bit High-Speed A/D Converter**

The AD1CON3 register has been changed to reflect the current operation of the A/D Clock Selection Bits (ADSC7:ADSC0). The changes are shown in Register 20-3, below (updated text in **bold**; bold text in original removed for clarity).

**REGISTER 20-3: AD1CON3: A/D CONTROL REGISTER 3**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADRC | — | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 ADRC: A/D Conversion Clock Source bit
1 = A/D internal RC clock
0 = Clock derived from system clock

bit 14-13 Unimplemented: Read as ‘0’

bit 12-8 SAMC4:SAMC0: Auto-Sample Time bits
11111 = 31 TAD
.....
00001 = 1 TAD
00000 = 0 TAD (not recommended)

bit 7-0 ADCS7:ADCS0: A/D Conversion Clock Select bits
**11111111**
**.....  = Reserved**
**01000000**
**00111111 = 64 • TCY**
.....
00000001 = 2 • TCY
00000000 = TCY

### 3. Module: I/O Ports

The following section and accompanying table have been added immediately after the existing **Section 9.2.1 "I/O Port Write/Read Timing".** The current Table 9-1 and subsequent tables are sequentially renumbered.

#### 9.2.2 ANALOG INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins are always to be avoided. Table 9-1 summarizes the input capabilities. Refer to **Section 26.1 "DC Characteristics"** for more details.

**TABLE 9-1: INPUT VOLTAGE LEVELS**

| Port or Pin | Tolerated Input | Description |
|---|---|---|
| PORTA<4:0> | VDD | Only VDD input levels tolerated. |
| PORTB<15:12> | | |
| PORTB<4:0> | | |
| PORTC<2:0>(1) | | |
| PORTA<10:7>(1) | 5.5V | Tolerates input levels above VDD, useful for most standard logic. |
| PORTB<11:5> | | |
| PORTC<9:3>(1) | | |

**Note 1:** Unavailable on 28-pin devices.

### 4. Module: Oscillator Configuration

The following section has been appended to the end of **Section 7.0 "Oscillator Configuration"**. Additional changes to the device data sheet related to this issue are presented in Clarification #6 (Special Features).

## 7.5 Secondary Oscillator Features

#### 7.5.1 SECONDARY OSCILLATOR LOW-POWER OPERATION

| | |
|---|---|
| **Note:** | This feature is implemented only on PIC24FJ64GA004 family devices with a major silicon revision level of B or later (DEVREV register value is 3042h or greater). |

The Secondary Oscillator (SOSC) can operate in two distinct levels of power consumption based on device configuration. In Low-Power mode, the oscillator operates in a low-gain, low-power state. By default, the oscillator uses a higher gain setting, and therefore, requires more power. The Secondary Oscillator Mode Selection bits, SOSCSEL1:SOSCSEL0 (CW2<12:11>), determine the oscillator's power mode.

When Low-Power mode is used, care must be taken in the design and layout of the SOSC circuit to ensure that the oscillator will start up and oscillate properly. The lower gain of this mode makes the SOSC more sensitive to noise and requires a longer start-up time.

#### 7.5.2 OSCILLATOR LAYOUT

On low pin count devices, such as those in the PIC24FJ64GA004 family, due to pinout limitations, the SOSC is more susceptible to noise than other PIC24F devices. Unless proper care is taken in the design and layout of the SOSC circuit, it is possible for inaccuracies to be introduced into the oscillator's period.

In general, the crystal circuit connections should be as short as possible. It is also good practice to surround the crystal circuit with a ground loop or ground plane. For more detailed information on crystal circuit design, please refer to the "*PIC24F Family Reference Manual*", **Section 6. "Oscillator"** (DS39700) and Microchip Application Notes *AN826,* "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PICmicro® Devices" (*DS00826) and *AN849, "Basic PICmicro® Oscillator Design"* (DS00849).

## 5. Module: Special Features

The existing version of **Section 23.2.5 "Voltage Regulator Standby Mode"** is modified with the following additional material. Changes are shown in **bold**.

Additional changes to the device data sheet related to this issue are presented in Clarification #6 (Special Features) and Clarification #7 (Electrical Specifications).

### 23.2.5 VOLTAGE REGULATOR STANDBY MODE

When enabled, the on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator automatically **places itself into Standby mode** whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (RCON<8>). By default, this bit is cleared which enables Standby mode.

**For select PIC24FJ64GA004 family devices, the time required for regulator wake-up from Standby mode is controlled by the WUTSEL1:WUTSEL0 Configuration bits (CW2<14:13>). The default wake-up time for all devices is 190 μs. Where the WUTSEL Configuration bits are implemented, a fast wake-up option is also available. When WUTSEL1:WUTSEL0 = 01, the regulator wake-up time is 25 μs.**

| | |
|---|---|
| **Note:** | **This feature is implemented only on PIC24FJ64GA004 family devices with a major silicon revision level of B or later (DEVREV register value is 3042h or greater).** |

**When the regulator's Standby mode is turned off (VREGS = 1), Flash program memory stays powered in Sleep mode and** the device can wake-up in less than 10 μs. When VREGS is set, the power consumption while in Sleep mode, will be approximately 40 μA higher than power consumption when the regulator is allowed to enter Standby mode.

## 6. Module: Special Features

Register 23-2 (CW2: Flash Configuration Word 2) has been amended to add the SOSCEL and WUTSEL Configuration bits. The changes are shown in the abbreviated Register 23-2 that follows. Changes are shown in **bold**, and bold from the original has been removed for clarity.

| | |
|---|---|
| **Note:** | The descriptions for bits 10 through 2 and their corresponding rows are unchanged in the original. They have been removed here for the sake of brevity. |

**REGISTER 23-2: CW2: FLASH CONFIGURATION WORD 2 (PARTIAL REPRESENTATION)**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| R/PO-1 | **R/PO-1** | **R/PO-1** | **R/PO-1** | **R/PO-1** | R/PO-1 | R/PO-1 | R/PO-1 |
|---|---|---|---|---|---|---|---|
| IESO | **WUTSEL1(1)** | **WUTSEL0(1)** | **SOSCSEL1(1)** | **SOSCSEL0(1)** | FNOSC2 | FNOSC1 | FNOSC0 |
| bit 15 | | | | | | | bit 8 |

| R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | U-1 | R/PO-1 | R/PO-1 | R/PO-1 |
|---|---|---|---|---|---|---|---|
| FCKSM1 | FCKSM0 | OSCIOFCN | IOL1WAY | — | I2C1SEL | POSCMD1 | POSCMD0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | r = Reserved bit | |
|---|---|---|---|
| R = Readable bit | PO = Program-once bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value when device is unprogrammed | | ‘1’ = Bit is set | ‘0’ = Bit is cleared |

bit 23-16 Unimplemented: Read as ‘1’

bit 15 IESO: Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) enabled
0 = IESO mode (Two-Speed Start-up) disabled

**bit 14-13 WUTSEL1:WUTSEL0: Voltage Regulator Standby Mode Wake-up Time Select bits(1)**
**11 = Default regulator start-up time used**
**01 = Fast regulator start-up time used**
**x0 = Reserved; do not use**

**bit 12-11 SOSCSEL1:SOSCSEL0: Secondary Oscillator Power Mode Select bits(1)**
**11 = Default (high gain) mode**
**01 = Low-Power (low gain) mode**
**x0 = Reserved; do not use**

bit 10-8 FNOSC2:FNOSC0: Initial Oscillator Select bits
.
.
.
. .
. .
. .

bit 1-0 POSCMD1:POSCMD0: Primary Oscillator Configuration bits
11 = Primary oscillator disabled
10 = HS Oscillator mode selected
01 = XT Oscillator mode selected
00 = EC Oscillator mode selected

**Note 1: These bits are implemented only in devices with a major silicon revision level of B or later (DEVREV register value is 3042h or greater). Refer to Section 27.0 “Packaging Information” for the location and interpretation of product date codes.**

## 7. Module: Electrical Characteristics

Table 26-6 has been amended to add the following information (added text in **bold**; bold text in original removed for clarity).

**TABLE 26-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| Parameter No. | Typical(1) | Max | Units | Conditions | | |
| Power-Down Current (IPD): PMD Bits are Set, VREGS Bit is '0'(2) | | | | | | |
| DC62 | 8 | 16 | µA | -40°C | 2.0V(3) | RTCC + Timer1 w/32 kHz Crystal: ΔRTCC ΔITI32(5) |
| DC62a | 12 | 16 | µA | +25°C | | |
| DC62b | 12 | 16 | µA | +85°C | | |
| DC62j | 18 | 23 | µA | +125°C | | |
| DC62c | 9 | 16 | µA | -40°C | 2.5V(3) | |
| DC62d | 12 | 16 | µA | +25°C | | |
| DC62e | 12.5 | 16 | µA | +85°C | | |
| DC62k | 20 | 25 | µA | +125°C | | |
| DC62f | 10.3 | 18 | µA | -40°C | 3.3V(4) | |
| DC62g | 13.4 | 18 | µA | +25°C | | |
| DC62h | 14.2 | 18 | µA | +85°C | | |
| DC62i | 23 | 28 | µA | +125°C | | |
| **DC63** | **2** | **—** | **µA** | **-40°C** | **2.0V(3)** | **RTCC + Timer1 w/Low-Power 32 kHz Crystal (SOCSEL<1:0> = 01): ΔRTCC ΔITI32(5)** |
| **DC63a** | **2** | **—** | **µA** | **+25°C** | **2.0V(3)** | |
| **DC63b** | **6** | **—** | **µA** | **+85°C** | **2.0V(3)** | |
| **DC63c** | **2** | **—** | **µA** | **-40°C** | **2.5V(3)** | |
| **DC63d** | **2** | **—** | **µA** | **+25°C** | **2.5V(3)** | |
| **DC63e** | **7** | **—** | **µA** | **+85°C** | **2.5V(3)** | |
| **DC63f** | **2** | **—** | **µA** | **-40°C** | **3.3V(4)** | |
| **DC63g** | **3** | **—** | **µA** | **+25°C** | **3.3V(4)** | |
| **DC63h** | **7** | **—** | **µA** | **+85°C** | **3.3V(4)** | |

**Note 1:** Data in the Typical column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled high. WDT, etc., are all switched off.

**3:** On-chip voltage regulator disabled (DISVREG tied to VDD).

**4:** On-chip voltage regulator enabled (DISVREG tied to VSS). Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

**5:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

## 8. Module: Electrical Specifications

Table 26-10 of **Section 26.1 “DC Specifications”** has been amended to expand the definition of TVREG, as well as add the definition of VBG. The updated version is shown below. Changes are shown in **bold**, and bold from the original has been removed for clarity.

**TABLE 26-10: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

| Operating Conditions: -40°C < TA < +125°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristics | Min | Typ | Max | Units | Comments |
| | VRGOUT | Regulator Output Voltage | — | 2.5 | — | V | |
| | **VBG** | **Band Gap Reference Voltage** | **—** | **1.23** | **—** | **V** | |
| | CEFC | External Filter Capacitor Value | 4.7 | 10 | — | µF | Series resistance < 3 Ohm recommended; < 5 Ohm required. |
| | TVREG | Voltage Regulator Start-up Time | — | 10 | — | µs | **POR, BOR or when VREGS = 1** |
| | | | **—** | **25** | **—** | **µs** | **VREGS = 0, WUTSEL1:WUTSEL0 = 01(1)** |
| | | | **—** | **190** | **—** | **µs** | **VREGS = 0, WUTSEL1:WUTSEL0 = 11(2)** |
| | TPWRT | | — | 64 | — | ms | DISVREG = VDD |

**Note 1: Available only in devices with a major silicon revision level of B or later (DEVREV register value is 3042h or greater).**

**2: WUTSEL Configuration bit setting is applicable only in devices with a major silicon revision level of B or later. This specification also applies to all devices prior to revision level B whenever VREGS = 0.**

## REVISION HISTORY

Rev A Document (7/2007)

Initial release of this document. Includes Data Sheet Clarification 1 (Special Functions Registers), 2 (Pin Diagrams), 3 (Memory Organization), 4 (Flash Program Memory), 5 (Oscillator Configuration), 6 (I/O Ports), 7-11 (Output Compare), 12-13 (Special Peripheral Interface), 14-15 (Inter-Intergrated Circuit™ – $I^2C$™), 16-18 (Universal Asynchronous Receiver Transmitter – UART), 19-20 (10-Bit High-Speed A/D Converter), 21-22 (Special Features) and 23-26 (Electrical Characteristics).

Rev B Document (1/2008)

Removed all previous Data Sheet Clarifications and added new Data Sheet Clarification 1 (Electrical Characteristics).

Rev C Document (7/2008)

Added new Data Sheet Clarifications 2 (10-Bit High-Speed A/D Converter), 3 (I/O Ports), 4 (Oscillator Configuration), 5-6 (Special Features) and 7-8 (Electrical Specifications).

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