PIC32MX3XX/4XX Rev. B3 Silicon Errata

The PIC32MX3XX/4XX devices (Rev. B3) you received conform functionally to the corresponding device data sheet (DS61143), except for the anomalies described in this silicon errata document.

Any data sheet clarification issues related to the PIC32MX3XX/4XX family would be described in a data sheet errata document and made available on the Microchip web site, www.microchip.com.

Silicon errata listed here pertain only to PIC32MX3XX/4XX family devices with the following Device/Revision IDs.

TABLE 1: PERTINENT DEVICE/REVISION IDS

Part Number	Device ID	Revision ID
PIC32MX460F512L	0x78	0x409
PIC32MX460F256L	0x74	0x409
PIC32MX440F128L	0x6C	0x409
PIC32MX440F256H	0x52	0x409
PIC32MX360F512L	0x38	0x409
PIC32MX360F256L	0x34	0x409
PIC32MX340F256H	0x12	0x409
PIC32MX320F128H	0x0A	0x409
PIC32MX320F128L	0x2A	0x409
PIC32MX320F064H	0x06	0x409
PIC32MX320F032H	0x02	0x409

The Device ID and Revision ID of a PIC32MX3XX/4XX Rev. B3 device can be confirmed by performing a "Reset and Connect" operation to the device using MPLAB® REAL ICE™ in-circuit emulator with MPLAB IDE, version 8.0 or later.

"Reset and Connect" requires that a device is specified by clicking *Configure>Select Device*. A message that includes the Device ID Revision number of the device is displayed in the **Output** window to indicate successful connection to the device.

A Device ID Revision number acquired by this method can be resolved to the data in Table 1 by splitting the number, as demonstrated by the following example:

"Device ID Revision = 40938000" yields the following IDs:

Device ID = 0x38
Revision ID = 0x409

The errata described in this section will be addressed in future revisions of silicon.

1. Module: Device Reset

A Reset ($\overline{MCLR}$) Pulse that is shorter than 2 SYSCLK will not reset the device properly.

Work around

Ensure that the device is held in Reset for more than 2 SYSCLK to ensure proper device Reset operation.

2. Module: Device Reset

All Resets, except Power-On-Reset (POR), can cause a fail-safe clock monitor event (if enabled), when the duration of the Reset pulse exceeds the clock period of the internal fail-safe clock reference clock–31 kHz.

Work around

If long Reset pulses are anticipated, ignore or disable fail-safe clock monitor events.

3. Module: Software Device Reset

Attempting to perform a software device Reset with PBDIV set to 1:1 and SYSCLK less than 1 MHz will not reset the device properly.

Work around

Work around 1: Change PBDIV before performing a software Reset.

Work around 2: Set SYSCLK to a value that is greater than 1 MHz.

4. Module: External Voltage Regulator Mode

A V_{DDCORE} voltage less than 1.75V will cause the CPU to reset when using an external core voltage supply.

Work around

Work around 1: Use the internal voltage regulator.

Work around 2: Use an external 1.8V regulator which has a regulation specification of <= 2.5%. The Microchip TC1055-1.8VCT713 Low Drop-Out regulator (LDO), or an equivalent, is recommended.

5. Module: ADC

When running the A/D converter in Internal Reference mode, the gain error is 3-4 LSb and the offset error is 1-2 LSb across voltage and speed.

Work around

Use in-system calibration and software techniques to compensate for these errors.

6. Module: Bus Matrix Registers

The BMXDUDBA, BMXDUPBA, and BMXPUPBA registers can be set to values that are outside of the device's actual memory-size limit.

Work around

Do not write values greater than the specified memory size of the device to the Bus Matrix registers. Ensure upper bits of the registers remain clear ('0').

7. Module: Clock Failure Event

After a clock failure event, any write to OSCCON erroneously clears fail-safe condition and attempts to switch to a new clock source that is specified by NOSC bits in OSCCON register.

Work around

After a clock failure event, do the following:

1. Write '000' to NOSC bits in OSCCON register to select the Fast RC oscillator. This will ensure that an erroneous clock switch selects the known good on-chip Fast RC oscillator.
2. Modify OSCCON register with any value your application requires.

8. Module: DMA Pattern Match Mode

In Pattern Match mode the DMA will generate up to 3 additional byte writes to the destination address–after the Pattern Detection event has occurred–when performing transfers with the DCHxSSIZ set to greater than 1.

Work around

Use one of the following three work-arounds:

Work around 1: The destination buffer needs to be large enough to accommodate the extra bytes (up to 3 extra bytes).

Work around 2: Set the destination size register to 1.

Work around 3: Set the source size register to 1.

9. Module: Output Compare in PWM Mode

The Output Compare module in PWM mode outputs a high of period register (PRx) length when attempting to use PWM values of 0x00 followed by a 0x01.

Work around

Do not use a PWM value of 0x01.

10. Module: Parallel Master Port (PMP)

In PMP Slave 4B Buffer mode, if underflow Status bit OBF (PMSTAT<6>) is cleared at the same time a PMP read is attempted, the PMP could get incorrect data.

Work around

The CPU can read the underflow flag OBUF and set/clear an I/O pin for the external master device to read. The state of the pin should indicate to the external master device that an underflow has occurred and no additional reads should occur until the underflow status has been cleared by the CPU.

11. Module: Ports

The SET/CLR/INV registers for port SFRs use latched value (LATCH) to perform single-cycle hardware read-modify-write operation.

Work around

Use one of the following two work-arounds:

Do not use SET/CLR/INV operations on a port if it contains one pin (or more) that are configured as a bidirectional digital pin.

Before performing SET/CLR/INV operations on a PORT containing a bidirectional digital pin, reset the corresponding LATCH bit to desired/fail-safe value.

12. Module: Timer1, 2, 3, 4, 5

TMRx register stays at zero for two timer clock cycles when the PRx register is 0x0000.

Work around

None.

13. Module: Timer1, 2, 3, 4, 5

Writes to SET/CLR/INV registers for TMRx and PRx produce incorrect results.

Work around

Use TMRx and PRx registers to manipulate bits.

14. Module: Timer1

Timer1 prescaler may not be reset correctly when it is used with a slow external clock. This can occur when the timer is disabled, and then re-enabled. The result could be a spurious count in the prescaler.

Work around

None.

15. Module: UART Hardware Handshake Mode

The CTS pin does not deassert until at least 2 bytes are free in the UART FIFO.

Work around

The UART TXREG must be read at least 2 times to rearm the hardware handshaking lines.

16. Module: Watchdog Timer (WDT)

An incorrect WDT Time-out Reset may occur when both of following conditions are present:

1. WDT is enabled.
2. Either a $\overline{\text{MCLR}}$ (EXTR) or Software Reset (SWR) occurs just before WDT is about to expire.

Work around

To detect incorrect WDT Time-out Reset, always confirm that only WDTO bit is set in RCON register. If EXTR, SWR, or any other Reset bits are set, it indicates that an incorrect WDT has occurred.

17. Module: DMA Channel Abort

DMA Channel Abort on a channel that is not currently active may have unintended effects on other active channels.

Work around

1. Suspend the channel, rather than abort, by clearing the channel enable bit DCHxCON<CHEN>.
2. Wait until other DMA channels complete before issuing the abort.

18. Module: Oscillator

The Primary Oscillator Circuit (POSC), when using XT/XTPLL/HS/HSPLL modes, does not operate over the temperature range that is listed as item D5 in the device data sheet. Operation range without the workaround is limited to -40°C to +60°C.

Work around

Install a 4.1 M Ohm resistor in parallel with the crystal. This allows operation across the temperature range that is listed in the data sheet.

19. Module: PMP

The WAITE field in PMMODE<1:0> does not add a wait state to PMP Master reads when it is programmed to the value '01'. The WAITE field allows wait states to be added to the end of PMP read/write operations. This field is intended to add the following wait clocks after the read operation completes:

00 – no wait states
01 – 1 wait state
10 – 2 wait states
11 – 3 wait states

Current behavior is the following:

00 – no wait states
01 – no wait states
10 – 2 wait states
11 – 3 wait states

Work around

This erratum only applies to PMP Master read operations. PMP writes work correctly. Use another wait state control value that is allowed for the attached device.

APPENDIX A: REVISION HISTORY

Revision A (02/2008)

Initial release of this document.

Revision B (04/2008)

Oscillator temperature issue was added. Flash Program Memory 500ns delay requirement is now classified as architectural behavior. Added PMP WAITE behavior.

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