PIC32MX Rev. B2 ES Silicon Errata

PIC32MX (Rev. B2 ES) Silicon Errata

The PIC32MX devices (Rev. B2 ES) you received were found to conform to the specifications and functionality described in the following documents:

- "*PIC32MX Family Data Sheet*" (DS61143)
- *"PIC32MX Family Reference Manual"*

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC32MX360F512L
- PIC32MX360F256L
- PIC32MX340F256H
- PIC32MX320F128H
- PIC32MX320F128L
- PIC32MX320F064H
- PIC32MX320F032H

PIC32MX Rev. B2 ES silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® REAL ICE™ in-circuit emulator with MPLAB IDE v8.0 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*.

The errata described in this section will be addressed in future revisions of silicon.

1. Module: Device Reset

A Reset ($\overline{MCLR}$) Pulse shorter than 2 SYSCLK will not properly reset the device.

Work around

Ensure the device is held in Reset for more than 2 SYSCLK to insure proper device Reset operation.

2. Module: Device Reset

All Resets except Power-On-Reset (POR) can cause fail-safe clock monitor event, if enabled, if the duration of Reset pulse exceeds the clock period of the internal fail-safe clock reference clock of 31 kHz.

Work around

Ignore or disable fail-safe clock monitor event, if your system may experience long Reset pulse.

3. Module: Software Device Reset

Attempting to perform a software device Reset with PBDIV set to 1:1 and SYSCLK less than 1 MHz will not properly reset the device.

Work around

Work around 1: Change PBDIV before preforming a software Reset.

Work around 2: Set SYSCLK greater than 1 MHz.

4. Module: External Voltage Regulator Mode

A V_{DDCORE} voltage less than 1.75V will cause the CPU to reset when using external core voltage supply.

Work around

Work around 1: Use the internal voltage regulator.

Work around 2: Use an external regulator which can ensure regulation above 1.75V.

5. Module: ADC

When the ADC is in operation, the current channel is shorted to VREF during the conversion period (12TAD) after sampling. The impact on high-impedance sources is that they may not have time to recover between conversions. The impact on low-impedance sources is a high current draw which may damage either the source or the device.

Work around

Place a 5k resistor between the device and any external capacitance on the board to limit current draw.

6. Module: ADC

When running the ADC in Internal Reference mode, the gain error is 3-4 LSb and the offset error is 1-2 LSb across voltage and speed.

Work around

Use in-system calibration and software techniques to compensate for these errors.

7. Module: Bus Matrix Registers

The BMXDUDBA, BMXDUPBA and BMXPUPBA registers can be set to values outside the device's actual memory size limit.

Work around

Do not write values greater than the specified memory size of the device to the Bus Matrix Registers. Ensure upper bits of the registers remain clear ('0').

8. Module: Clock Failure Event

After a clock failure event, any write to OSCCON erroneously clears fail-safe condition and attempts to switch to a new clock source specified by NOSC bits in OSCCON register.

Work around

After a clock failure event, do the following:

1. Write '000' to NOSC bits in OSCCON register to select the Fast RC oscillator. This will ensure that an erroneous clock switch selects the known good on-chip Fast RC oscillator.
2. Modify OSCCON register with any value your application requires.

9. Module: DMA pattern Match Mode

In Pattern Match mode the DMA will generate up to 3 additional byte writes to the destination address after the Pattern Detection event has occurred when performing transfers with the DCHxSSIZ set to greater than 1.

Work around

There are three possible work-arounds:

Work around 1: The destination buffer needs to be large enough to accommodate the extra bytes (up to 3 extra bytes).

Work around 2: Set the destination size register to 1.

Work around 3: Set the source size register to 1.

10. Module: Output Compare in PWM Mode

The Output Compare module in PWM mode outputs a high of period register (PRx) length when attempting to use PWM values of 0x00 followed by a 0x01.

Work around

Do not use a PWM value of 0x01.

11. Module: Prefetch Cache

If the Predictive Prefetch Cache Enable bits (PREFEN<1:0>) in CHECON register are non-zero, improper processor behavior may occur during a rare boundary condition. This condition occurs only when predictive prefetch is enabled, and can occur in both cacheable and non-cacheable memory areas. The prefetch buffer can be overwritten by the "next" 16-bytes of instructions causing invalid instruction execution. This may cause an invalid instruction fault, or execution of a wrong instruction.

Work around

Make sure that the PREFEN field in CHECON is programmed to 00. The cache is still used, although predictive prefetching will be disabled.

12. Module: PMP

In PMP Slave 4B Buffer mode, if underflow Status bit OBF (PMSTAT<6>) is cleared at the same time a PMP read is attempted, it could get incorrect data.

Work around

The CPU can read the underflow flag, OBUF and set/clear an I/O pin for the external master device to read. The state of the pin should indicate to the external master device that an underflow has occurred and no additional reads should occur until the underflow status has been cleared by the CPU.

13. Module: PORTs

The SET/CLR/INV registers for PORT SFRs use latched value (LATCH) to perform single-cycle hardware read-modify-write operation.

Work around

Do not use SET/CLR/INV operations on a PORT if it contains at least one pin configured as bidirectional digital pin.

OR before performing SET/CLR/INV operations on a PORT containing bidirectional digital pin, reset the corresponding LATCH bit to desired/fail-safe value.

14. Module: Timer1, 2, 3, 4, 5

TMRx register stays at zero for two timer clock cycles when the PRx register is 0x0000.

Work around

None.

15. Module: Timer1, 2, 3, 4, 5

Writes to SET/CLR/INV registers for TMRx and PRx produce incorrect results.

Work around

Use TMRx and PRx registers to manipulate bits.

16. Module: Timer1

Timer1 prescaler has the possibility of not getting reset correctly when used with a slow external clock. This can occur when the timer is disabled, then re-enabled, possibly resulting in a spurious count in the prescaler.

Work around

None.

17. Module: UART Hardware Handshake Mode

The CTS pin does not deassert until at least 2 bytes are free in the UART FIFO.

Work around

The UART TXREG must be read at least 2 times in order to rearm the hardware handshaking lines.

18. Module: Watchdog Timer (WDT)

An incorrect WDT Time-out Reset may occur, if all of following conditions are present:

1. WDT is enabled.
2. Either $\overline{\text{MCLR}}$ (EXTR) or Software Reset (SWR) occurs just before WDT is about to expire.

Work around

To detect incorrect WDT Time-out Reset, always confirm that only WDTO bit is set in RCON register. If EXTR, SWR or any other Reset bits are set, it indicates that an incorrect WDT has occurred.

19. Module: DMA Channel Abort

DMA Channel Abort on a channel that is not currently active may have unintended effects on other active channels.

Work around

1. Suspend the channel rather than abort by clearing the channel enable bit (DCHxCON.CHEN).
2. Wait until other DMA channels complete before issuing the abort.

20. Module: Flash Program Memory

NVM registers must not be written immediately after a programming operation is complete. When a NVM operation completes, NVMWR bit (NVMCON<15>) switches state from a 1 to a 0 indicating that another NVM operation may be started. However, there is a period of 2 internal FRC clocks after this transition where a write to NVMCON may not work correctly. Since the internal FRC clock is 8 MHz, and the system clock may be much faster, care must be taken to insure that the correct delay is met.

Work around

Wait at least 500 ns after seeing a '0' in NVMCON<15> before writing to any NVM registers.

APPENDIX A: REVISION HISTORY

Revision A (11/2007)

Initial release of this document.

Revision B (1/2008)

Revised existing and added new modules.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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