SED1351

GRAPHICS LCD CONTROLLER

■ DESCRIPTION

The SED1351F is a graphics LCD controller capable of controlling medium to large resolution displays. It transfers data from MPU to external frame buffer RAM and converts this data to display signals for LCD drivers. The SED1351F can display images with 4 gray shades and support display duty cycle as high as 1/1024.

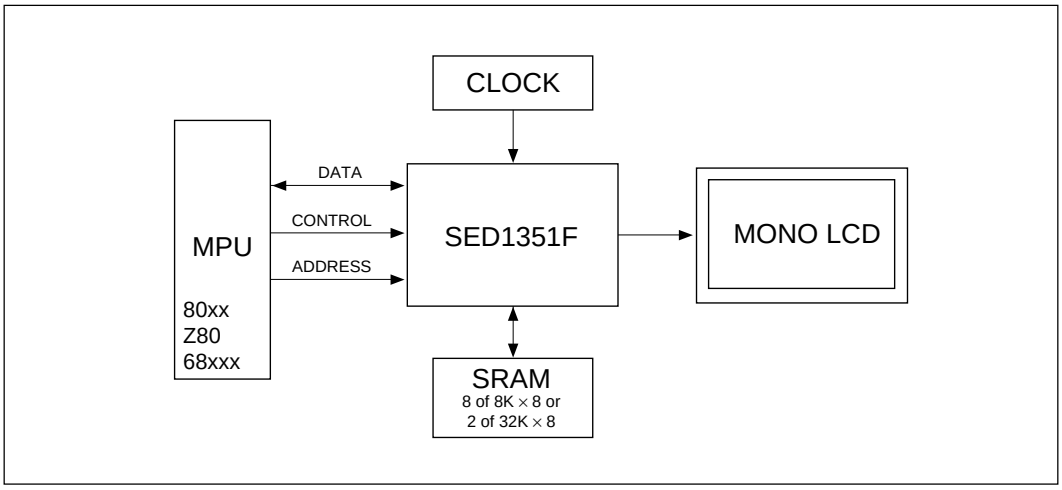
The SED1351F is designed to achieve high efficiency and data throughput to the LCD. It has a cycle steal mode which allows MPU to access frame buffer RAM without interfering with the display operation. The SED1351F can directly interface with up to eight 64K-bit SRAMs or two 256K-bit SRAMs.

The SED1351F can operate with either 5V or 3V power supply. The 5V version chip is the SED1351F0A and the 3V version chip is the SED1351FLB.

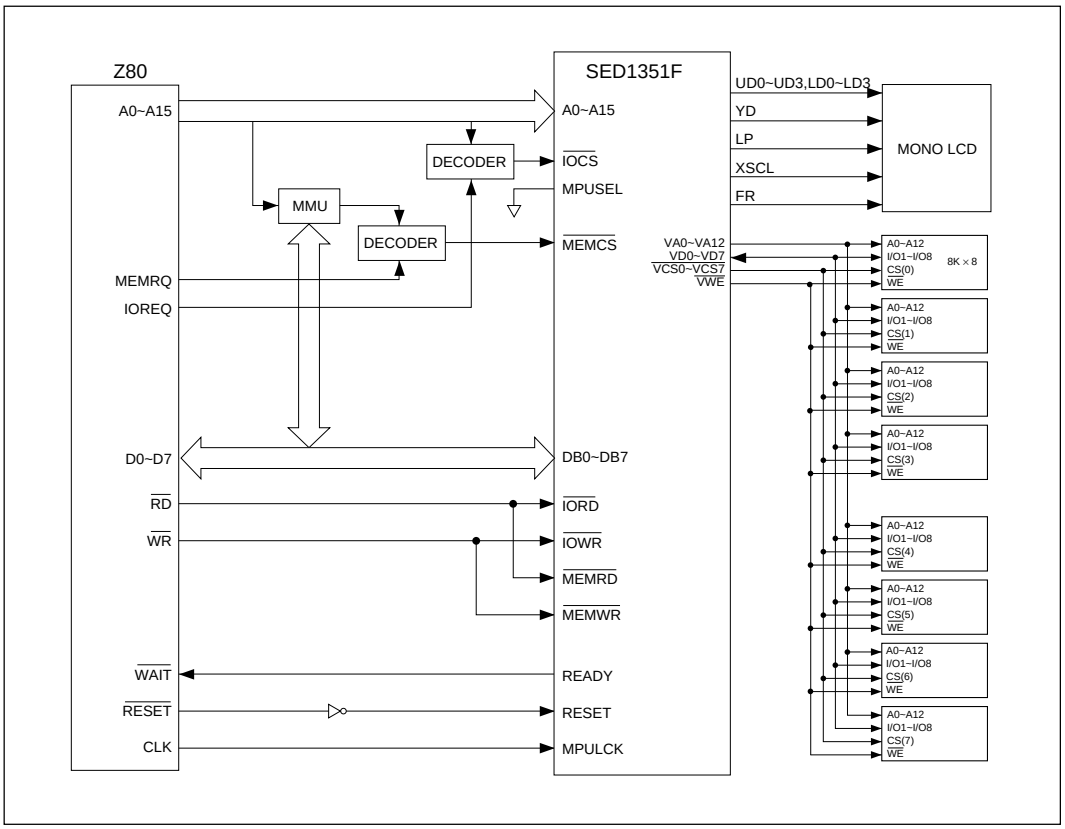
■ FEATURES

- Low-power CMOS technology
- 8-bit or 16-bit MPU data interface
- Direct interface with 80xx, Z80 and 68xxx MPU
- 4- or 8-bit panel data bus for single panel and 4-bit bus for dual panel
- Support logical OR of layers and panel division
- Smooth vertical scrolling
- Virtual screen display up to 1024
- Binary mode (on/off only) generates black & white images
- Gray mode (on/off and two gray steps) generates images with 4 gray shades
- Maximum number of rows
  Binary mode 2048
  Gray mode 1024
- Maximum number of rows:
  Single panel 1024
  Dual panel 2048
- Maximum display sizes when 64K-byte SRAMs are used:
  Binary mode ..... 2048 × 256 / 1024 × 512
  Gray mode ..... 1024 × 256 / 512 × 512
- Available models:
  $SED1351F_{0A}$ ..... 5V, QFP5-100 pin
  $SED1351F_{LB}$ ..... 3V,QFP15-100 pin

■ SYSTEM BLOCK DIAGRAM

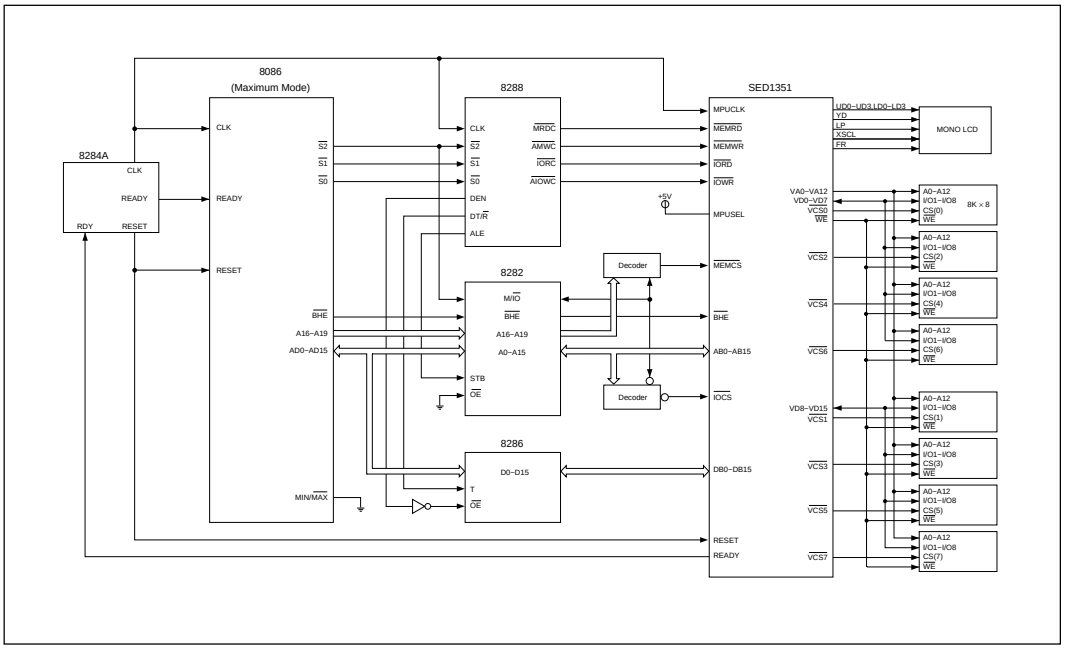


■ INTERFACE WITH 8-BIT MPU (Z-80) AND 64K-BIT SRAM (8 of 8K x 8)



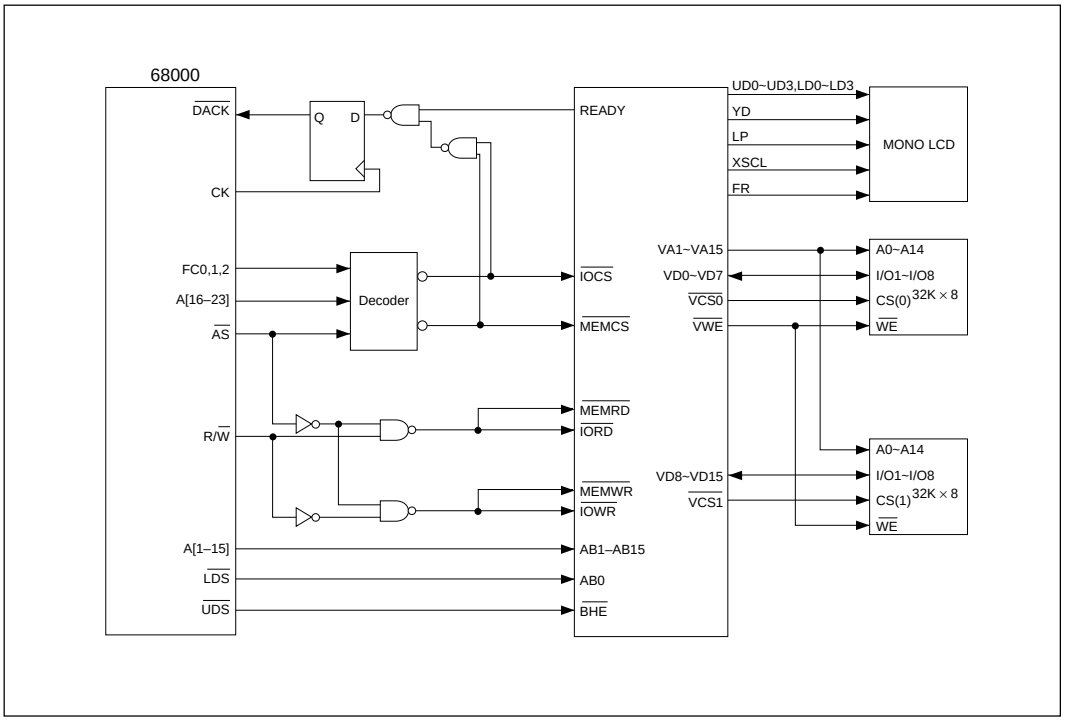
Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (8086) AND 64K-BIT SRAM (8 of 8K x 8)



Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (68000) AND 256K-BIT SRAM (2 of 32K x 8)

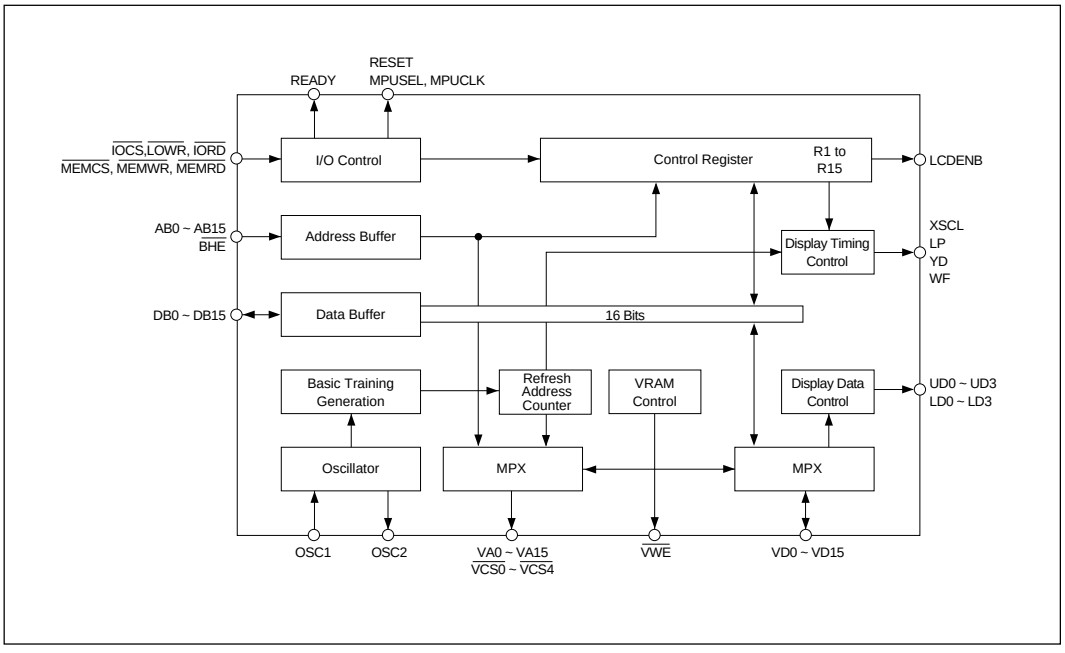


Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

Display RAM	Maximum Display Size				SRAM Type	CPU Interface	SRAM Interface
	Monochrome		4 Grayscale				
	X	Y	X	Y			
8K	256	256	256	128	1 of 8K × 8	8 bit	8 bit
16K	512	256	256	256	2 of 8K × 8	8 bit 16 bit	8 bit 16 bit
24K	512	384	384	256	3 of 8K × 8	8 bit	8 bit
32K	512	512	512	256	4 of 8K × 8	8 bit 16 bit	8 bit 16 bit
					1 of 32K × 8	8 bit	8 bit
48K	768	512	512	384	6 of 8K × 8	8 bit 16 bit	8 bit 16 bit
56K	896	512	512	448	7 of 8K × 8	8 bit	8 bit
64K	1024	512	512	512	8 of 8K × 8	8 bit 16 bit	8 bit 16 bit
					2 of 32K × 8	8 bit 16 bit	8 bit 16 bit

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● SED1351F0A

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	V_{SS}–0.3 to 7.0	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
Output current/pin	I_O	±10	mA
Power dissipation	P_D	200	mW
Supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}		–20	—	75	°C

○ **DC Characteristics (F0A)**

(Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I_{DDS}	$V_{IN} = V_{DD}$, V_{DD} = Max, V_{SS}, $I_{OH} = I_{OL} = 0$	—	—	100	µA
Input leakage current (Type 1)	I_{LI}	V_{DD} = 5.5V, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–10	—	10	µA
High level input voltage 1 (OSC1)	V_{IH1}	V_{DD} = 5.5V	3.5	—	—	V
Low level input voltage 1 (OSC1)	V_{IL1}	V_{DD} = 4.5V	—	—	1.0	V
High level input voltage 2 (Type 2)	V_{IH2}	V_{DD} = 5.5V	2.0	—	—	V
Low level input voltage 2 (Type 2)	V_{IL2}	V_{DD} = 4.5V	—	—	0.8	V
High level input voltage 3 (Type 3)	V_{T+}	V_{DD} = 5.5V	4.0	—	—	V
Low level input voltage 3 (Type 3)	V_{T-}	V_{DD} = 4.5V	—	—	0.8	V
Hysteresis voltage (Type 3)	V_H	V_{DD} = 5V	0.3	—	—	V
High level output voltage 1 (Type 4)	V_{OH1}	V_{DD} = 4.5V, I_{OH} = –2mA, I_{OL} = 6mA	V_{DD} – 0.4	—	—	V
Low level output voltage 1 (Type 4)	V_{OL1}		—	—	V_{SS} + 0.4	V
High level output voltage 2 (OSC2)	V_{OH2}	V_{DD} = 4.5V, I_{OH} = –50µA, I_{OL} = 50µA	V_{DD} – 0.4	—	—	V
Low level output voltage 2 (OSC2)	V_{OL2}		—	—	V_{SS} + 0.4	V

Note:

Type 1. $\overline{\text{MEMCS}}$, $\overline{\text{MEMWR}}$, $\overline{\text{MEMRD}}$, $\overline{\text{IOCS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, MPUCLK, AB0 ~ AB15, $\overline{\text{BHE}}$, MPUSEL, RESET, OSC

Type 2. $\overline{\text{MEMCS}}$, $\overline{\text{MEMWR}}$, $\overline{\text{MEMRD}}$, $\overline{\text{IOCS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, MPUCLK, AB0 ~ AB15, $\overline{\text{BHE}}$, DB0 ~ DB15, VD0 ~ VD15

Type 3. MPUSEL, RESET

Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, $\overline{\text{VCS0}}$ ~ $\overline{\text{VCS4}}$, VD0 ~ VD15, $\overline{\text{VWE}}$, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

- **SED1351FLA**
- **Absolute Maximum Ratings**

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	V_{SS}–0.3 to 7.0	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.5	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.5	V
Output current/pin	I_O	±24	mA
Power dissipation	P_D	200	mW
Supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	–65 to 150	°C

- **Recommended Operating Conditions**

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		2.7	—	3.6	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}		–20	—	75	°C

○ **DC Characteristics (FLB)**

(Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I_{DDS}	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = MAX, $I_{OH} = I_{OL} = 0$	—	—	30	µA
Input leakage current (Type 1)	I_L	V_{DD} = MAX, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–1	—	1	µA
High level input voltage 1 (OSC1)	V_{IH1}	V_{DD} = MAX	0.7V_{DD}	—	—	V
Low level input voltage 1 (OSC1)	V_{IL1}	V_{DD} = MIN	—	—	0.2V_{DD}	V
High level input voltage 2 (Type 2)	V_{IH2}	V_{DD} = MAX	0.7V_{DD}	—	—	V
Low level input voltage 2 (Type 2)	V_{IL2}	V_{DD} = MIN	—	—	0.2V_{DD}	V
High level input voltage 3 (Type 3)	V_{T+}	V_{DD} = MAX	0.8V_{DD}	—	—	V
Low level input voltage 3 (Type 3)	V_{T-}	V_{DD} = MIN	—	—	0.2V_{DD}	V
Hysteresis voltage (Type 3)	V_H	V_{DD} = TYP	0.3	—	—	V
High level output voltage 1 (Type 4)	V_{OH1}	V_{DD} = MIN, I_{OH} = –1.5mA, I_{OL} = 3mA	V_{DD} – 0.3	—	—	V
Low level output voltage 1 (Type 4)	V_{OL1}		—	—	V_{SS} + 0.3	V
High level output voltage 2 (OSC2)	V_{OH2}	V_{DD} = MIN, I_{OH} = –50µA, I_{OL} = 50µA	V_{DD} – 0.4	—	—	V
Low level output voltage 2 (OSC2)	V_{OL2}		—	—	V_{SS} + 0.4	V

Note:

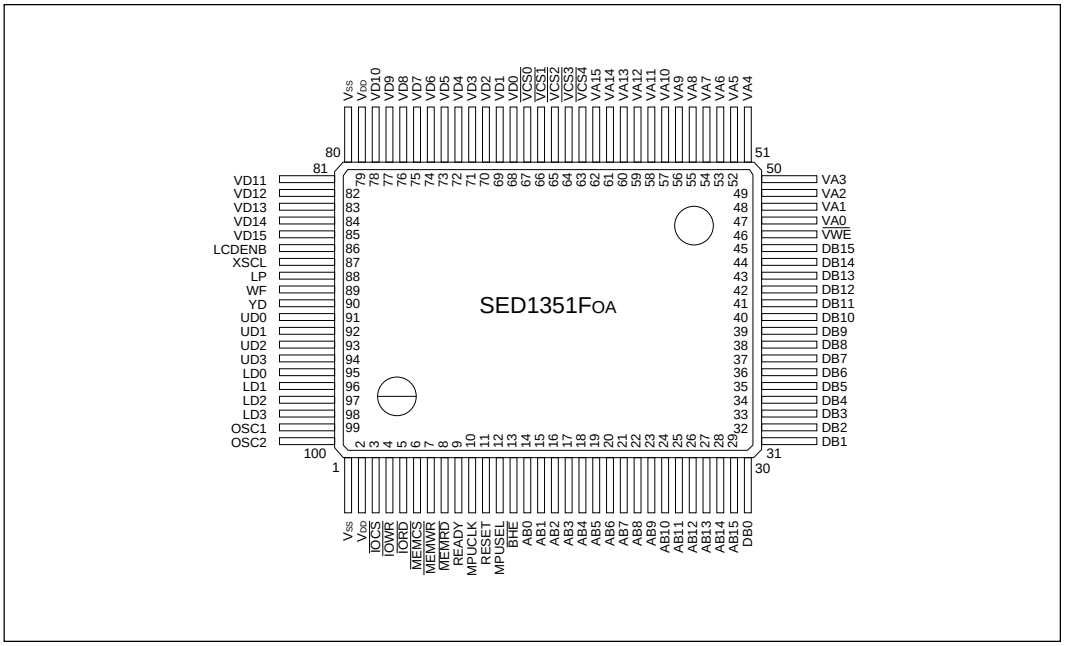
Type 1. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, MPUSEL, RESET, OSC

Type 2. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, DB0 ~ DB15, VD0 ~ VD15

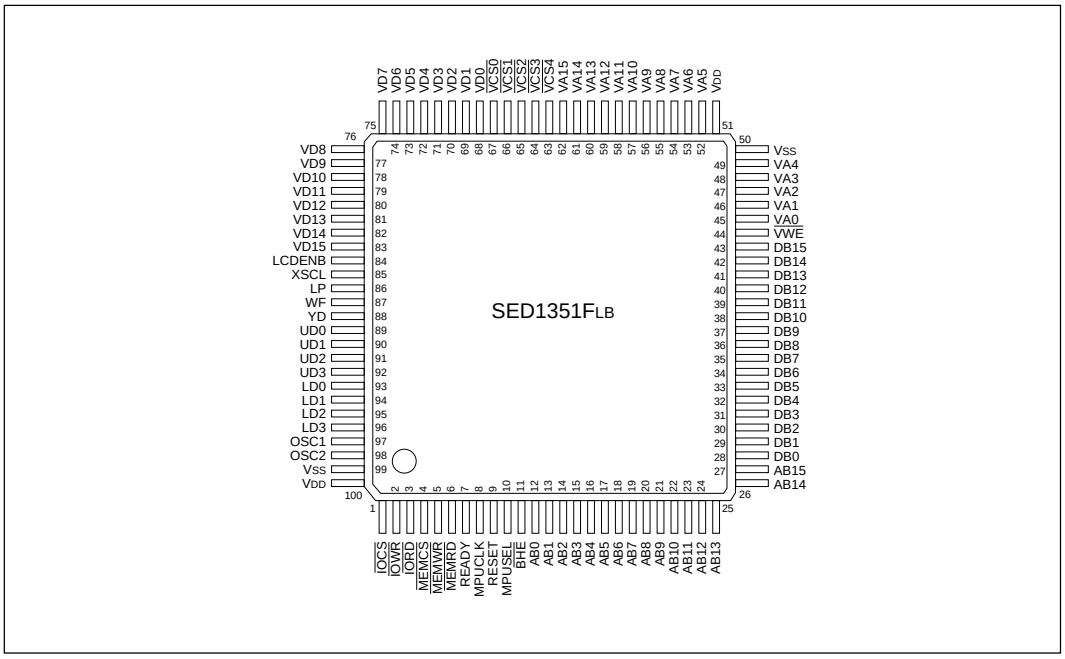
Type 3. MPUSEL, RESET

Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, $\overline{VCS0}$ ~ $\overline{VCS4}$, VD0 ~ VD15, $\overline{VWE}$, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

■ PIN CONFIGURATION (F0A)



■ PIN CONFIGURATION (FLB)



■ PIN DESCRIPTION

1. System Connector Terminals (at MPU)

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
DB0 to DB15	I/O	30 to 45	28 to 43		These pins are interfaced with the MPU data bus. When using an 8-bit MPU, connect DB8 to DB15 to VDD.
AB0 to AB15	I	14 to 29	12 to 27		These pins are interfaced with the MPU address bus. If multiplexed address signals are used, connect them via latch circuits. A control register is selected by AB0 to AB3. Correspondence of the MPU address bus to the VRAM address bus is such that ABi = VAi (where i is a pin number).
$\overline{BHE}$	I	13	11		This signal is a bus high enable signal where a 16-bit MPU is used. It goes "L" (low) when an odd address is encountered. When using an 8-bit MPU configuration, connect the BHE pin to VDD.
$\overline{IOCS}$	I	3	1		This pin selects a control register contained in the SED1351. It is "L" active, and must be assigned to MPU I/O space.
$\overline{IOWR}$	I	4	2		This signal is used for writing data into a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an OUT instruction from the MPU.
$\overline{IORD}$	I	5	3		This signal is used for reading data from a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an IN instruction from the MPU.
$\overline{MEMCS}$	I	6	4		This signal is used for selecting VRAM. It is "L" active, and must be assigned to MPU memory space.
$\overline{MEMWR}$	I	7	5		This signal is used for writing data to the VRAM. It is "L" active, and must go "L" when it encounters a memory write instruction from the MPU.
$\overline{MEMRD}$	I	8	6		This signal is used for reading data from the VRAM. It is "L" active, and must go "L" when it encounters a memory read instruction from the MPU.
READY	O	9	7		This signal requests the MPU to wait. It goes "L" by the falling edge of IOCS or MEMCS. It goes "H" by the rising edge of MPUCLK after completion of the SED1351 internal processing. Since READY is not a tri-state pin, it needed not be pulled up and must be connected directly to the READY (WAIT) terminal of the MPU.
MPUCLK	I	10	8		This pin accepts an MPU clock. The MPU wait state is cleared by the rising edge of MPUCLK.
MPUSEL	I	12	10		This signal is connected to either VDD or VSS for selection of an MPU. MPUSEL = V_{SS} 8-bit MPU (e.g., Z80, V20, i8088) MPUSEL = V_{DD} 16-bit MPU (e.g., V30, i8086)
RESET	I	11	9		The MPU reset signal comes to this pin. It is "H" active, and initializes a control register.

Combinations of Control Pins

$\overline{IOCS}$	$\overline{IOWR}$	$\overline{IORD}$	$\overline{MEMCS}$	$\overline{MEMWR}$	$\overline{MEMRD}$	Operation
1	*	*	1	*	*	Invalid
0	0	1	1	1	1	Write to control register
0	1	0	1	1	1	Read from control register
1	1	1	0	0	1	Write to VRAM
1	1	1	0	1	0	Read from VRAM

Note: Any combination other than those listed above will cause a system error.

1 = "H" (high)

0 = "L" (low)

* = Don't care

2. VRAM Connector Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
VD0 to VD15	I/O	68 to 78, 81 to 85	68 to 83		These pins are interfaced with the VRAM data bus. For a 16-bit MPU configuration, VD0 to VD7 must be connected to even addresses, and VD8 to VD15 to odd addresses. For an 8-bit configuration, VD8 to VD15 must be connected to VDD.
VA0 to VA12	O	47 to 59	45 to 49, 52 to 59		These pins are interfaced with the VRAM address bus and chip select pins.
VA13/$\overline{VCS7}$ to VA15/VCS5	O	60 to 62	60 to 62		The SED1351 has chip select pins that can directly control eight 64K SRAMs (8K bytes each) or two 256K SRAMs (32K bytes) in the 64K VRAM space. See Technical Manual for details.
$\overline{VCS0}$ to $\overline{VCS4}$	O	67 to 63	67 to 63		
$\overline{VWE}$	O	46	44		This signal is used for writing data to the VRAM. It is "L" active, and must be connected to the WE pin of the VRAM.

3. Oscillator Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
OSC1	I	99	97		The OSC1 (input) and OSC2 (output) pins generate clocks for internal operation. They allow crystal oscillation and external clock input.
OSC2	O	100	98		

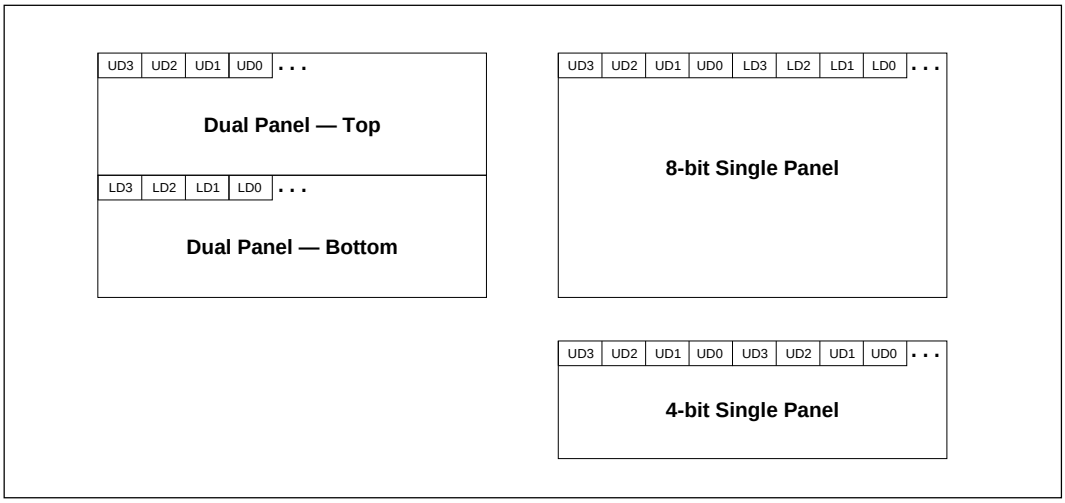
4. Power Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
V_{DD}	—	2, 79	51, 100		The power supply pins include two V_{DD}s and two V_{SS}s. Apply +5V or +3V to V_{DD} and 0V to V_{SS}. A capacitor (4.7 µF or more) must be connected near each pair of V_{DD}/V_{SS} pins.
V_{SS}	—	1, 80	50, 99		

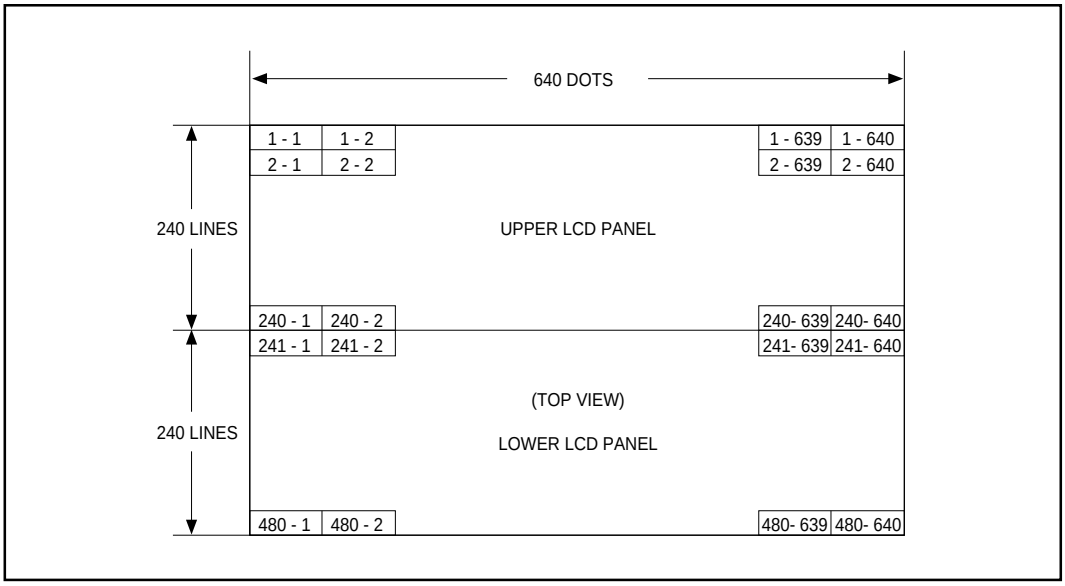
5. LCD Connector Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
UD0 to UD3	I/O	91 to 94	89 to 92		LCD display data. UD0 to UD3 are the upper panel display data in the signal panel or double panel drive panel mode. LD0/UD4 to LD3/UD7 are the lower panel display data in the double panel drive mode. UD0 to UD3, and LD0/UD4 to LD3/UD7 are used for 8-bit data transfer in the single panel drive mode.
LD0/UD4 to LD3/UD7	O	95 to 98	93 to 96		
XSCL	O	87	85		This single is a shift clock for display data transfer. Take the UD0 to UD3, LD0/UD4 to LD3/UD7 display data into LCDs by the falling edge of XSCL.
LP	O	88	86		This pin provides both a display data latch pulse and a scan signal transfer clock. Upon completion of transferring the LCD data on one line, display data can be latched or a scan signal transferred by the falling edge of LP.
WF	O	89	87		This pin provides a frame signal used for LCD AC driving.
YD	O	90	88		This pin provides a scanning line start pulse. The signal is “H” active. Allow the scanning line drive IC to take in YD by the falling edge of LP. The SED1351 has two lines of retracing; if two scanning line drive ICs are cascade-connected for the upper and lower panels in the double panel drive mode, two lines must be provided between the upper and lower scanning line drive outputs.
LCDENB	O	86	84		This pin provides the data which is set in bit 1 (D1) of the mode register (R1). LCDENB goes “L” when the system is reset; it can be effectively used for LCD power control.

Illustrated below are the display data which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:

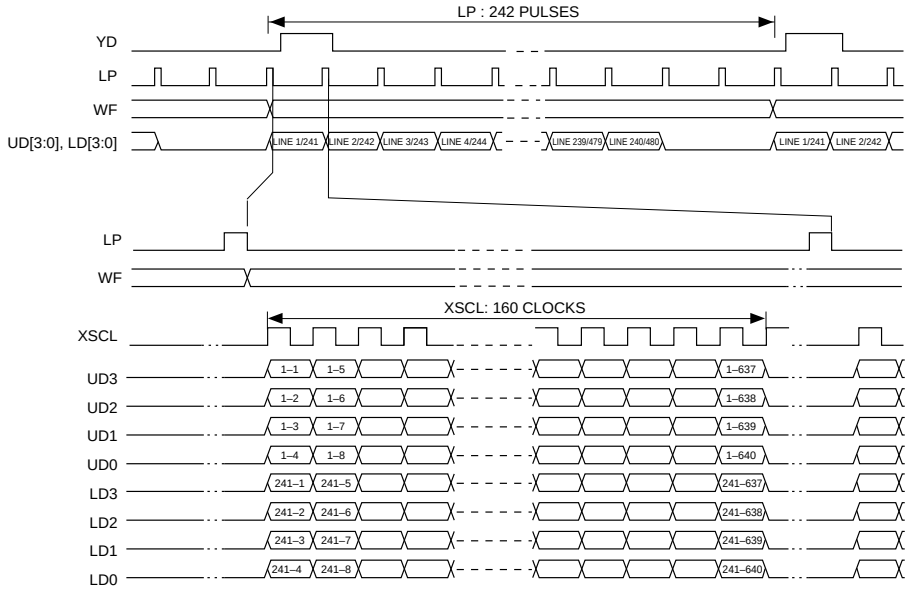


■ LCD PANEL PIXELS



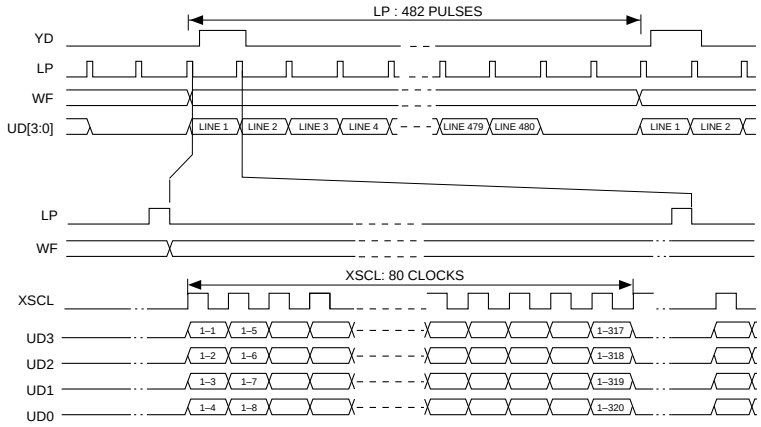
■ MONOCHROME LCD PANEL INTERFACE

8-Bit Dual Monochrome Panel (i.e. 640 × 480)

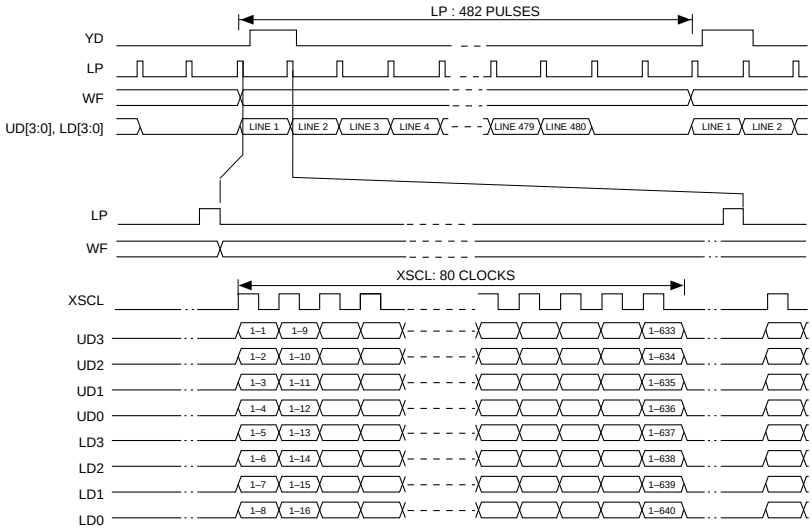


■ MONOCHROME LCD PANEL INTERFACE

4-Bit Single Monochrome Panel (i.e. 320 × 480)



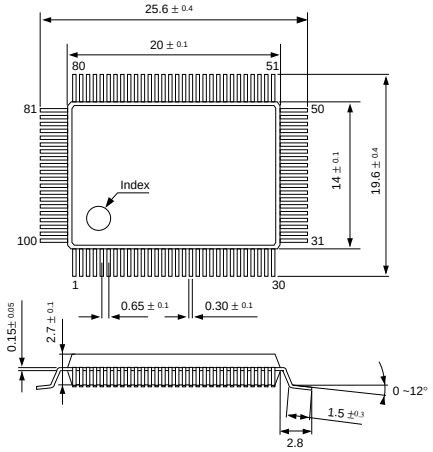
8-Bit Single Monochrome Panel (i.e. 640 × 480)

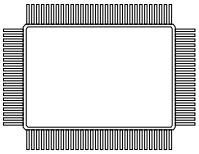


■ PACKAGE DIMENSIONS

● SED1351F0A

QFP5-100pin Unit: mm

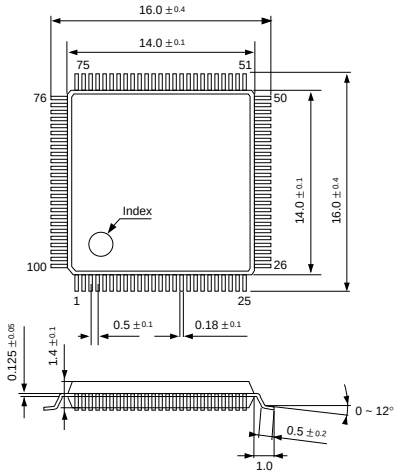


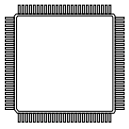


Actual Size

● SED1351FLB

QFP15-100pin Unit: mm





Actual Size

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