"Soft" Turn-Off Feature

Products with Feature: HCPL-316J, ACPL-331J, ACPL-332J

Application Note 5315

Introduction

Avago's Gate Optocoupler "Soft" turn-off feature is used to increase the reliability of an application during short-circuit or over-current period. This feature works after the DESAT protection is activated, which provides protection for transistor switches (IGBT / MOSFET) against short-circuit and over-current events. Desaturation protection circuit is illustrated in Figure 1. With "Soft" turn-off feature, the gate voltage will be reduced slowly in order to reduce IGBT current. This is a two stage turn-off system. It will slowly discharge the IGBT gate to prevent fast change in drain current. The "Soft" IGBT turn-off method will avoid over-voltage spike across the IGBT due to lead and wire inductances.

How does Desaturation Protection and "Soft" Shut-down work? This is illustrated in Figure 2.

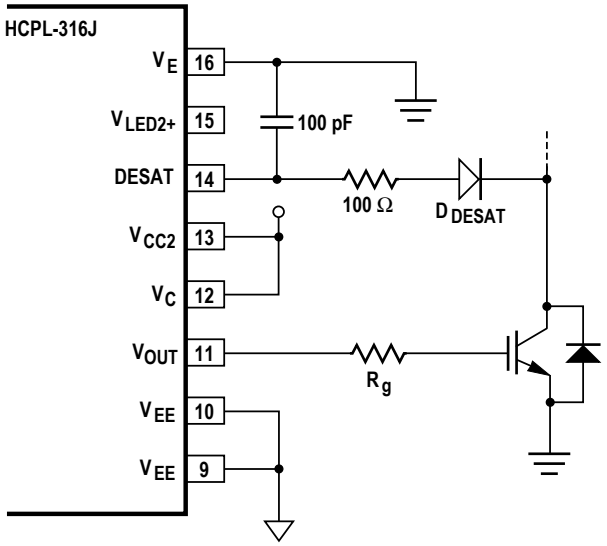

Figure 1. Desaturation Protection using HCPL-316J

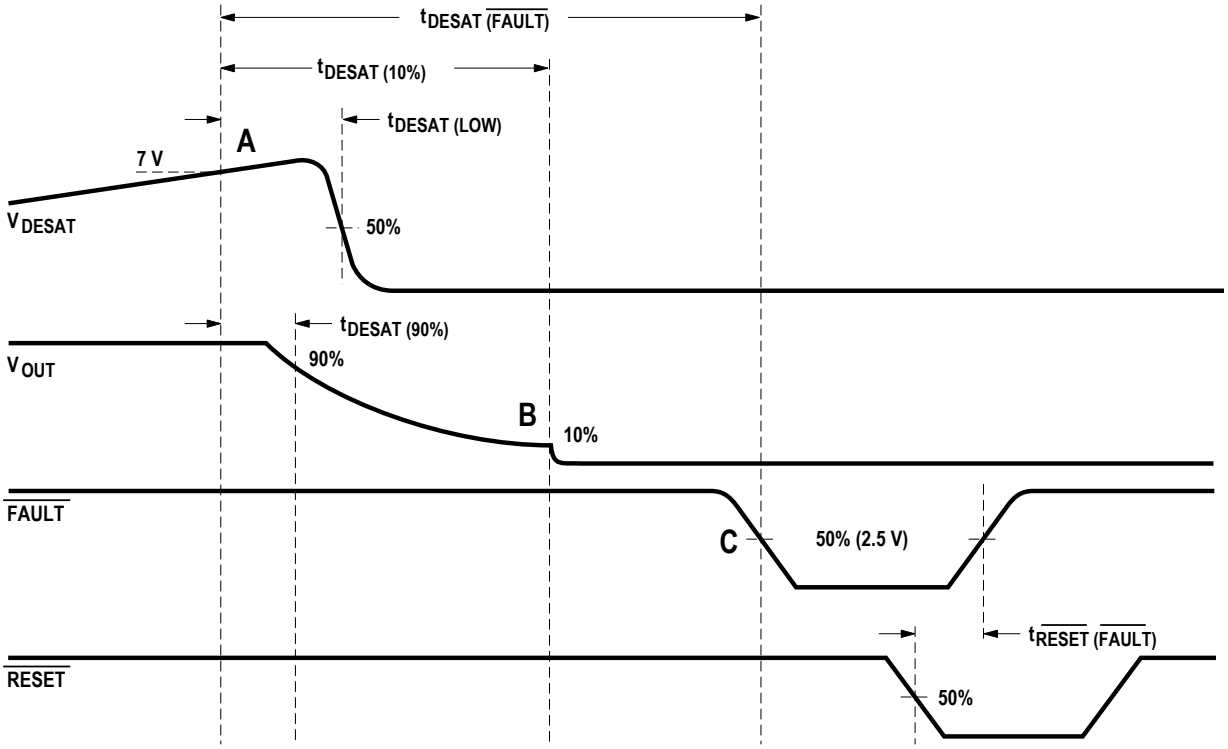

Figure 2. Desaturation, Gate Output Voltage V_{OUT}, FAULT and RESET waveform during short-circuit or overcurrent

Note:
$t_{DESAT(90\%)}$ is the DESAT Sense to 90% V_{OUT} time delay
$t_{RESET(FAULT)}$ is the RESET to High Level FAULT signal time delay

i. Fault Detection:

IGBT collector-emitter voltage, VCESAT is monitored through DESAT pin 14. The IGBT is turned off if the voltage threshold (typical 6.5V to 7V) is reached (Point A).

ii. Soft Turn-Off:

This is a two stage process. In the first stage, a weak pull-down device in the output drive stage will turn on to 'softly' turn off the IGBT. This device slowly discharges the IGBT. This turn off delay time of the gate optocoupler, is labeled as DESAT sense to 10% VOUT delay, $t_{DESAT(10\%)}$ in Figure 2. During soft turn-off, the internal 1xDMOS transistor is turned on.

During the slow turn off, the large output pull-down device, which is the second stage (Point B) remains off until the output gate voltage falls below V_{EE} + 2 Volts, at which time the large pull down device, 50xDMOS transistor, clamps the IGBT gate to V_{EE}. 50x represents DMOS 50 times larger than 1x (figure 3).

This $t_{DESAT(10\%)}$ time is dependent on the gate resistor R_g, gate capacitance C_g, output supply voltage V_{CC2}, and DMOS $R_{ds(on)}$ value. In HCPL-316J datasheet, $t_{DESAT(10\%)}$ is typically 2us for $R_g = 10\Omega$ and $C_g = 10nF$.

An approximation of the DMOS $R_{ds(on)}$ can be obtained by V_{OUT}/I_{OL} = 2.5/2.3 = 1.09Ω (Page 9 of HCPL-316J datasheet, Low Level Output Current). Hence the 1x DMOS $R_{ds(on)}$ is 50 x 1.09 = 54.5Ω. The time constant can be approximated using the following $C_g(R_g + 54.5)$.

Two characterization graphs reflecting the influence of Rg and Cg to the DESAT sense to 10% time are shown in Figure 4 and Figure 5. Both graphs can be found on page 13 in HCPL-316J datasheet

iii. Fault Output and Off State:

After the DESAT sense to Low Level FAULT signal delay time, $t_{DESAT(FAULT)}$, the FAULT signal goes low (Point C). Fault detect circuitry is disabled to prevent false 'fault' signals. The driver outputs will remain low (IGBT off) until the following two conditions are met:

The DESAT detection is low AND there is RESET signal (HCPL-316J) or Auto-RESET in the next INPUT PWM high signal is sent (ACPL-331J,ACPL-332J).

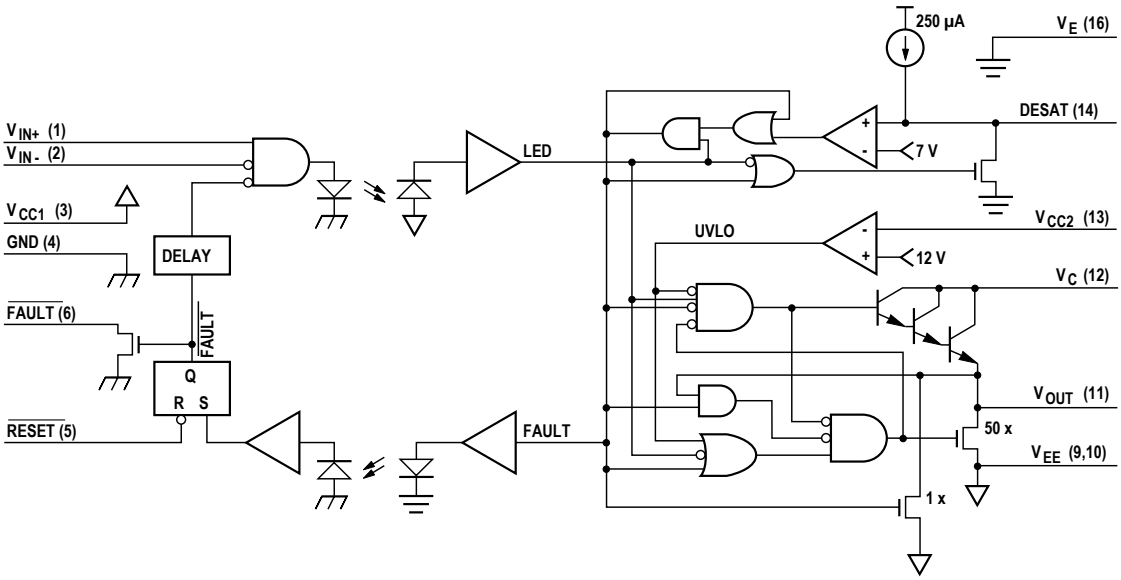

Figure 3.

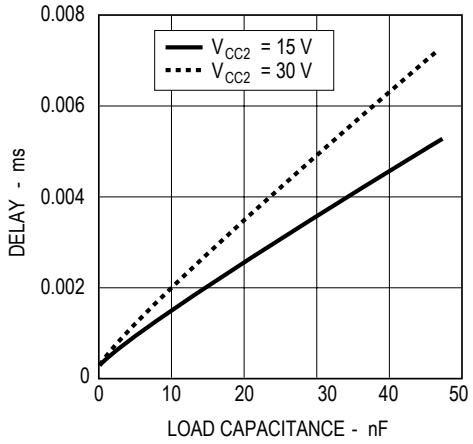

Figure 4.

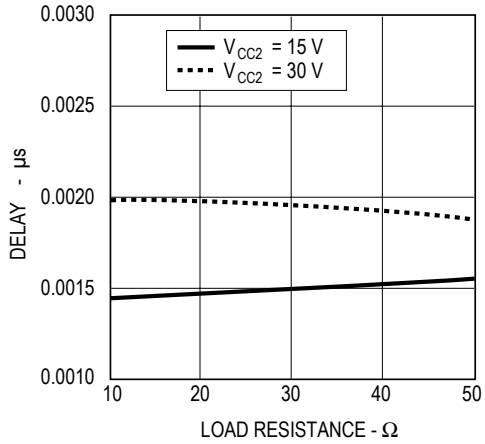

Figure 5.

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AV02-0073EN - January 24, 2007