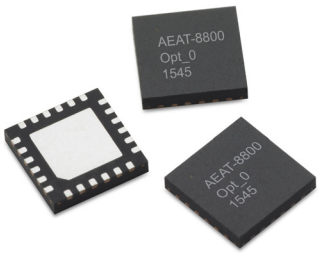
AEAT-8800-Q24

Magnetic Encoder IC
10- to 16-Bit Programmable Angular Magnetic Encoder

Data Sheet



Description

The Avago AEAT-8800-Q24 is an angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation.

It is a sophisticated system that uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A simple two-pole magnet generates the necessary magnetic field by rotating it in perpendicular, placed in alignment to the center of the device.

The Avago AEAT-8800-Q24 is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and one-time programmable resolution of 10, 12, 14, or 16 bits. When selected, its positioning data is then represented in its digital form to be assessed through a standard SSI 3 wire communication protocol. Where desired, users may also choose to receive its absolute angle position in PWM-encoded output signals.

The incremental positions are indicated on ABI and UVW signals with user configurable CPR 32, 64, 128, 256, 512, 1024, 2048, and 4096 of ABI signals and pole pairs from 1 to 8 (2 to 16 poles) for UVW commutation signals. An internal voltage regulator allows the AEAT-8800-Q24 to operate at either 3.3V or 5V supplies.

Key Features

- 5V or 3.3V operation
- Three-wire SSI interface for absolute output
- Selectable 10, 12, 14, or 16 bits of absolute resolution
- Incremental ABI and UVW pins out
- PWM output modes
- User-programmable zero position, direction, and index pulse width
- Selectable zero latency mode option to reduce latency to near 0
- Programmable hysteresis
- Easy alignment and calibration mode
- Compact QFN-24 leads (5 mm × 5 mm) package
- RoHS compliant

Specifications

- Absolute 10-bits to 16-bits resolution
- Incremental output resolutions 32 to 4096 CPR
- UVW output of 1 to 8 pole pairs
- Wide operating temperature –40°C to 125°C

Applications

- Three-phase commutation for a brushless DC motor
- Resolver and potentiometer replacement
- Industrial automation and robotics
- Industrial sewing machine and textiles equipment

NOTE This product is not specifically designed or manufactured for use in any specific device. Customers are solely responsible for determining the suitability of this product for its intended application and solely liable for all loss, damage, expense, or liability in connection with such use.

Definitions

Electrical Degree (°e): CPR × 360 electrical degrees = 360 mechanical degrees.

Cycle (C): One cycle of the incremental signal is 360 mechanical degrees/resolution and is equal to 360 electrical degrees (°e).

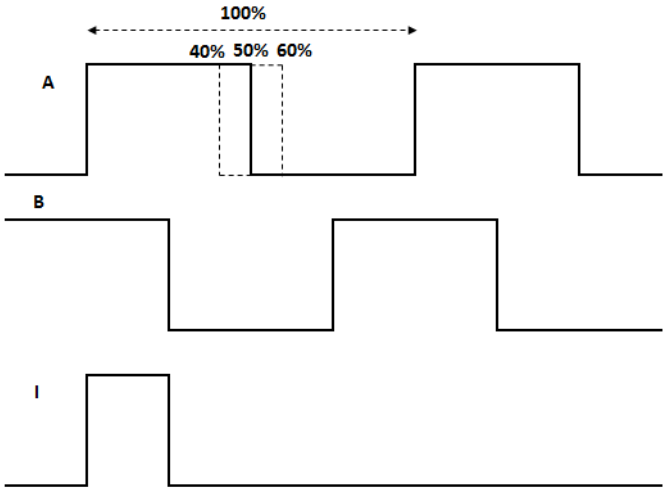
Pulse Width (P): The number of electrical degrees that an output is high during one cycle, nominally 180°e or one-half of a cycle.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are four states per cycle, each nominally 90°e.

Phase (Φ): The number of electrical degrees between the center of the high state on channel A and the center of the high state on channel B.

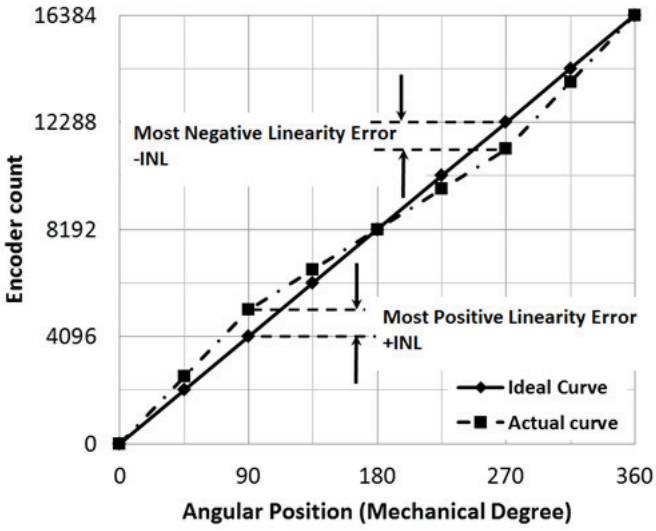
Relative angular accuracy: With reference to the output period at A and B. The relative accuracy of the edges to each other at a CPR setting of 256 is within ± 10% for 5V operation in a typical condition. Therefore, based on a period at A or B, the edge occurs in a window between 40% and 60% as shown in the following figure.

Figure 1 ABI Signals of AEAT-8800-Q24



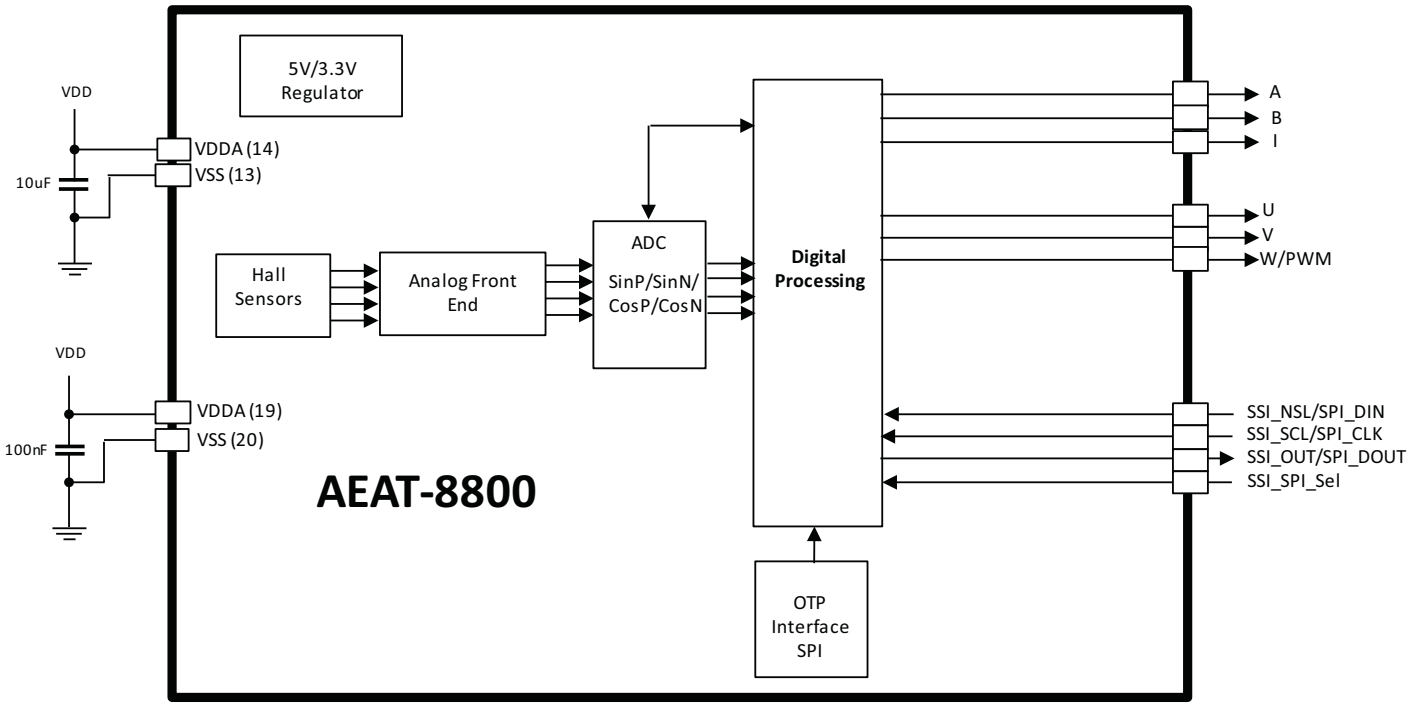
Integral non-linearity (INL): The maximum deviation between actual angular position and the position indicated by the encoder's output count, over one revolution. It is defined as the most positive linearity error +INL or the most negative linearity error –INL from the best fit line, whichever is larger.

Figure 2 Integral Non-Linearity Example



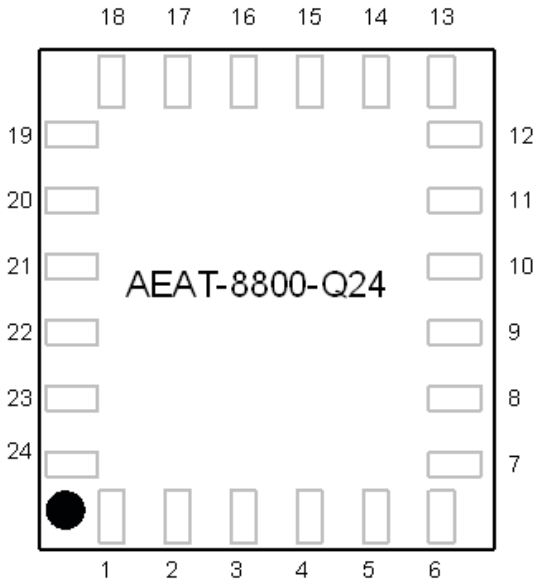
Functional Description

Figure 3 AEAT-8800-Q24 Block Diagram



Pin Assignment

Figure 4 Pin Configuration for AEAT-8800-Q24



Pin-out Description

Pin	Symbol	Description
1–6	No connection	N/A
7	I	Index output (ABI mode)
8	B	Incremental B output (ABI mode)
9	A	Incremental A output (ABI mode)
10	SSI_SCL_SPI_CLK	SSI/SPI clock input
11	SSI_NSL_SPI_DI	SSI/SPI data input
12	SSI_DO_SPI_DO	SSI/SPI data out
13	VSS	Supply ground
14	VDDA	3.3V/5V supply input
15	No connection	No connection
16	No connection	No connection
17	No connection	No connection
18	No connection	No connection
19	VDDA	3.3V/5V supply input
20	VSS	Supply ground
21	SSI_SPI_SEL	SSI/SPI select pin
22	U	U commutation output (UVW mode)
23	V	V commutation output (UVW mode)
24	W or PWM	W commutation (UVW mode)/ PWM output

The AEAT-8800-Q24 is manufactured with a CMOS standard process. It is capable of accurately measuring a magnet's rotational angle when it is placed in alignment and in perpendicular to the device by using its integrated Hall sensors to detect its magnetic field. The detected magnetic signals are then taken as input signals to be properly conditioned to negate its non-idealities before inputting them into the analog amplifiers for strength amplification and filtering. After which, the amplified analog signals are then fed into the internal analog-to-digital converter (ADC) to be converted into digital signals for the final stage of digital processing. The digital processing provides a digitized output of the absolute and incremental signals.

For optimal performance, the used magnet's center axis should be aligned to the center of the device with a tolerable displacement radius of 0.5mm from defined Hall sensor center as described in Magnet and IC Package Placement. Moreover, the used magnet should have sufficient magnetic field strength mT to generate the magnetic field for the signal generation as highlighted in Recommended Magnetic Input Specifications. The device provides digital information of magnetic field strength high MHi and magnetic field strength low MLo from SSI read to indicate whether the magnets are too close or too far away from our device's surface.

Users can assess the device's digitized absolute data using standard Synchronous Serial Interface (SSI) protocols. In addition, an absolute angular representation also can be selected using a pulse width modulated (PWM) signal.

The incremental outputs are available from digital outputs of their respective A, B, and I pins. This is the same for the U, V, and W pins.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	125	°C	
DC Supply Voltage VDD pin VPP pin	 VDD VPP	 –0.3 –0.3	 5.5 5.5	Volts	
Input Voltage Range	Vi_n	–0.3	5.5	Volts	
Electrostatic Discharge		–2.0	+2.0	kVolts	
Moisture Sensitivity Level			3		Maximum floor life = 168 hrs

CAUTION Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices. These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

Electrical Characteristics

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Ambient Temperature	T_A	–40	-	125	°C	
DC Supply Voltage to VDD pin 5V operation 3.3V operation	VDD 	 4.5 3.0	 5.0 3.3	 5.5 3.6	Volts	
OTP Programming Voltage at VDDA Pin		5.5	5.6	5.7	Volts	
Incremental Output Frequency	f_{MAX}	—	—	1.0	MHz	Frequency = Velocity(rpm) × CPR/60
Load Capacitance	C_L	—	—	15	pF	

Systems Parameters

Condition: Electrical characteristics over the recommended operating conditions. Typical values specified at VDD = 5.0V and 25°C, optimum placement of magnet.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Current Consumption						
Supply Current Normal Operation Mode	I_{DD}	—	20	24	mA	
Digital Outputs (DO)						
High Level Output Voltage	V_{OH}	VDD – 0.5	—	—	Volts	Normal operation
Low Level Output Voltage	V_{OL}	—	—	GND + 0.4	Volts	
Power-up time Absolute Output Incremental Output PWM Output	t_{PwrUp}	—	4		ms	
Digital Inputs (DI)						
Input High Level	V_{IH}	0.7 × VDD	—	—	Volts	
Input Low Level	V_{IL}	—	—	0.3 × VDD	Volts	
Pull-up low level input current	I_{IL}	—	—	120	µA	
Pull-down high level input current	I_{IH}	—	—	120	µA	

Encoding Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Absolute Output						
Resolution	RES	10	—	16	Bit	10, 12, 14, or 16 bits
Integral Non-Linearity (optimum)	INL_{nom}	—	—	± 0.5	Deg	Best fit line, centered magnet, after calibration. Tamb = 25ºC @ 5V.
Integral Non-Linearity	INL	—	—	± 1.5	Deg	Best fit line, over displacement of magnet, after calibration. Tamb = –40 to +125ºC Voltage = 5V
Output Sampling Rate	f_S	—	10	—	MHz	Based on SSI protocol
Code monotony 10, 12, 14 bit			1		Step	Tamb = –40 to 125ºC @ 5V
Incremental Output (Channel ABI)						
Resolution	R_{INC}	32	—	4096	CPR	Programmable options 32, 64,128, 256, 512,1024, or 4096 CPR
Index Pulse Width	P_O	90	—	360	°e	Programmable options: 90, 180, 270, or 360 ºe
Relative angular accuracy	%	—	± 10%		%	Reference to an output period at outputs A and B, at 256 CPR, 5V and 10,000 RPM
Commutation Characteristic (Channel U,V,W)						
Commutation Format	Programmable pole pairs from 1 to 8 (2 to 16 poles)					
Commutation Accuracy	ΔUVW		± 2		°mechanical	
PWM Output						
PWM frequency	f_{PWM}	122		976	Hz	Adjustable based on our PWM settings
Minimum pulse width	PW_{MIN}		1		µs	
Maximum pulse width	PW_{MAX}		8192		µs	

NOTE Encoding Characteristics over Recommended Operating Range unless otherwise specified.

Encoding Timing Characteristics

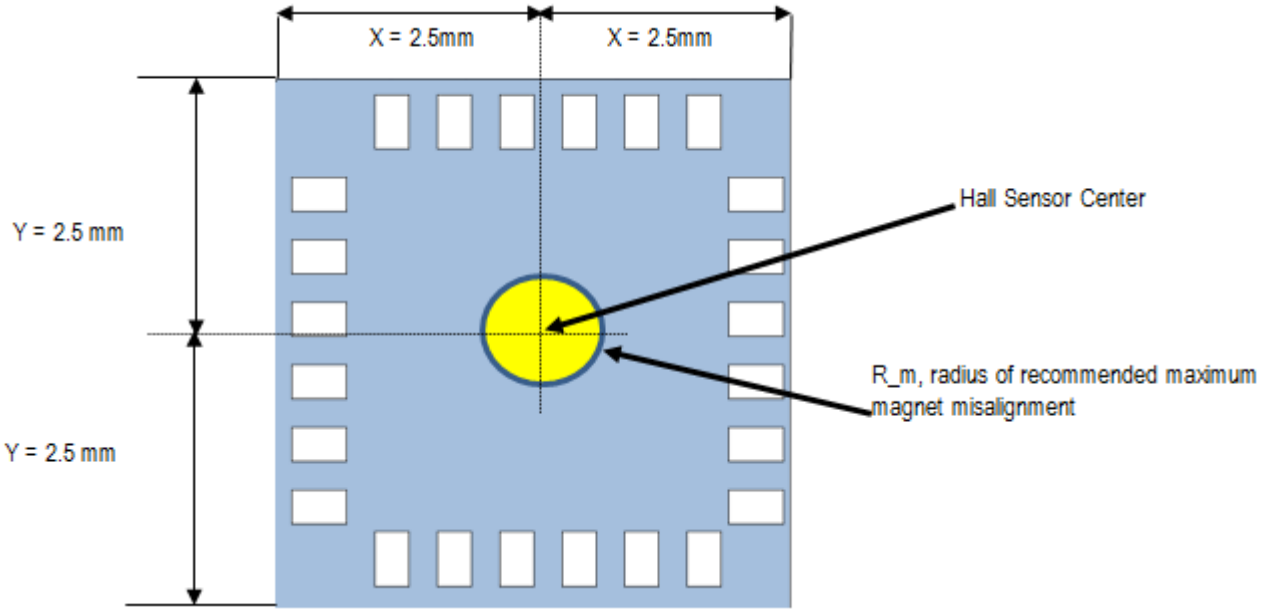
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Incremental Output (ABI and UVW)						
System reaction time	t_{delay}		4		ms	First ABI pulse detection upon power up.

Recommended Magnetic Input Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Diameter	d		6		mm	Recommended magnet: Cylindrical magnet, diametrically magnetized and 1 pole pair.
Thickness	t		2.5		mm	
Magnetic input filed magnitude	B_{pk}	45	—	75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet displacement radius	R_m			0.5	mm	Displacement between magnet axis to the device center
Recommended magnet material and temperature drift			–0.12		%/K	NdFeB (Neodymium Iron Boron), grade N35SH

Magnet and IC Package Placement

Figure 5 Defined Chip Sensor Center and Magnet Displacement Radius



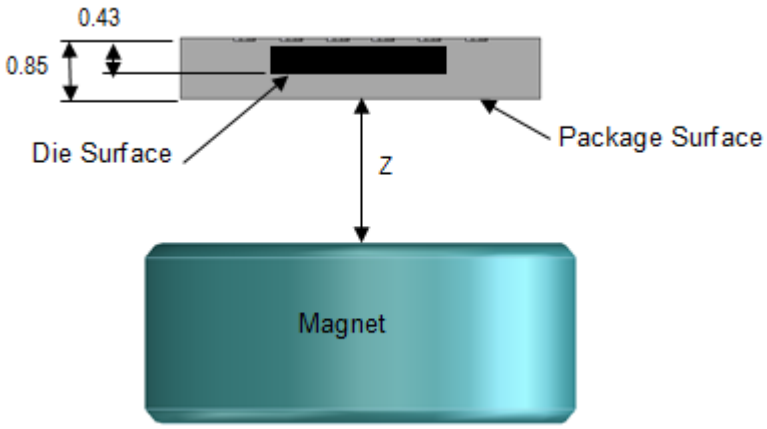
Align the magnet's center axis within a displacement radius of 0.5 mm from defined hall sensor center.

Place the magnet so that it faces the sensor. The magnet must be mounted on a non-magnetic part. The Z gap varies depending on the magnetic strength on the die surface, with the recommended magnet material and dimensions.

The typical distance Z is 0.5 mm to 1.5 mm. However, larger distance is possible as long as the magnetic strength is within the defined limit.

It is important not to put magnetic material close to the magnet because it will affect the magnetic field and increase the INL.

Figure 6 Vertical Placement of the Magnet



Timing Characteristics

Parameter	Sym	Min.	Typ.	Max.	Units	Notes
F_{clk}		—	—	10000	kHz	SCL clock frequency for SSI protocol
tREQ		300	—		ns	Minimum time required for encoder to prepare SSI output
tNSLH		200	—	—	ns	Minimum wait time between SSI request

NOTE SSI timing characteristics are over recommended operating range unless otherwise specified. See SSI 3 Wires (SSI) for more information on the table.

Memory Map

Avago AEAT-8800-Q24 uses nonvolatile one-time programmable (OTP) as shown in the following tables.

The memory is separated into 8 bits per address.

Nonvolatile Register (OTP)

1. OTP is one time programmable only. Any OTP bit with value 0 can be written to 1, but *not* vice versa. Do *not* program 1 to the same address bit twice.
2. OTP shadow registers are volatile registers that are loaded with corresponding OTP values after power ON.
3. All bits (except addresses 0x00–0x03, 0x10–0x12, and 0x1B) are in a LOCK mode by default after power ON. To enter UNLOCK mode (to be able to write to the OTP shadow registers or registers), write 0xAB to address 0x10.
4. In UNLOCK mode, write to *any* OTP shadow registers or registers. Values written remain until power OFF.
5. UNLOCK state is maintained until the power supply is turned OFF or any value (except 0xAB) is written to address 0x10.
6. All OTP memory is programmable only by writing appropriate commands to addresses 0x11–0x13 and 1B.

OTP Shadow Registers

1. OTP shadow registers are volatile (upon power up, reload values from OTP) and are not written to OTP automatically.
2. To write OTP shadow registers values to OTP (nonvolatile) memory, see Programming OTP via SPI.
3. The OTP shadow registers are from addresses 0x00 to 0x0D.

The following tables show the registers.

Customer Reserve and Zero Offset Registers

Table 1 Customer Reserve and Zero Reset Registers

Address	Bit(s)	Name	Description	Default
0x00	7–0	Customer Reserve 0	User programmable	8'h0
0x01	7–0	Customer Reserve 1	User programmable	8'h0
0x02	7–0	Zero Reset0	Zero Reset Position [7:0]	8'h0
0x03	7–0	Zero Reset1	Zero Reset Position [15:8]	8'h0

Customer Configuration Registers

These registers are required to unlock and can be done by writing 8'hAB to address 0x10, then write to OTP shadow register.

Customer Configuration 0

Table 2 Customer Configuration 0 Registers

Address	Bit (s)	Name	Description	Default
0x04	7	UVW Select	■ 1: Select UVW mode ■ 0: Select PWM mode	0
	6–5	PWM Setting	■ 11: PWM period = 8193 µs ■ 10: PWM period = 4097 µs ■ 01: PWM period = 2049 µs ■ 00: PWM period = 1025 µs	00
	4–3	I-width Setting	■ 11: (ABI) I-width = 360 electrical deg (edeg) ■ 10: (ABI) I-width = 270 electrical deg (edeg) ■ 01: (ABI) I-width = 180 electrical deg (edeg) ■ 00: (ABI) I-width = 90 electrical deg (edeg)	00
	2–0	UVW Setting	■ 111: UVW = 8 pole-pairs ■ 110: UVW = 7 pole-pairs ■ 101: UVW = 6 pole-pairs ■ 100: UVW = 5 pole-pairs ■ 011: UVW = 4 pole-pairs ■ 010: UVW = 3 pole-pairs ■ 001: UVW = 2 pole-pairs ■ 000: UVW = 1 pole-pairs	000

Customer Configuration 1

Table 3 Customer Configuration 1 Registers

Address	Bit(s)	Name	Description	Default
0x05	7–4	CPR Setting 1[a]	■ 0111: (ABI) 4096 CPR ■ 0110: (ABI) 2048 CPR ■ 0101: (ABI) 1024 CPR ■ 0100: (ABI) 512 CPR ■ 0011: (ABI) 256 CPR ■ 0010: (ABI) 128 CPR ■ 0001: (ABI) 64 CPR ■ 0000: (ABI) 32 CPR	0000
	3–0	Hysteresis Setting	■ 1001: 1.4 mechanical degree (mdeg) ■ 1000: 0.7 mechanical degree (mdeg) ■ 0111: 0.35 mechanical degree (mdeg) ■ 0110: 0.17 mechanical degree (mdeg) ■ 0101: 0.08 mechanical degree (mdeg) ■ 0100: 0.04 mechanical degree (mdeg) ■ 0011: 0.02 mechanical degree (mdeg) ■ 0010: 0.01 mechanical degree (mdeg) ■ 0001: 0.005 mechanical degree (mdeg) ■ 0000: No Hysteresis	0000

a. Incremental: The CPR setting 1 in address 0x05 must match to CPR setting 2 in 0x06.
Absolute: For absolute only application, set CPR setting 2 in 0x06 to 0100.

Customer Configuration 2

Table 4 Customer Configuration 2 Registers

Address	Bit(s)	Name	Description	Default
0x06	7	Dir[a]	■ 1: Count up at counter-clockwise rotation ■ 0: Count up at clockwise rotation	0
	6	Zero Latency Mode[b]	■ 1: Zero Latency is ON ■ 0: Zero Latency is OFF	0
	5–4	Absolute Resolution	■ 11: 10-b absolute resolution (SSI) ■ 10: 12-b absolute resolution (SSI) ■ 01: 14-b absolute resolution (SSI) ■ 00: 16-b absolute resolution (SSI)	00
	3–0	CPR setting 2[c]	■ 0101: 4096 CPR ■ 0101: 2048 CPR ■ 0100: 1024 CPR ■ 0100: 512CPR ■ 0011: 256CPR ■ 0010: 128CPR ■ 0010: 64CPR ■ 0010: 32CPR ■ 0100: Absolute Resolution	0000

a. See Figure 7 for the direction definition.

b. Zero Latency is only applicable from 32cpr ~1024cpr. When Zero Latency Mode is On, user must set CPR setting 2 in 0x06 to 0101 for all the applicable CPR (32~1024).

c. Incremental: The CPR setting 1 in address 0x05 must match to CPR setting 2 in 0x06.
Absolute: For absolute only application, set CPR setting 2 in 0x06 to 0100.

Feature Settings

Zero Reset

AEAT-8800-Q24 allows the user to configure a Zero Reset position. This value is stored at OTP 0x02 (lower 8-b) and 0x03 (upper 8-b). To set the Zero Reset position, for example, position X, perform the following steps.

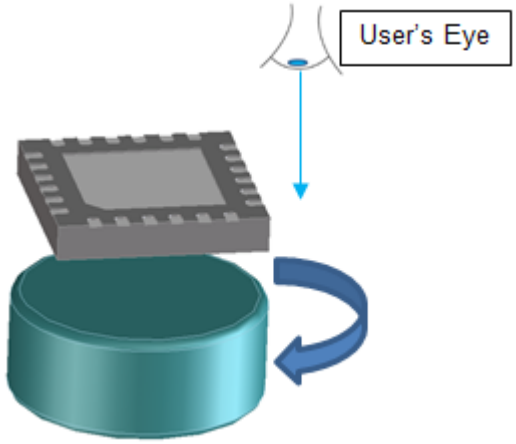
NOTE The user should decide the desired direction or orientation, (as detailed inDirection) before setting the Zero Reset position.

1. Stop the motor at position X.
2. Read the 16-b value of position X using SSI protocol (for example read 16'hABCD).
3. Write lower 8-b (from the preceding example, 8'hCD) to 'OTP shadow registers' 0x02 using SPI.
4. Write upper 8-b (from the preceding example, 8'hAB) to 'OTP shadow registers' 0x03 using SPI.
5. Confirm that the correct Zero Reset value is written to 'OTP shadow registers' by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding step jumps incurred by noise).
6. To permanently save this Zero Reset value, write 8'hA2 to internal registers 0x12.
7. Power-cycle the chip, and confirm that the correct Zero Reset value is written to OTP by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding step jumps incurred by noise).

Direction

The direction must be defined as to whether to count up at clockwise or counterclockwise per rotation. Per the default setting, if the magnet is spinning at a clockwise position, based on the user's line of sight per the following figure, then AEAT-8800-Q24 will count up.

Figure 7 Direction Definition when the Magnet Rotates



Offset Calibration

The AEAT-8800-Q24 features offset calibration to enhance the angular accuracy measurement detected by the Hall sensors. This feature enables the user to align the Hall sensors to the best accuracy within the recommended alignment area as defined in Magnet and IC Package Placement.

This alignment can address the variations of the spatial displacement during integration.

Perform the following steps to use this feature.

1. Write 8'h02 to 0x17 to start a calibration.
2. Rotate the magnet at any direction at 100 rpm.
3. Monitor the ABI output of AEAT-8800-Q24 with an oscilloscope.
4. The following signal indications (monitored with an oscilloscope) describe the status of the signal during calibration:
   - ABI = 3'b111

     Indication of AEAT-8800-Q24 successfully calibrated.
   - A=0

     Indication that the distance between AEAT-8800-Q24 and the magnet is too close or too far.
   - B or/and I=0

     Indication of AEAT-8800-Q24 not being able to calibrate properly due to poor magnet alignment; it is beyond of its spatial tolerances.
5. Repeat step 2 to step 3, until the indication at step 4 meets the expected criterion.
6. To end the calibration, write 8'h00 to 0x17.
7. The calibration is completed when ABI signals all high (observed with the oscilloscope).
8. To OTP offset calibration, write 8'hA5 to address 0x1B as indicated in the table in Programming OTP via SPI.

NOTE A typical successful calibration should be completed in less than 30 revolutions.

Absolute Output Format

The AEAT-8800-Q24 provides SSI 3 wires and PWM outputs to indicate absolute position of the motor.

SSI 3 Wires (SSI)

SSI protocol uses three pins and is shared between SSI and SPI protocols. Use SSI_SPI_sel (the input pin) to select either protocol at a time. Assert 1 on SSI_SPI_sel to select SSI protocol, which supports up to 10-MHz clock rates.

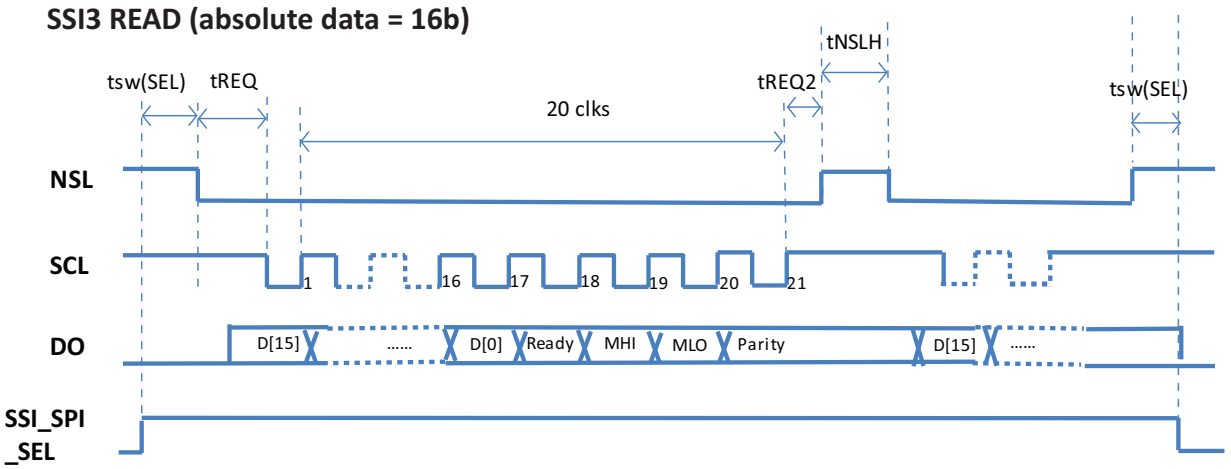
- SSI_NSL_SPI_DIN → NSL (enable) signal for SSI protocol, input to AEAT-8800-Q24
- SSI_SCL_SPI_CLK → SCL (clock) signal for SSI protocol, input to AEAT-8800-Q24
- SSI_DO_SPI_DO → DO (data out) signal for SSI protocol, output from AEAT-8800-Q24

NOTE Notes for timing diagram in the following figure:

- NSL must held high for at least 3 ms after power up.
- NSL = 1 means it is in load mode and is used to obtain the position of the magnet.
- NSL = 0 is shift mode of the registers and with the SCL (clock) pin, the register will be clocked.
- tREQ ≥ 300 ns.
- tNSLH ≥ 200 ns.

The user is advised to read from the SSI falling edge.

Figure 8 SSI Protocol Timing Diagram



Symbol	Description	Min	Typ	Max	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1			µs
tREQ	SCL hight time between NLS falling edge and first SCL falling edge	300			ns
tREQ2	NSL low time after rising edge of last clock period for an SSI read	200			ns
tNSLH	NSL high time between 2 successive SSI reads	200			ns

NOTE CLK=1 when inactive; DIN=1 when inactive.

Important: Make sure that CLK is high when switching between SSI and SPI modes.

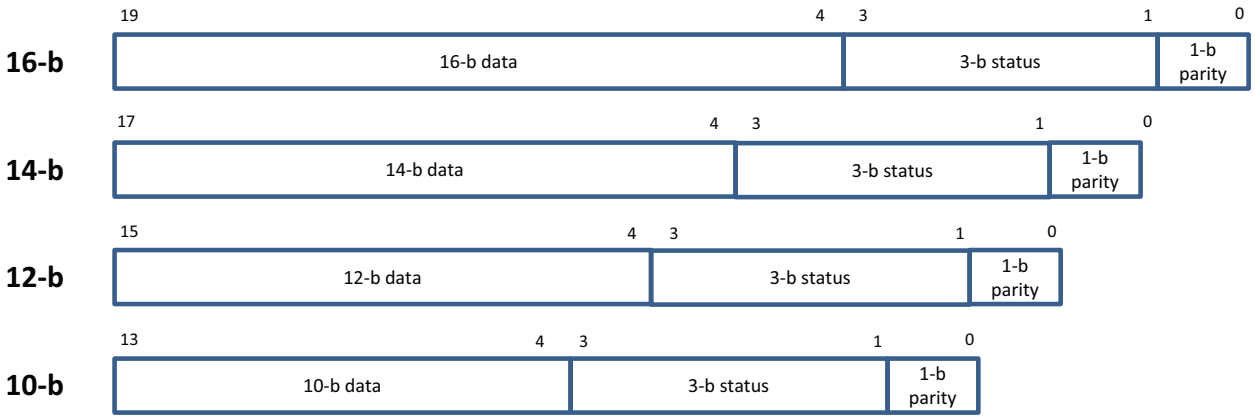
SSI data format may vary depending on the different settings on absolute resolution (16/14/12/10 bits).

The total data length is shown in the following figure.

Three bits status is for Ready, MHI, and MLO.

Figure 9 SSI Output Format for Different Absolute Resolution Settings

SSI3 READ Data Format



NOTE

- Total data length: 16-b pos —> 20-b, 14-b pos—> 18-b, 12-b pos —> 16-b, 10-b pos —> 14-b
- 3-b status: {Ready, MHI, MLO}

- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change the weaker magnet or increase the distance between the chip and the magnet.

  The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change the stronger magnet or decrease the distance between the chip and the magnet.

  The value for this alarm is represented as 1.
- **Ready:** The chip is ready, and the ready value is 1.

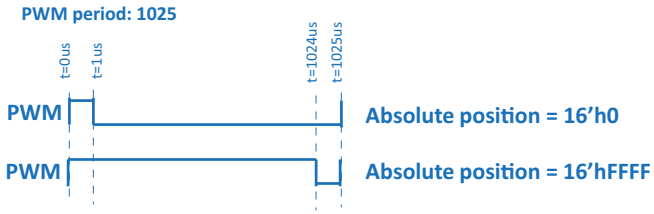
  1-b parity is even parity.

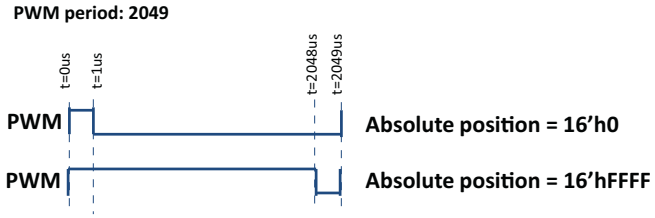
PWM

PWM protocol uses one output pin (W_PWM) from AEAT-8800-Q24. Note that W_PWM pin is shared between UVW and PWM protocols. The PWM signals are configurable to have period of 1025, 2049, 4097, or 8193 µs. During power-up, the PWM signal is 0 before chip ready.

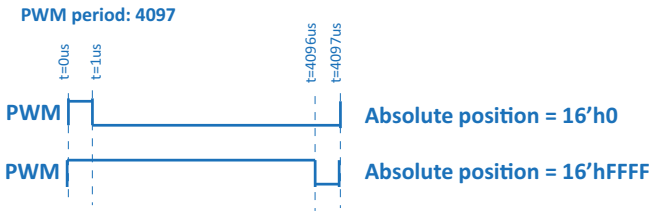
Figure 10 PWM Signals (Period = 1025/2049/4097/8193 µs)

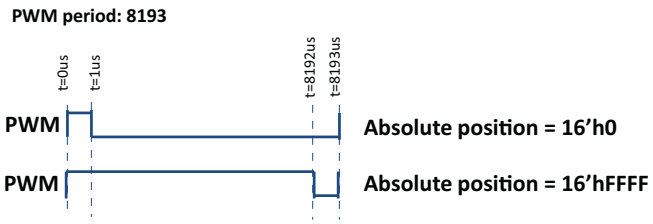
- PWM period: 1025, 2049, 4097, 8193 µs





- PWM period: 1025, 2049, 4097, 8193 µs





Incremental Output Format

The AEAT-8800-Q24 provides ABI and UVW signals to indicate incremental position of the motor.

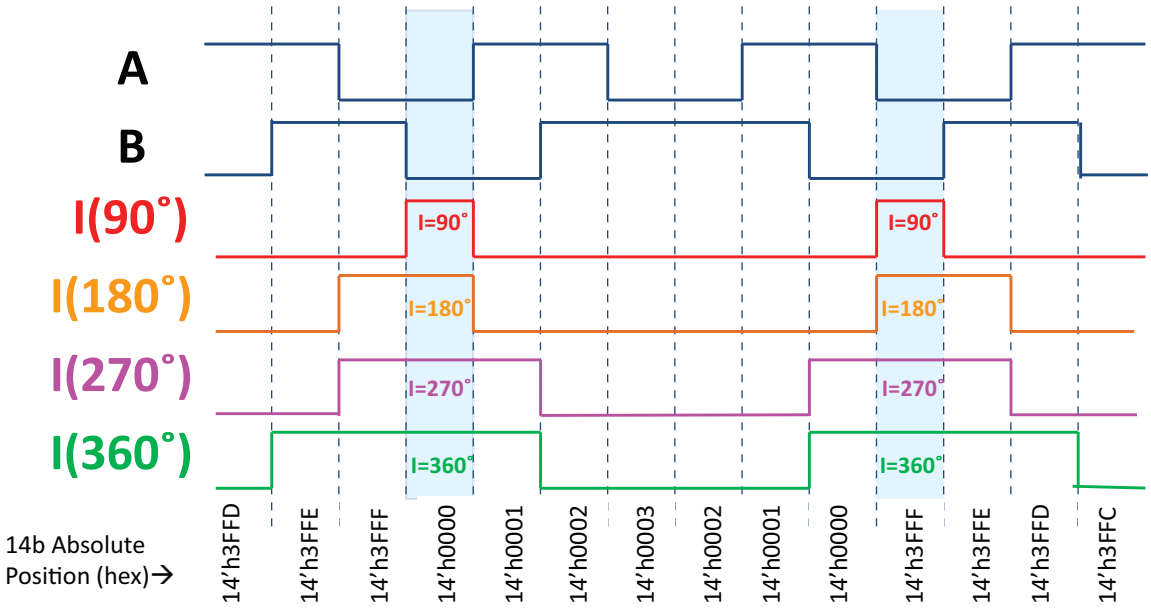
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution The ABI signal is configurable using the memory map registers. It supports the following configuration:

- Programmable CPR: 32, 64, 128, 256, 512, 1024, 2048, or 4096
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)

Figure 11 ABI Signal (4096 CPR, with Different I-Width Settings), Assuming User Sets Hysteresis at 0.02 Mechanical Degree

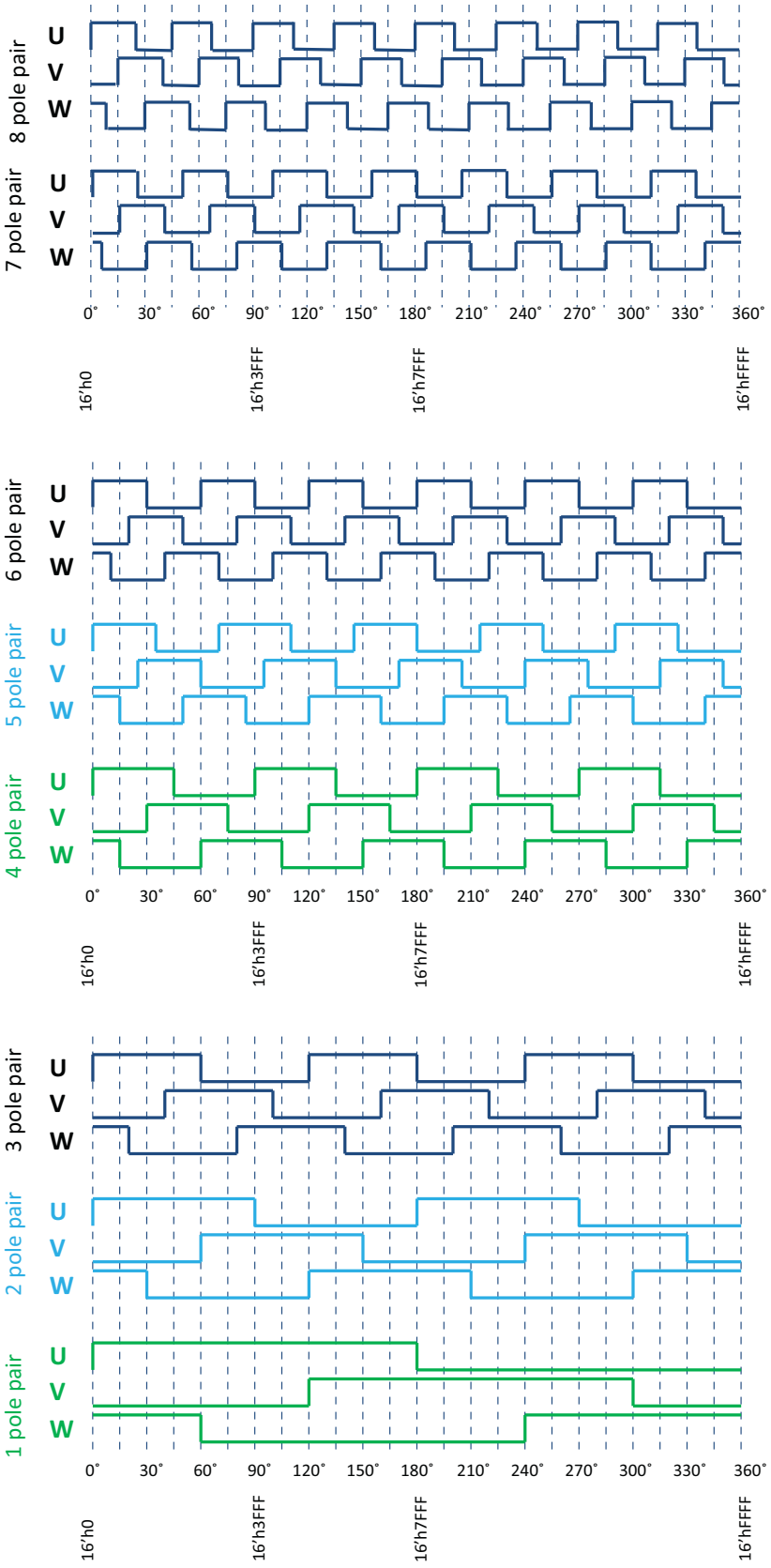


UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that W_PWM pin is shared between the UVW and PWM protocols.

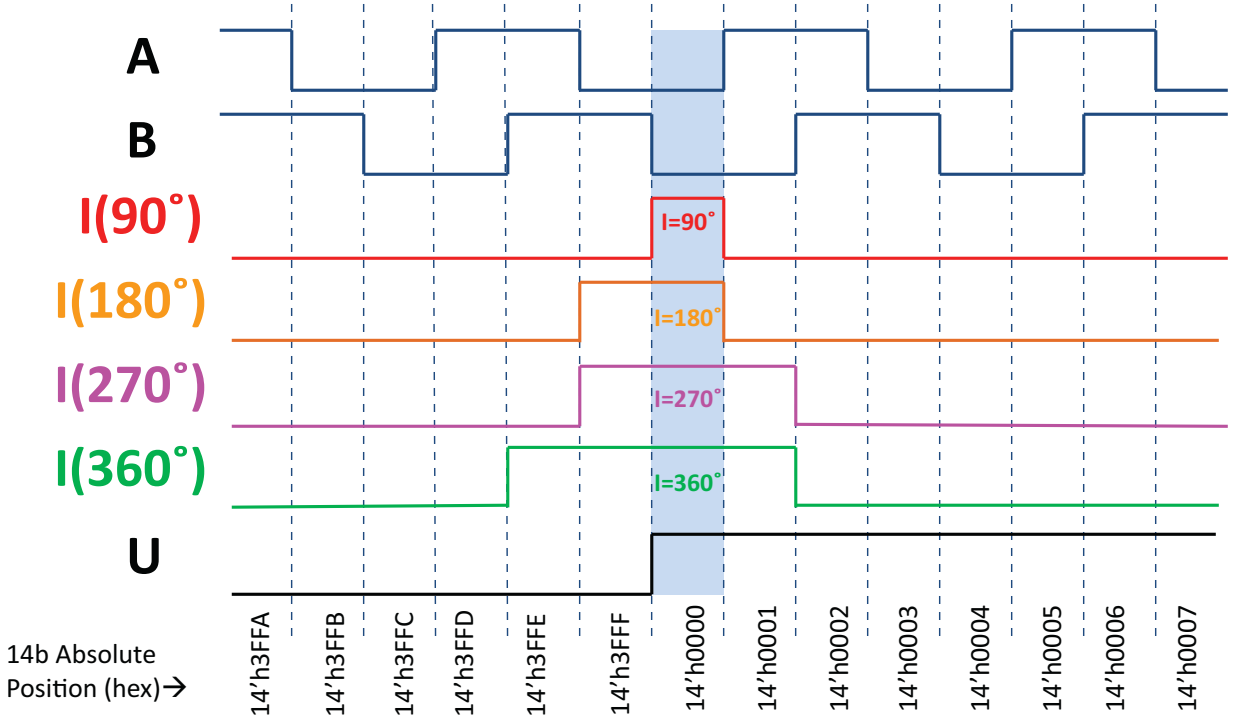
AEAT-8800-Q24 can configure pole pairs from 1 to 8 equivalents to 2 to 16 poles.

Figure 12 UVW Signals (1~8 Pole-Pairs)



Note that signal U from UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 13 U-to-I Tagging



Programming the AEAT-8800-Q24

The OTP shadow registers and internal registers are programmable using the SPI protocol. Writing specific commands to specific addresses of internal registers will program values of OTP shadow registers to OTP permanently.

SPI Protocol

SPI protocol uses three pins from AEAT-8800-Q24. These three pins are shared between SSI and SPI protocols. SSI_SPI_sel (input pin) selects either protocol at a time. Assert 0 on SSI_SPI_sel to select the SPI protocol. The AEAT-8800-Q24 supports the SPI protocol from 10 kHz to 1 MHz.

- SSI_NSL_SPI_DIN → DIN (data in) signal for SPI protocol, input to AEAT-8800-Q24
- SSI_SCL_SPI_CLK → CLK (clock) signal for SPI protocol, input to AEAT-8800-Q24
- SSI_DO_SPI_DO → DO (data out) signal for SPI protocol, output from AEAT-8800-Q24

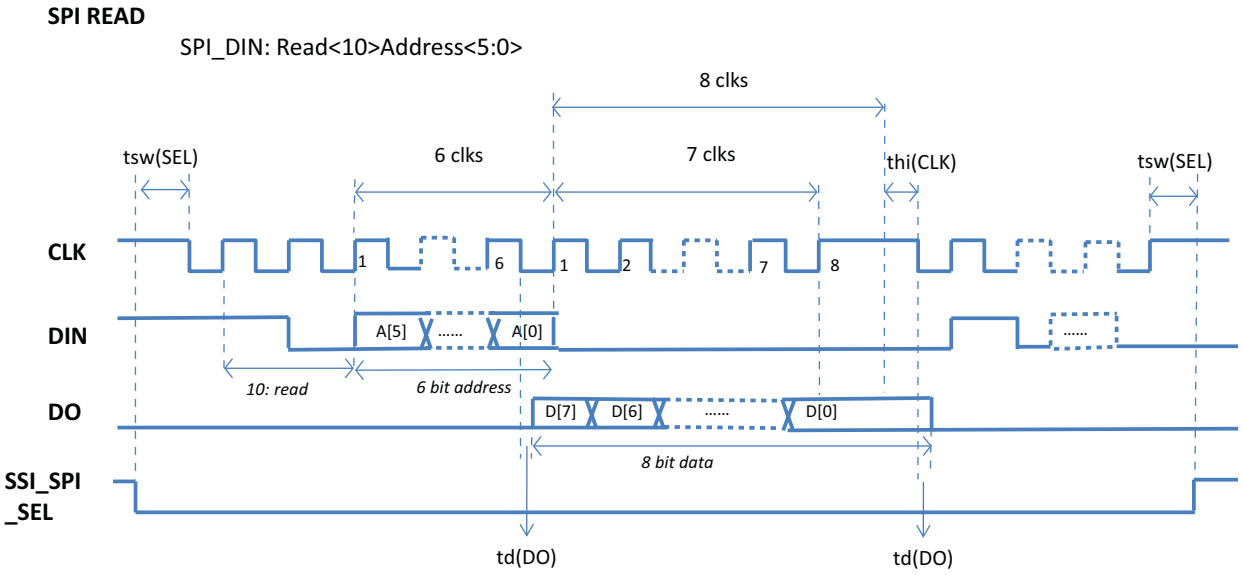
To read an address using SPI:

DIN: Read<2'b10>Address<5:0>; from 8 bits DIN

Read 8-bit data on DO by clocking 8 SPI_CLK clock.

NOTE The user should read output data at the rising edge of SPI_CLK.

Figure 14 SPI Read Timing Diagram



Symbol	Description	Min	Typ	Max	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1			µs
td(DO)	DO data valid after falling edge of CLK			200	ns
thi(CLK)	CLK high time after end of last clock period for an SPI read/write command	300			ns

NOTE

- CLK=1 when inactive; DIN=1 when inactive.
- Important: Make sure CLK is high when switching between SSI and SPI modes.

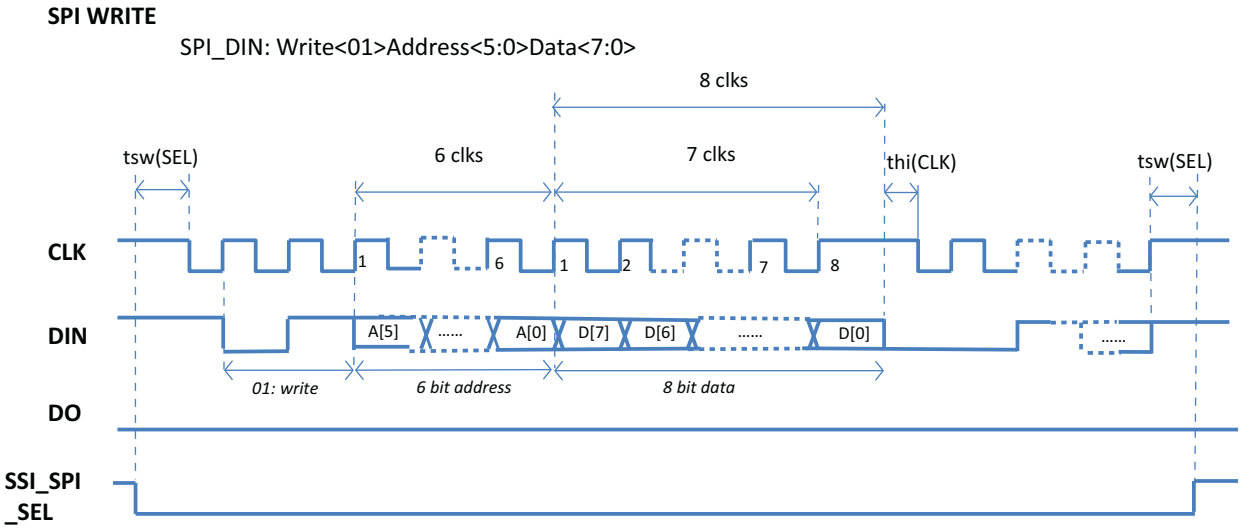
To write to an address using SPI:

Write <2'b01>Address<5:0>; from 8 bits DIN

- SPI_DIN: Write<01>Address<5:0>Data<7:0>
  - Write is specified as 2 bits (01) in the MSB of the address bus, followed by the 6-bit address, and lastly 8-bit data.

NOTE The user should read back data to confirm data written successfully.

Figure 15 SPI Write Timing Diagram



Symbol	Description	Min	Typ	Max	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1			µs
td(DO)	DO data valid after falling edge of CLK			200	ns
thi(CLK)	CLK high time after end of last clock period for an SPI read/write command	300			ns

NOTE

- CLK=1 when inactive; DIN=1 when inactive.
- Important: Make sure CLK is high when switching between SSI and SPI modes.

Programming OTP via SPI

Here are steps for permanently program the OTP nonvolatile memory.

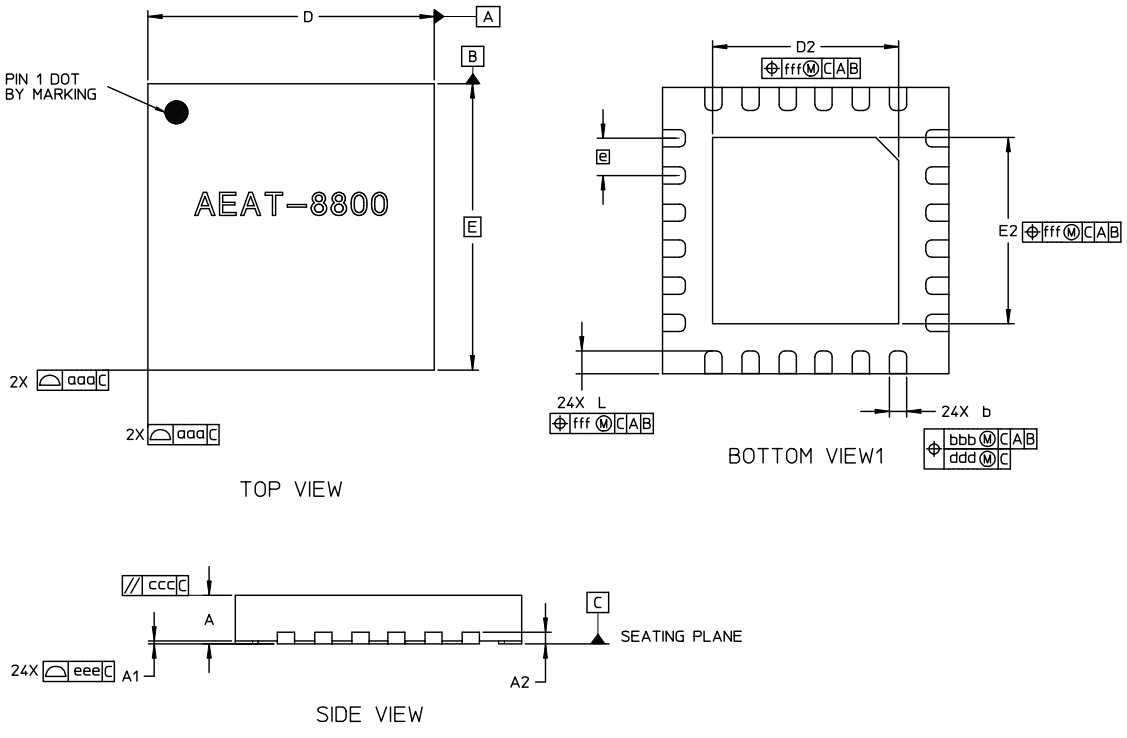
See the memory map address as described in Memory Map.

The following are details on the register 0x10 to 0x1B.

Address	Bit(s)	Name	Description	Default
0x10	7–0	Unlock Registers	Write 0xAB to this address to unlock all OTP shadow registers and internal registers (except 0x00~0x03, 0x10, 0x11, 0x12, and 0x1B, which are not locked).	8'h0
0x11	7–0	Program Customer Reserved OTP (0x00, 0x01)	Write 0xA1 to this address to program customer reserved OTP (0x00, 0x01) to OTP.	8'h0
0x12	7–0	Program ST Zero Reset OTP (0x02, 0x03)	Write 0xA2 to this address to program ST Zero Reset OTP (0x02, 0x03) to OTP.	8'h0
0x13	7–0	Program Customer Configuration OTP (0x04, 0x05, 0x06)	Write 0xA3 to this address to program Customer Configuration OTP (0x04, 0x05, 0x06) to OTP.	8'h0
0x1B	7–0	Program Configuration of Full Calibration OTP	Write 0xA5 to this address to program full calibration results to OTP.	8'h0

Package Drawings (in mm)

Figure 16 AEAT-8800, 24 QFN Dimensions



Dimension Reference			
REF	**Min**	**Nom**	**Max**
A	0.800	0.850	0.900
A1	0.000	-	0.050
A2	0.203 REF		
D	5.000 BSC		
E	5.000 BSC		
D2	3.200	3.250	3.300
E2	3.200	3.250	3.300
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.350	0.400	0.450
Dimension Tolerance			
aaa	0.100		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

Product Ordering Information

Ordering Part Number	Product Description	Package	Delivery Form
AEAT-8800-Q24	Programmable 16bits rotary magnetic encoder	QFN 24leads, 5 mm × 5 mm	Tube

NOTE Refer to the AEAT-8800-Q24 application note for the normal operation and OTP programming mode.

Optional OTP Programming Kit Ordering Information

Ordering Part Number	Product Description
HEDS-8988	AEAT-8800-Q24 magnetic encoder programming kit

For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

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