March 2015

FCD3400N80Z / FCU3400N80Z

N-Channel SuperFET® II MOSFET

800 V, 2 A, 3.4 Ω

Features

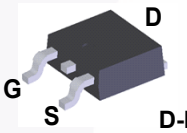
- $R_{DS(on)}$ = 2.75 Ω (Typ.)
- Ultra Low Gate Charge (Typ. Q_g = 7.4 nC)
- Low E_{oss} (Typ. 0.9 uJ @ 400V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 41 pF)
- 100% Avalanche Tested
- RoHS Compliant
- ESD Improved Capability

Description

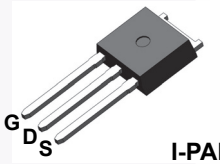
SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

Applications

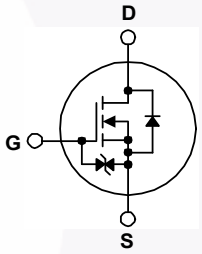
- AC - DC Power Supply
- LED Lighting



D-PAK



I-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCD3400N80Z FCU3400N80Z	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f > 1 Hz)	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	2.0	A
		- Continuous (T_C = 100°C)	1.2	
I_{DM}	Drain Current	- Pulsed (Note 1)	4.0	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	12.8	mJ
I_{AR}	Avalanche Current	(Note 1)	0.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	0.32	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt	(Note 3)	20	
P_D	Power Dissipation	(T_C = 25°C)	32	W
		- Derate Above 25°C	0.26	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCD3400N80Z FCU3400N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD3400N80Z	FCD340080Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FCU3400N80Z	FCU340080Z	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	-	0.9	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 640 V, V_{GS} = 0 V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	µA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.2 mA	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 1 A	-	2.75	3.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 1 A	-	2	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	299	400	pF
C_{oss}	Output Capacitance		-	12.7	15	pF
C_{rss}	Reverse Transfer Capacitance		-	0.36	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	6.2	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	41	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 640 V, I_D = 2 A, V_{GS} = 10 V (Note 4)	-	7.4	9.6	nC
Q_{gs}	Gate to Source Gate Charge		-	1.6	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	3.1	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	3.2	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 2 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	10	30	ns
t_r	Turn-On Rise Time		-	6.4	23	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22.7	55	ns
t_f	Turn-Off Fall Time		-	14	38	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	1.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	3.8	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2 A, dI_F/dt = 100 A/µs	-	119	-	ns
Q_{rr}	Reverse Recovery Charge		-	868	-	nC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 0.4 A, R_G = 25 Ω, starting T_J = 25°C
3. I_{SD} ≤ 2 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C
4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

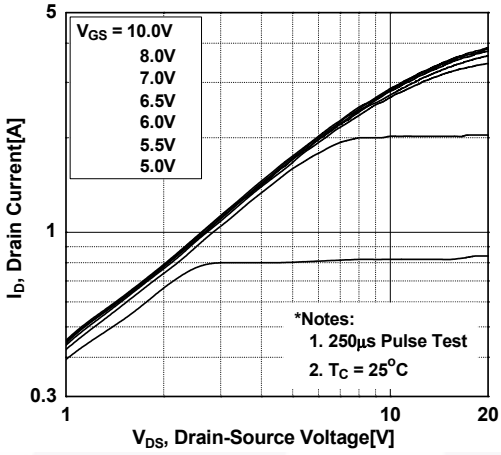


Figure 2. Transfer Characteristics

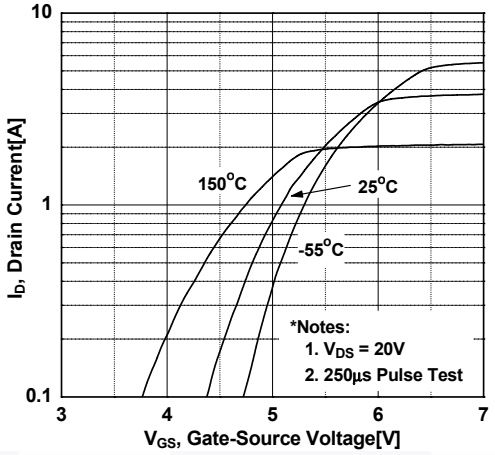


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

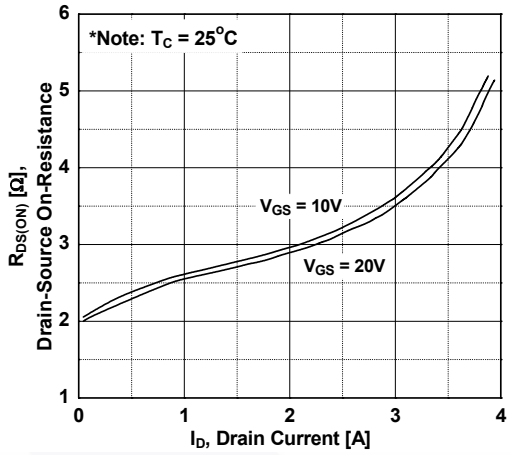


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

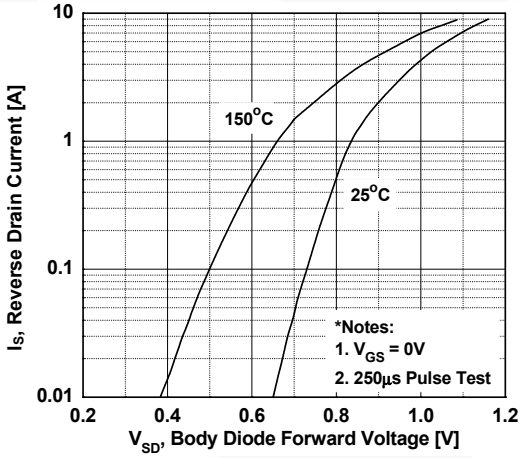


Figure 5. Capacitance Characteristics

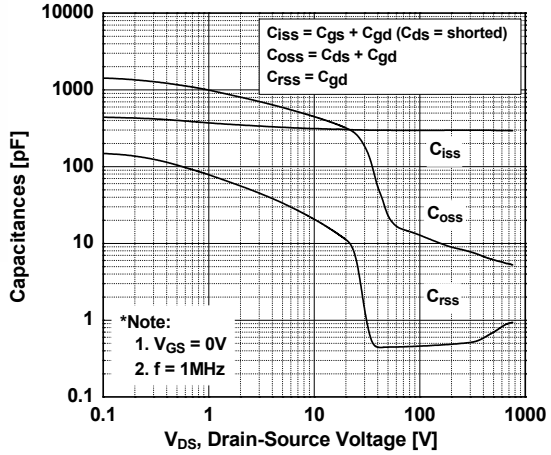
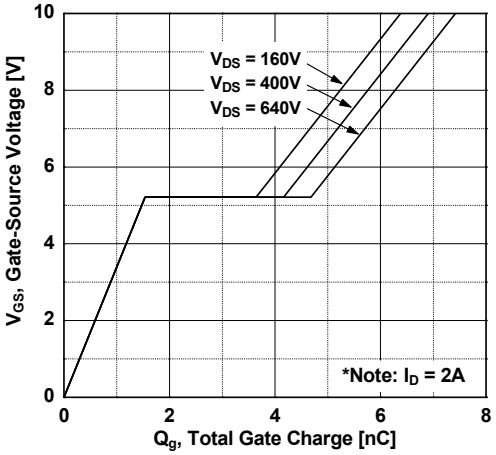


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

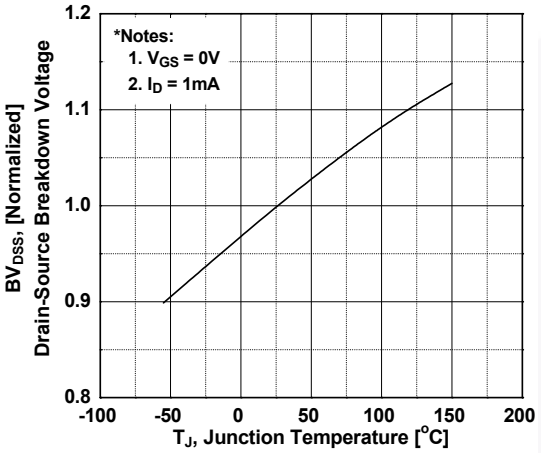


Figure 8. On-Resistance Variation vs. Temperature

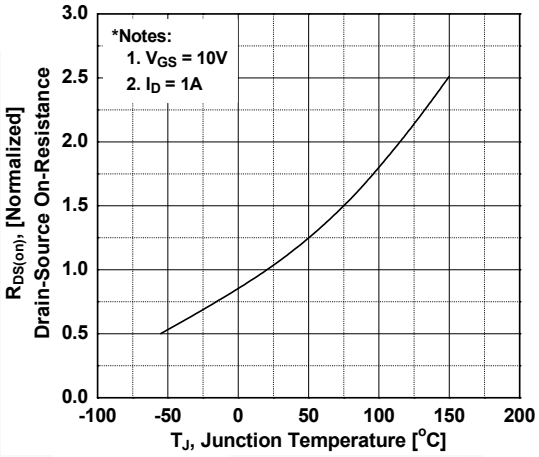


Figure 9. Maximum Safe Operating Area

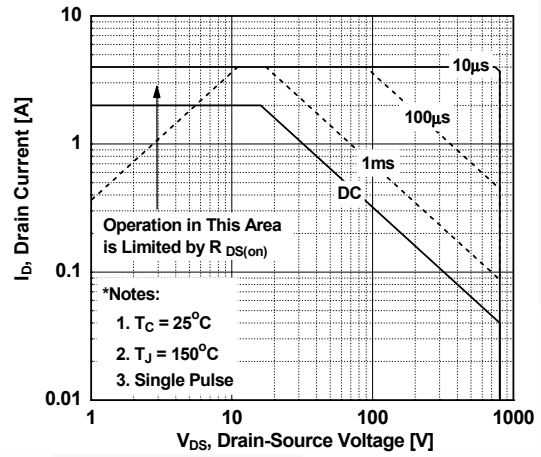


Figure 10. Maximum Drain Current vs. Case Temperature

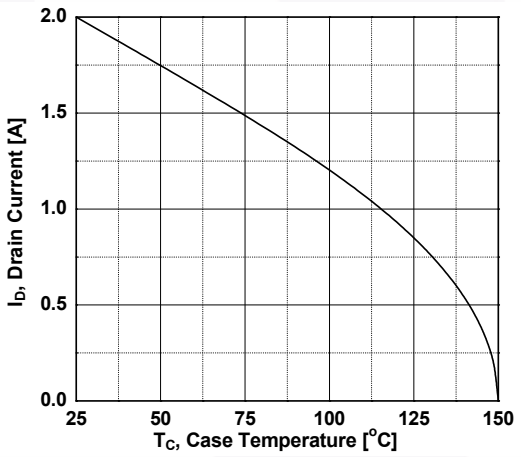
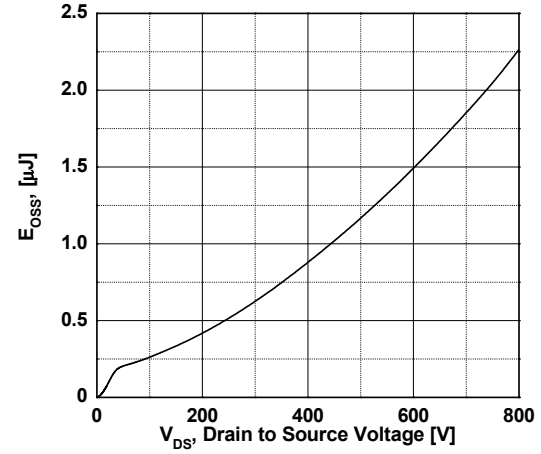
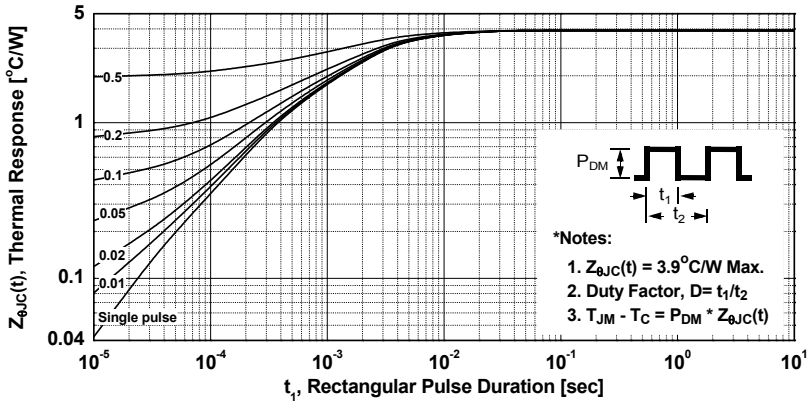


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



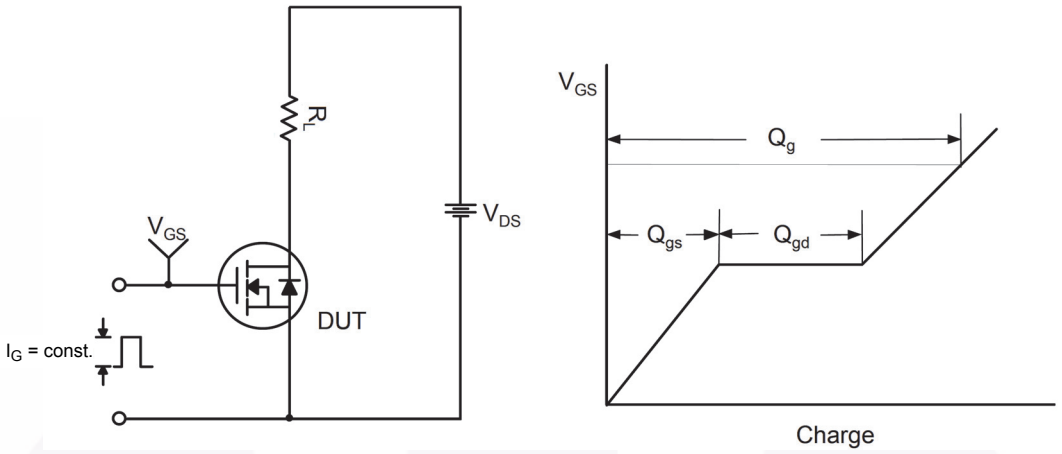


Fig 13. Gate Charge Test Circuit & Waveform

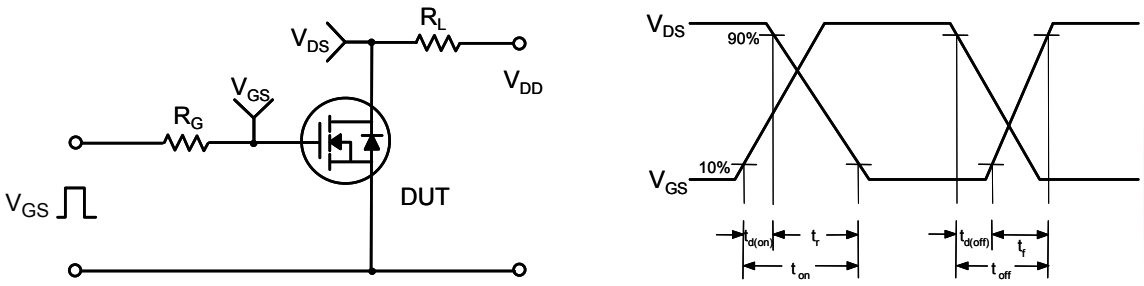


Fig 14. Resistive Switching Test Circuit & Waveforms

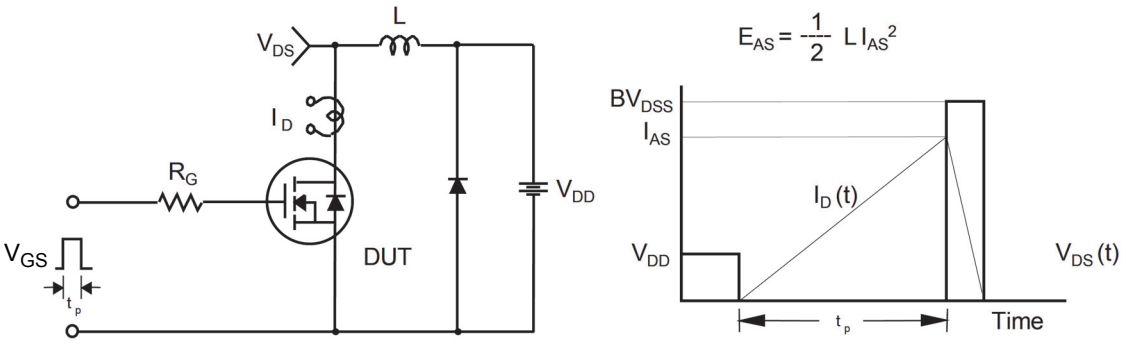


Fig 15. Unclamped Inductive Switching Test Circuit & Waveforms

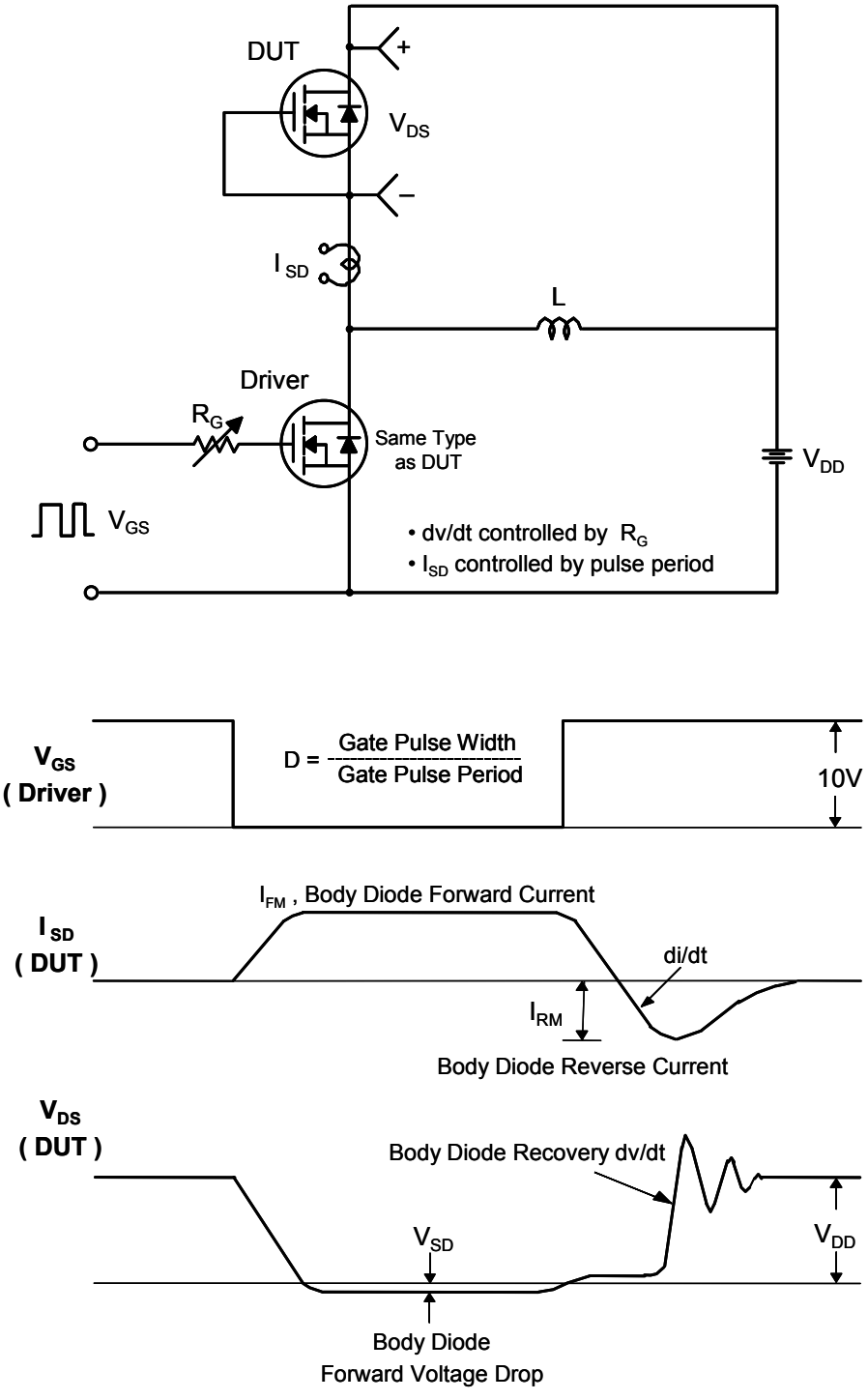
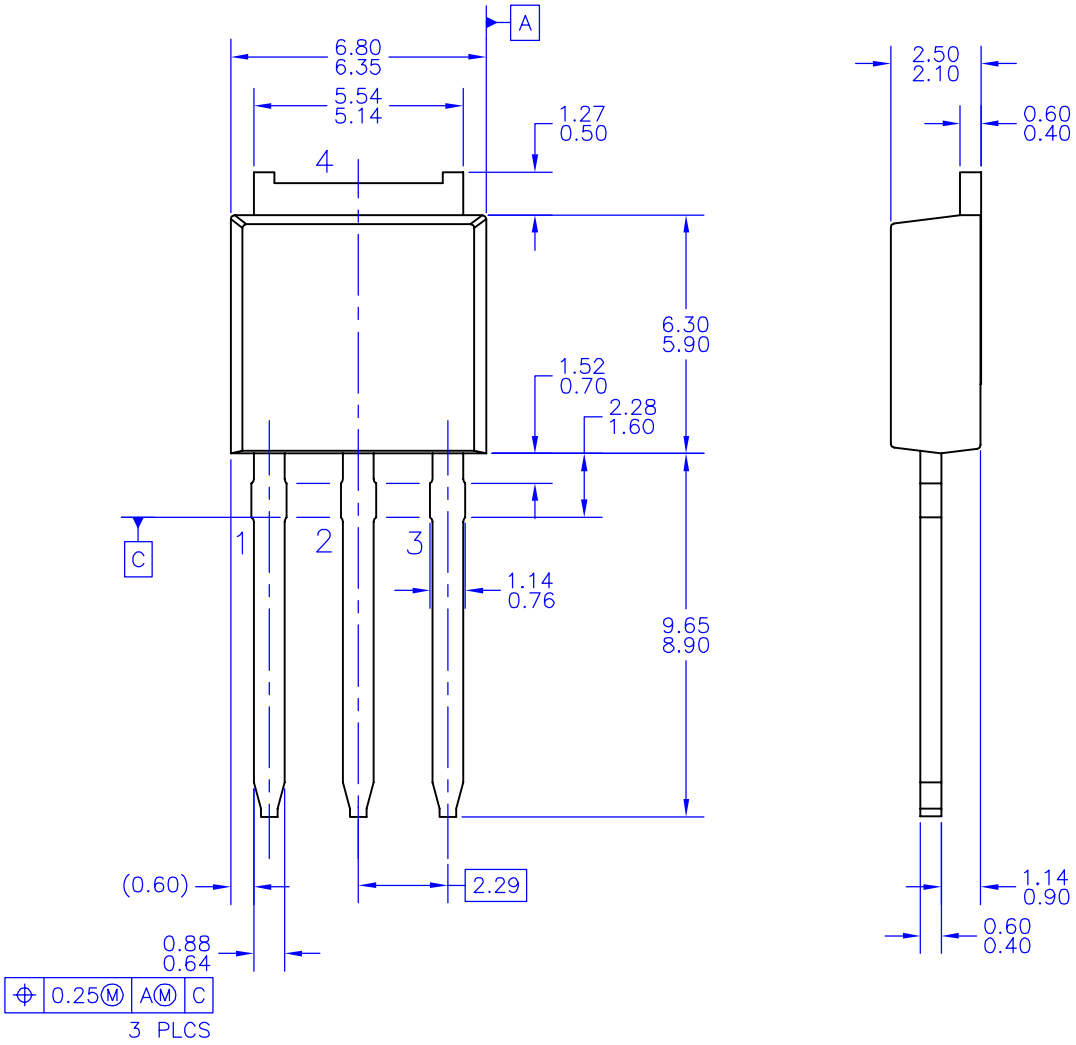


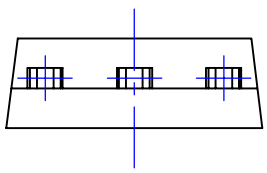
Fig 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

APPROVALS	DATE
DRAWN: J. GOMEZ	16MAR2001
CHECKED: R. MANABIT	
APPROVED: M. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

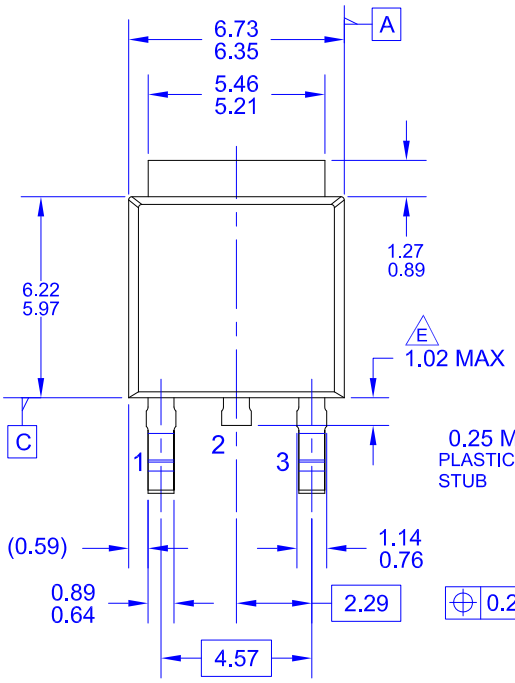
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TO-251 (I-PAK) MOLDED, 3 LEAD, OPTION AA

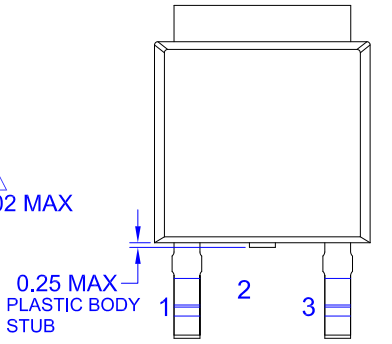
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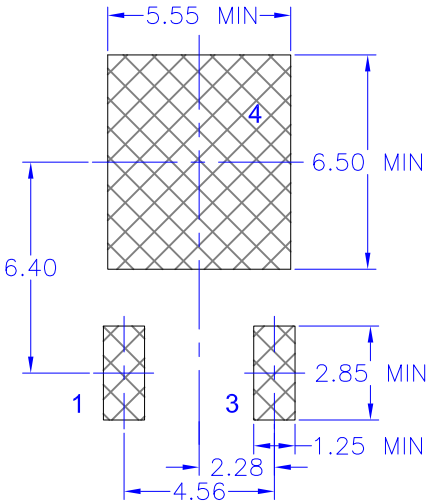
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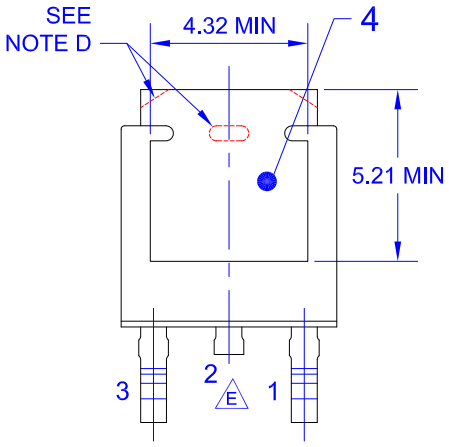
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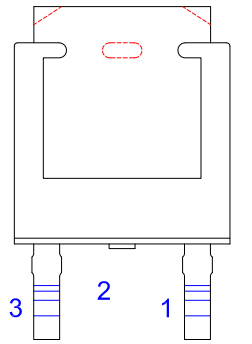
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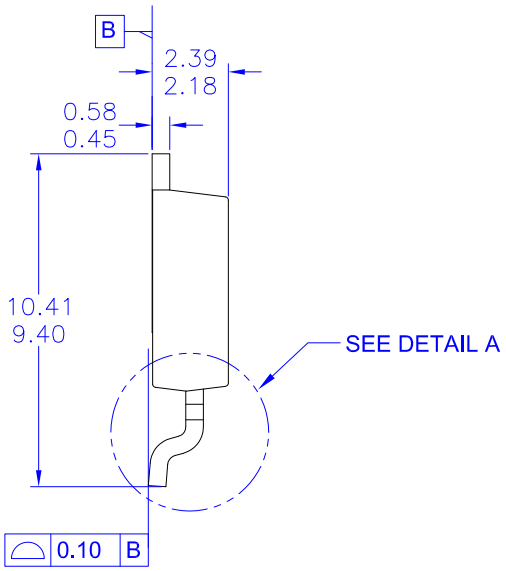
LAND PATTERN RECOMMENDATION



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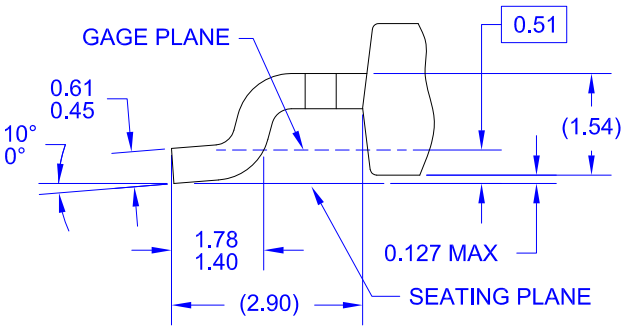


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C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



DETAIL A
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ANTI-COUNTERFEITING POLICY

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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