Blackfin+ Core Embedded Processor

Preliminary Technical Data ADSP-BF700/701/702/703/704/705/706/707

FEATURES

Blackfin+ core with up to 400 MHz performance
- **Dual 16-bit or single 32-bit MAC support per cycle**
- **16-bit complex MAC and many other instruction set enhancements**
- **Instruction set compatible with previous Blackfin products**

Low-cost packaging
- **88-Lead LFCSP (QFN) package (12 mm × 12mm), RoHS compliant**
- **184-Ball CSP_BGA package (12 mm × 12mm × 0.8mm pitch), RoHS compliant**

Low system power with < 100 mW total device power at 400 MHz (< 0.25 mW/MHz) at 25°C $T_{JUNCTION}$

PERIPHERALS FEATURES

See Figure 1, Processor Block Diagram and Table 1, Processor Comparison

MEMORY

136KB L1 SRAM with multi-parity-bit protection (64KB instruction, 64KB data, 8KB scratchpad)

Large on-chip L2 SRAM with ECC protection
- **256KB, 512KB, 1MB variants**

On-chip L2 ROM (512KB)

L3 interface (CSP_BGA only) optimized for lowest system power, providing 16-bit interface to DDR2 or LPDDR SDRAM devices (up to 200 MHz)

Security and one-time-programmable memory
- **Crypto hardware accelerators**
- **Fast secure boot for IP protection**
- **memDMA encryption/decryption for fast run-time security**

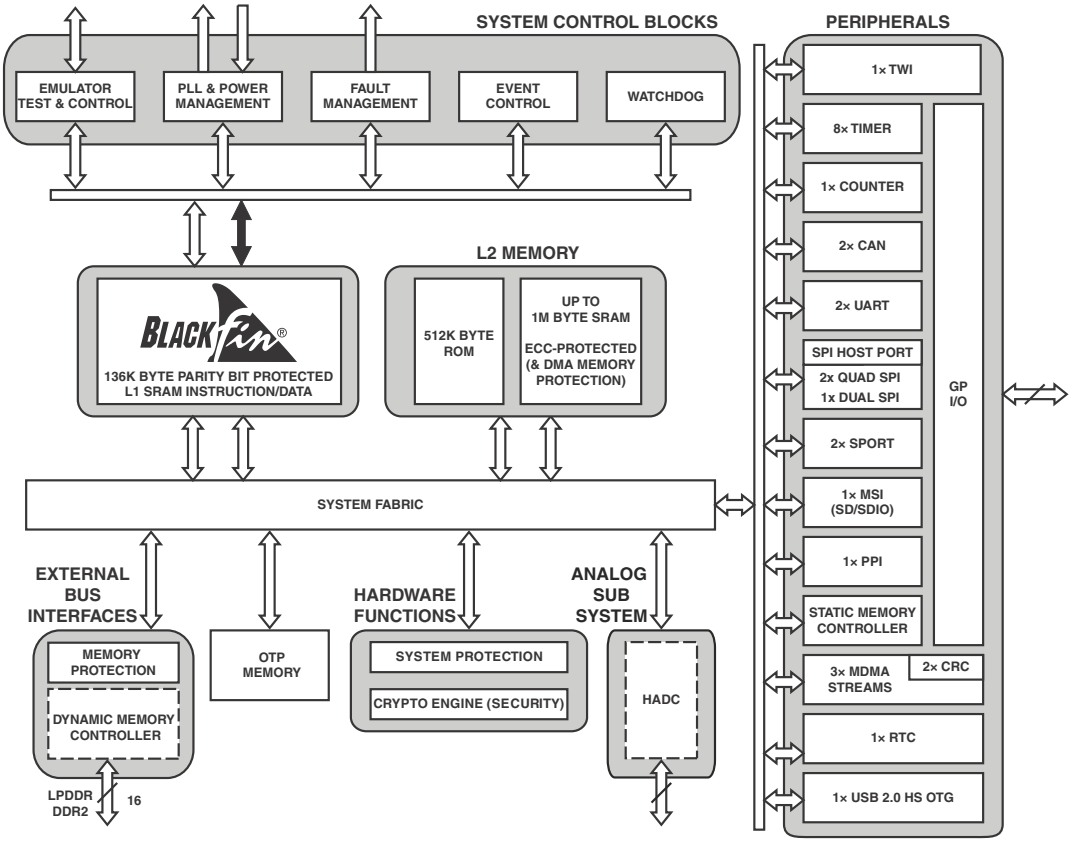


Figure 1. Processor Block Diagram

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Rev. PrC

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TABLE OF CONTENTS

Features 1
Peripherals Features 1
Memory 1
General Description 3
- Blackfin+ Processor Core 4
- Instruction Set Description 5
- Processor Infrastructure 5
- Memory Architecture 7
- Security Features 8
- Processor Safety Features 8
- Additional Processor Peripherals 9
- Power and Clock Management 12
- System Debug 14
- Development Tools 15
- Additional Information 16
- Related Signal Chains 16

ADSP-BF70x Detailed Signal Descriptions 17
184-Ball CSP_BGA Signal Descriptions 21
GP I/O Multiplexing for 184-Ball CSP_BGA 28
12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions 30
GP I/O Multiplexing for 12 mm × 12 mm 88-Lead LFCSP (QFN) 35
ADSP-BF70x Designer Quick Reference 37
Specifications 47
- Operating Conditions 47
- Electrical Characteristics 50
- HADC 52
- Package Information 53
- Absolute Maximum Ratings 53
- ESD Sensitivity 53
- Timing Specifications 54
- Output Drive Currents 90
- Test Conditions 90
- Environmental Conditions 91

ADSP-BF70x 184-Ball CSP_BGA Ball Assignments (Numerical by Ball Number) 92
ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Lead Assignments (Numerical by Lead Number) 95
Outline Dimensions 98
- Surface-Mount Design 99

Pre Release Products 100

REVISION HISTORY

05/14—Revision PrB to Revision PrC

Revised Processor Block Diagram 1
Added processors to Processor Comparison 3
Added Housekeeping ADC (HADC) 12
Added System Crossbars (SCB) 12
Added specs to Electrical Characteristics 50
Added HADC 52
Revised Timer Cycle Timing 67
Added thermal characteristic values to Environmental Conditions 91

GENERAL DESCRIPTION

The ADSP-BF70x processor is a member of the Blackfin family of products. The Blackfin processor combines a dual-MAC 16-bit state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture. New enhancements to the Blackfin+ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements—all while maintaining instruction set compatibility to previous Blackfin products.

The processor offers performance up to 400 MHz, as well as low static power consumption. Produced with a low-power and low-voltage design methodology, they provide world-class power management and performance.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the Blackfin processor is the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package. These applications span a wide array of markets, from automotive systems to embedded industrial, instrumentation, video/image analysis, biometric and power/motor control applications.

Table 1. Processor Comparison

Processor Feature	ADSP-BF700	ADSP-BF701	ADSP-BF702	ADSP-BF703	ADSP-BF704	ADSP-BF705	ADSP-BF706	ADSP-BF707
Maximum Speed Grade (MHz)[1]	200		400					
Maximum SYSCLK (MHz)	100		200					
Package Options	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA
GPIOs	43	47	43	47	43	47	43	47
Memory (bytes) L1 Instruction SRAM	48K							
Memory (bytes) L1 Instruction SRAM/Cache	16K							
Memory (bytes) L1 Data SRAM	32K							
Memory (bytes) L1 Data SRAM/Cache	32K							
Memory (bytes) L1 Scratchpad (L1 Data C)	8K							
Memory (bytes) L2 SRAM	128K		256K		512K		1024K	
Memory (bytes) L2 ROM	512K							
Memory (bytes) DDR2/LPDDR (16-bit)	No	Yes	No	Yes	No	Yes	No	Yes
I^2C	1							
Up/Down/Rotary Counter	1							
GP Timer	8							
GP Counter	1							
SPORTs	2							
Quad SPI	2							
Dual SPI	1							
SPI Host Port	1							
USB 2.0 HS OTG	1							
Parallel Peripheral Interface	1							
CAN	2							
UART	2							
Security Crypto Engine	Yes							
SD/SDIO (MSI)	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit
4-channel 10-bit ADC	No	Yes	No	Yes	No	Yes	No	Yes

[1] Other speed grades available.

BLACKFIN+ PROCESSOR CORE

As shown in Figure 1, the processor integrates a Blackfin+ processor core. The core, shown in Figure 2, contains two 16-bit multipliers, one 32-bit multiplier, two 40-bit accumulators (which may be used together as a 72-bit accumulator), two 40-bit ALUs, one 72-bit ALU, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

The core can perform two 16-bit by 16-bit multiply-accumulates or one 32-bit multiply-accumulate in each cycle. Signed and unsigned formats, rounding, saturation, and complex multiplies are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations,
16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If a second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

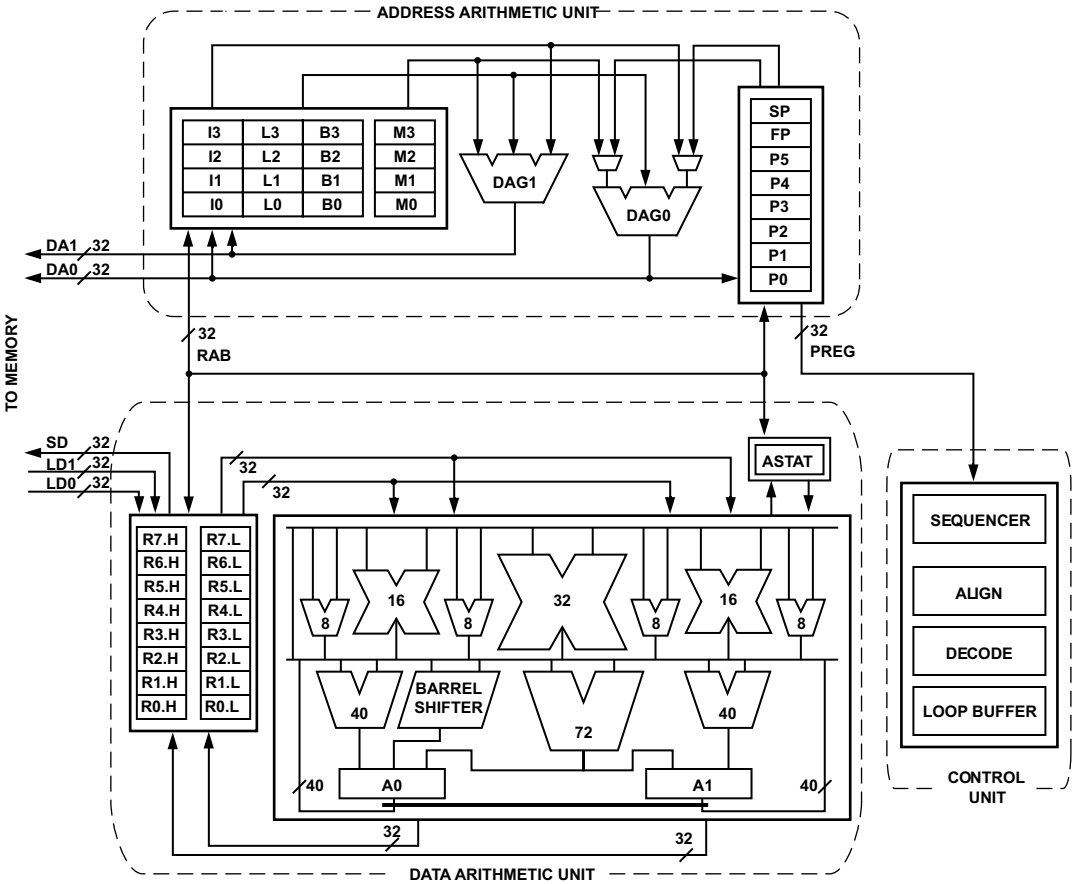


Figure 2. Blackfin+ Processor Core

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with dynamic branch prediction), and subroutine calls. Hardware supports zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

The Blackfin processor supports a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

INSTRUCTION SET DESCRIPTION

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. The Blackfin processor supports a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Control of all asynchronous and synchronous events to the processor is handled by two subsystems: the Core Event Controller (CEC) and the System Event Controller (SEC).
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADSP-BF70x processor.

DMA Controllers

The processor uses Direct Memory Access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processor can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory-to-memory DMA stream uses two channels, where one channel is the source channel, and the second is the destination channel.

All DMAs can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers, descriptor-based or register-based. Register-based DMA allows the processor to directly program DMA control registers to initiate a DMA transfer. On completion, the control registers may be automatically updated with their original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together and a DMA channel can be programmed to automatically set up and start another DMA transfer after the current sequence completes.

The DMA controller supports the following DMA operations.

- A single linear buffer that stops on completion.
- A linear buffer with negative, positive or zero stride length.
- A circular, auto-refreshing buffer that interrupts when each buffer becomes full.

- A similar buffer that interrupts on fractional buffers (for example, 1/2, 1/4).
- 1D DMA – uses a set of identical ping-pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address.
- 1D DMA – uses a linked list of 4 word descriptor sets containing a link pointer, an address, a length, and a configuration.
- 2D DMA – uses an array of one-word descriptor sets, specifying only the base DMA address.
- 2D DMA – uses a linked list of multi-word descriptor sets, specifying everything.

Event Handling

The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The processor provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated either by the software watchdog timer, by the $\overline{\text{NMI}}$ input signal to the processor, or by software. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

The SEC manages the enabling, prioritization, and routing of events from each system interrupt or fault source. Additionally, it provides notification and identification of the highest priority active system interrupt request to the core and routes system fault sources to its integrated fault management unit. The SEC triggers core general-purpose interrupt IVG11. It is recommended that IVG11 be set to allow self-nesting. The four lower priority interrupts (IVG15-12) may be used for software interrupts.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – A “write one to modify” mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers – Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Interrupts

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Three system-level interrupt channels (PINT0–3) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of 4 peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature – that is, when the

output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

MEMORY ARCHITECTURE

The processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency core-accessible memory as cache or SRAM, and larger, lower-cost and performance interface-accessible memory systems. See Figure 3.

Internal (Core-Accessible) Memory

The L1 memory system is the highest-performance memory available to the Blackfin+ processor core.

The core has its own private L1 memory. The modified Harvard architecture supports two concurrent 32-bit data accesses along with an instruction fetch at full processor speed which provides high-bandwidth processor performance. In the core, a 64K byte block of data memory partners with an 64K byte memory block for instruction storage. Each data block is multibanked for efficient data exchange through DMA and can be configured as SRAM. Alternatively, 16K bytes of each block can be configured in L1 cache mode. The four-way set-associative instruction cache and the 2 four-way set-associative data caches greatly accelerate memory access performance, especially when accessing external memories.

The L1 memory domain also features a 8K byte data SRAM block which is ideal for storing local variables and the software stack. All L1 memory is protected by a multi-parity-bit concept, regardless of whether the memory is operating in SRAM or cache mode.

Outside of the L1 domain, L2 and L3 memories are arranged using a Von Neumann topology. The L2 memory domain is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The L2 memory domain is accessible by the Blackfin+ core through a dedicated 64-bit interface. It operates at SYSCLK frequency.

The processor features up to 1M byte of L2 SRAM, which is ECC-protected and organized in eight banks. Individual banks can be made private to any system master. There is also a 512K byte single-bank ROM in the L2 domain. It contains boot code, security code, and general-purpose ROM space.

OTP Memory

The processor features 4KB of One-Time-Programmable (OTP) memory which is memory-map accessible. This memory stores a unique chip identification and is used to support secure-boot and secure operation.

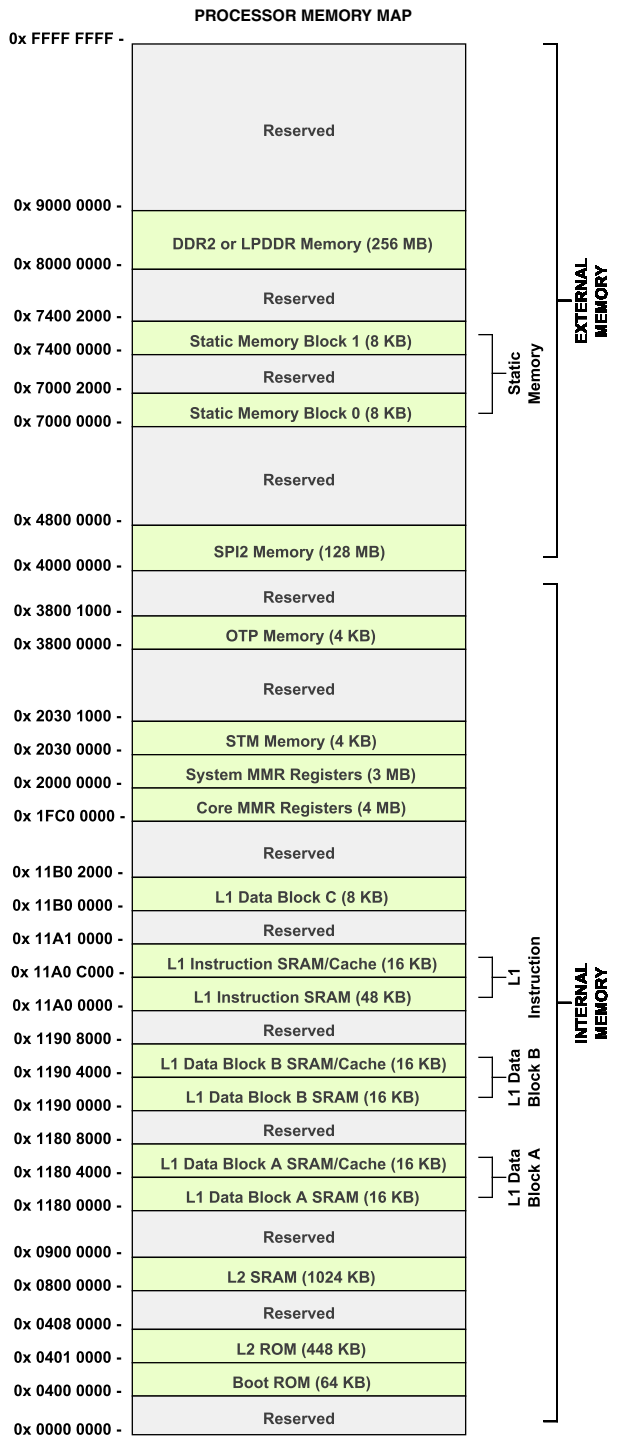


Figure 3. ADSP-BF706/ADSP-BF707 Internal/External Memory Map

Static Memory Controller (SMC)

The SMC can be programmed to control up to two blocks of external memories or memory-mapped devices, with very flexible timing parameters. Each block occupies a 8K byte segment regardless of the size of the device used.

Dynamic Memory Controller (DMC)

The DMC includes a controller that supports JESD79-2E compatible double-data-rate (DDR2) SDRAM and JESD209A low-power DDR (LPDDR) SDRAM devices. The DMC PHY features on-die termination on all data and data strobe pins that can be used during reads.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses in a region of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processor has several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE input pins dedicated for this purpose. There are two categories of boot modes. In master boot mode, the processor actively loads data from serial memories. In slave boot modes, the processor receives data from external host devices.

The boot modes are shown in Table 2. These modes are implemented by the SYS_BMODE bits of the reset configuration register and are sampled during power-on resets and software-initiated resets.

Table 2. Boot Modes

SYS_BMODE Setting	Boot Mode
00	No Boot/Idle
01	SPI2 Master
10	SPI2 Slave
11	UART0 Slave

SECURITY FEATURES

The ADSP-BF70x processor supports standards-based hardware-accelerated encryption, decryption, authentication, and true random number generation.

The following hardware-accelerated cryptographic ciphers are supported:

- AES in ECB, CBC, ICM and CTR modes with 128-, 192- and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key

The following hardware-accelerated hash functions are supported:

- SHA-1
- SHA-2 with 224-bit and 256-bit digest
- HMAC transforms for SHA-1 and SHA-2

Public Key Accelerator is available to offload computation-intensive public key cryptography operations.

Both a hardware-based non-deterministic random number generator and pseudo-random number generator are available. The TRNG also provides HW post-processing to meet NIST requirements of FIPS 140-2, while the PRNG is ANSI X9.31 compliant.

Secure boot is also available with 224-bit Elliptic Curve Digital Signatures ensuring integrity and authenticity of the boot stream. Optionally, confidentiality is also ensured via AES-128 encryption.

Secure Debug is also employed to allow only trusted users to access the system with debug tools.

PROCESSOR SAFETY FEATURES

The ADSP-BF70x processor has been designed for functional safety applications. While the level of safety is mainly dominated by the system concept, the following primitives are provided by the devices to build a robust safety concept.

Multi-Parity-Bit-Protected L1 Memories

In the processor's L1 memory space, whether SRAM or cache, each word is protected by multiple parity bits to detect the single event upsets that occur in all RAMs. This applies both to L1 instruction and data memory spaces.

ECC-Protected L2 Memories

Error correcting codes (ECC) are used to correct single event upsets. The L2 memory is protected with a Single Error Correct-Double Error Detect (SEC-DED) code. By default ECC is enabled, but it can be disabled on a per-bank basis. Single-bit errors are transparently corrected. Dual-bit errors can issue a system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2 and even L3 memories (DDR2, LPDDR). The processor features two CRC engines which are embedded in the memory-to-memory DMA

controllers. CRC checksums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Memory Protection

The Blackfin+ core features a memory protection concept, which grants data and/or instruction accesses to enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

The System Protection Unit (SPU) guards against accidental or unwanted access to a peripheral's MMR space by providing a write-protection mechanism. The user is able to choose and configure the peripherals that are protected as well as configure which ones of the four system MMR masters (core, memory DMA, the SPI host port and Coresight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write-protection functionality, the SPU is employed to define which resources in the system are secure or non-secure and to block access to secure resources from non-secure masters.

Synonymously, the System Memory Protection Unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are two SMPU units in the ADSP-BF70x processors. One is for the L2 memory and the other is for the external DDR memory.

The SMPU is also part of the security infrastructure. It allows the user to not only protect against arbitrary read and/or write transactions, but it also allows regions of memory to be defined as secure and prevent non-secure masters from accessing those memory regions.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or the core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the fault management unit of the SEC.

Watchdog

The on-chip software watchdog timer can supervise the Blackfin+ core.

Bandwidth Monitor

Memory-to-memory DMA channels are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The Watchdog Period mode monitors whether external signals toggle with a period within an expected range. The Watchdog Width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the GP counter can flag this to the processor or to the fault management unit of the SEC.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a "fault". Additionally, the system events can be defined as an interrupt to the core. If defined as such, the SEC forwards the event to the fault management unit, which may automatically reset the entire device for reboot, or simply toggle the SYS_FAULT output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken via a keyed sequence, to provide a final chance for the Blackfin+ core to resolve the issue and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processor contains high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not previously described.

Timers

The processor includes several timers which are described in the following sections.

General-Purpose Timers

There is one GP timer unit, and it provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TIMER_TMRx pins, an external TIMER_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer may also be started and/or stopped by any TRU master without core intervention.

Core Timer

The processor core also has its own dedicated timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Watchdog Timer

The core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value. This protects the system from remaining in an unknown state where software that would normally reset the timer has stopped running due to an external noise condition or software error.

After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in its timer control register that is set only upon a watchdog-generated reset.

Serial Ports (SPORTs)

Two synchronous serial ports (comprised of four "half-SPORTs") provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. Each half-SPORT is made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

General-Purpose Counters

A 32-bit counter is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumbwheel devices. All three pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

Parallel Peripheral Interface (PPI)

The processor provides a parallel peripheral interface (PPI) that supports data widths up to 18 bits. The PPI supports direct connection to TFT LCD panels, parallel analog-to-digital and digital-to-analog converters, video encoders and decoders, image sensor modules and other general-purpose peripherals.

The following features are supported in the PPI module:

- Programmable data length: 8 bits, 10 bits, 12 bits, 14 bits, 16 bits, and 18 bits per clock.
- Various framed, non-framed, and general-purpose operating modes. Frame syncs can be generated internally or can be supplied by an external device.
- ITU-656 status word error detection and correction for ITU-656 receive modes and ITU-656 preamble and status word decode.
- Optional packing and unpacking of data to/from 32 bits from/to 8 bits, 16 bits and 24 bits. If packing/unpacking is enabled, endianness can be configured to change the order of packing/unpacking of bytes/words.
- RGB888 can be converted to RGB666 or RGB565 for transmit modes.
- Various de-interleaving/interleaving modes for receiving/transmitting 4:2:2 YCrCb data.
- Configurable LCD data enable (DEN) output available on Frame Sync 3.

Serial Peripheral Interface (SPI) Ports

The processors have three industry-standard SPI-compatible ports that allow it to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, four-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An additional two (optional) data pins are provided to support quad SPI operation. Enhanced modes of operation such as flow control, fast mode and dual I/O

mode (DIOM) are also supported. In addition, a direct memory access (DMA) mode allows for transferring several words with minimal CPU interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other devices, acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI Ready pin which flexibly controls the transfers.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

SPI Host Port (SPIHP)

The processor includes one SPI Host Port which may be used in conjunction with any available SPI port to enhance its SPI slave mode capabilities. The SPIHP allows a SPI host device access to memory-mapped resources of the processor through a SPI SRAM/FLASH style protocol. The following features are included:

- Direct read/write of memory and memory-mapped registers
- Support for pre-fetch for faster reads
- Support for SPI controllers that implement hardware-based SPI memory protocol
- Error capture and reporting for protocol errors, bus errors, and over/underflow

UART Ports

The processor provides two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the Clear To Send (CTS) input and Request To Send (RTS) output with programmable assertion FIFO levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

TWI Controller Interface

The processor includes a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Media Storage Interface (MSI)

The media storage interface (MSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), and secure digital input/output cards (SDIO). The following list describes the main features of the MSI controller:

- Support for a single MMC, SD memory, SDIO card
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for eMMC 4.3 embedded NAND flash devices
- Support for power management and clock control
- An eleven-signal external interface with clock, command, optional interrupt, and up to eight data lines
- Card interface clock generation from SCLK0 or SCLK1
- SDIO interrupt and read wait features

Controller Area Network (CAN)

A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- CAN wakeup from hibernation mode (lowest static power consumption mode)
- Interrupts, including: TX complete, RX complete, error and global

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from a system clock through a programmable divider.

USB 2.0 On-the-Go Dual-Role Device Controller

The USB 2.0 OTG dual-role device controller provides a low-cost connectivity solution for the growing adoption of this bus standard in industrial applications, as well as consumer mobile devices such as cell phones, digital still cameras, and MP3 players. The USB 2.0 controller allows these devices to transfer data using a point-to-point USB connection without the need for a PC host. The module can operate in a traditional USB peripheral-only mode as well as the host mode presented in the On-the-Go (OTG) supplement to the USB 2.0 specification.

The USB clock is provided through a dedicated external crystal or crystal oscillator.

The USB On-the-Go dual-role device controller includes a Phase Locked Loop with programmable multipliers to generate the necessary internal clocking frequency for USB.

Housekeeping ADC (HADC)

The HADC provides a general-purpose, multi-channel successive approximation analog-to-digital converter. It supports the following features:

- 12-bit ADC core (10-bit accuracy) with built in sample and hold
- 4 single-ended input channels
- Throughput rates up to 1 MSPS
- Single external reference with analog inputs between 0 and 3.3 V
- Selectable ADC clock frequency including the ability to program a pre-scaler
- Adaptable conversion type: allows single or continuous conversion with option of autoscan
- Auto sequencing capability with up to 4 “autoconversions” in a single session. Each conversion can be programmed to select any input channel.
- Four data registers (individually addressable) to store conversion values

System Crossbars (SCB)

The System Crossbars (SCB) are the fundamental building blocks of a switch-fabric style for (on-chip) system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnect, which satisfies the performance and flexibility requirements of a specific system.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

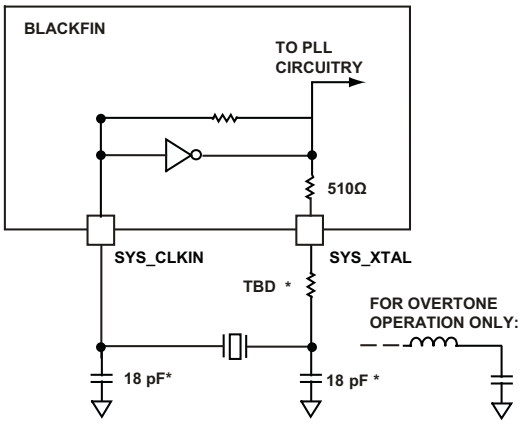
POWER AND CLOCK MANAGEMENT

The processor provides three operating modes, each with a different performance/power profile. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 5 for a summary of the power settings for each mode.

System Crystal Oscillator and USB Crystal Oscillator

The processor can be clocked by an external crystal, (Figure 4) a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor’s SYS_CLKIN pin. When an external clock is used, the SYS_XTAL pin must be left unconnected. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used.

For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor grade crystal is connected across the SYS_CLKIN and SYS_XTAL pins. The on-chip resistance between SYS_CLKIN and the SYS_XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 4. External Crystal Connection

The two capacitors and the series resistor shown in Figure 4 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the crystal manufacturers’ load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by

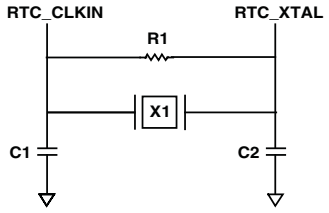
the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over the required temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) Using Third Overtone Crystals with the ADSP-218x DSP on the Analog Devices website (www.analog.com)—use site search on "EE-168". The same recommendations may be used for the USB crystal oscillator.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. Connect RTC pins RTC_CLKIN and RTC_XTAL with external components as shown in Figure 5.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3pF.

Figure 5. External Components for RTC

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a specific day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0 and SCLK1), the LPDDR or DDR2 clock (DCLK) and the output clock (OCLK).

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the V_{DD_EXT} pins. The rising edge of $\overline{\text{SYS_HWRST}}$ can be applied after all voltage supplies are within specifications, and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be output on the SYS_CLKOUT pin.

Table 3. Clock Dividers

Clock Source	Divider (if available on SYS_CLKOUT)
CCLK (core clock)	By 16
SYSCLK (System clock)	By 8
SCLK0 (system clock, all peripherals not covered by SCLK1)	Not available on SYS_CLKOUT
SCLK1 (system clock for crypto IP and MDMA)	By 8
DCLK (LPDDR/DDR2 clock)	By 8
OCLK (output clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
OTP Memory	V_{DD_OTP}

Table 4. Power Domains (Continued)

Power Domain	V_{DD} Range
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
All other I/O (includes SYS, JTAG, and Ports pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

See Table 5 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core and to all of the peripherals. This setting signals the external voltage regulator supplying the V_{DD_INT} pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation.

Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a non-volatile storage device (or self-refreshed DRAM) prior to removing power if the processor state is to be preserved.

Since the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or the core and is the result of a hardware- or software-triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with the core being ready to boot.

The Reset Control Unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when the core is reset (programs must ensure that there is no pending system activity involving the core when it is being reset).

From a system perspective reset is defined by both the reset target and the reset source as described below.

Target defined:

- Hardware Reset – All functional units are set to their default states without exception. History is lost.
- System Reset – All functional units except the RCU are set to their default states.
- Core-only Reset – Affects the core only. The system software should guarantee that the core, while in reset state, is not accessed by any bus master.

Source defined:

- Hardware Reset – The $\overline{\text{SYS_HWRST}}$ input signal is asserted active (pulled down).
- System Reset – May be triggered by software (writing to the RCU_CTL register) or by another functional unit such as the dynamic power management (DPM) unit (Hibernate) or any of the system event controller (SEC), trigger routing unit (TRU), or emulator inputs.
- Core-only Reset – Triggered by software.
- Trigger request (peripheral).

Voltage Regulation

The processor requires an external voltage regulator to power the V_{DD_INT} pins. To reduce standby power consumption, the external voltage regulator can be signaled through SYS_EXTWAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, all external supply pins (V_{DD_EXT}, V_{DD_USB}, V_{DD_DMC}) can still be powered, eliminating the need for external buffers. The external voltage regulator can be activated from this power down state by asserting the $\overline{\text{SYS_HWRST}}$ pin, which then initiates a boot sequence. SYS_EXTWAKE indicates a wakeup to the external voltage regulator.

SYSTEM DEBUG

The processor includes various features that allow for easy system debug. These are described in the following sections.

System Watchpoint Unit

The System Watchpoint Unit (SWU) is a single module which connects to a single system bus and provides for transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently, but share common event (interrupt, trigger and others) outputs.

Debug Access Port

DAP (Debug Access Port) provides IEEE-1149.1 JTAG interface support through its JTAG debug and Serial Wire debug Port (SWJ-DP). SWJ-DP is a combined JTAG-DP and SW-DP that enables either Serial Wire Debug (SWD) or a JTAG emulator to be connected to a target. SWD signals share the same pins as JTAG. There is an auto-detect mechanism that switches between JTAG-DP and SW-DP. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to MIPI System Trace Protocol version 2(STPv2).

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (CrossCore® Embedded Studio), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE, a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each DAP-enabled processor, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP), Serial Wire Debug Port (SWJ-DP), and Trace capabilities. In-circuit emulation is facilitated by use of the JTAG or SWD interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The emulators require the target board to include a header(s) that supports connection of the processor’s DAP to the emulator for trace and debug.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, contact the factory for more information.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF702/ADSP-BF703/ADSP-BF704/ADSP-BF705/ADSP-BF706/ADSP-BF707 processors can be accessed electronically on our website:

- *ADSP-BF70x Blackfin+ Processor Hardware Reference*
- *ADSP-BF70x Blackfin + Processor Programming Reference*
- *ADSP-BF70x Blackfin+ Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ADSP-BF70X DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n** Address bus
DMC_BAn	Output	**Bank Address Input n** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC_CAS}}$	Output	**Column Address Strobe** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC_CK}}$	Output	**Clock (complement)** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC_CSn}}$	Output	**Chip Select n** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n** Bi-directional Data bus
DMC_LDM	Output	**Data Mask for Lower Byte** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement)** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC_RAS}}$	Output	**Row Address Strobe** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement)** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC_WE}}$	Output	**Write Enable** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the WEb input of dynamic memory.
PPI_CLK	I/O	**Clock** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n** Bi-directional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC)** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC)** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD)** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n** Analog voltage inputs for digital conversion.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
HADC_VREFN	Input	**Ground Reference for ADC** Connect to an external voltage reference that meets data sheet specifications.
HADC_VREFP	Input	**External Reference for ADC** Connect to an external voltage reference that meets data sheet specifications.
MSI_CD	Input	**Card Detect** Connects to a pull-up resistor and to the card detect output of an SD socket.
MSI_CLK	Output	**Clock** The clock signal applied to the connected device from the MSI.
MSI_CMD	I/O	**Command** Used to send commands to and receive responses from the connected device.
MSI_Dn	I/O	**Data n** Bidirectional data bus.
MSI_INT	Input	**eSDIO Interrupt Input** Used only for eSDIO. Connects to an eSDIO card's interrupt output. An interrupt may be sampled even when the MSI clock to the card is switched off.
Px_nn	I/O	**Position n** General purpose input/output. See the GP Ports chapter of the HRM for programming information.
RTC_CLKIN	Input	**Crystal input / external oscillator connection** Connect to an external clock source or crystal.
RTC_XTAL	Output	**Crystal output** Drives an external crystal. Must be left unconnected if an external clock is driving RTC_CLKIN.
SMC_ABEn	Output	**Byte Enable n** Indicate whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1b=0 and SMC_ABE0b=1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1b=1 and SMC_ABE0b=0.
SMC_AMSn	Output	**Memory Select n** Typically connects to the chip select of a memory device.
SMC_AOE	Output	**Output Enable** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
SMC_ARE	Output	**Read Enable** Asserts at the beginning of a read access.
SMC_AWE	Output	**Write Enable** Asserts for the duration of a write access period.
SMC_Ann	Output	**Address n** Address bus
SMC_Dnn	I/O	**Data n** Bi-directional data bus
SPI_CLK	I/O	**Clock** Input in slave mode, output in master mode.
SPI_D2	I/O	**Data 2** Used to transfer serial data in Quad mode. Open-drain when ODM mode is enabled.
SPI_D3	I/O	**Data 3** Used to transfer serial data in Quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	I/O	**Master In, Slave Out** Used to transfer serial data. Operates in the same direction as SPI_MOSI in Dual and Quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	I/O	**Master Out, Slave In** Used to transfer serial data. Operates in the same direction as SPI_MISO in Dual and Quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	I/O	**Ready** Optional flow signal. Output in slave mode, input in master mode.
SPI_SELn	Output	**Slave Select Output n** Used in Master mode to enable the desired slave.
SPI_SS	Input	**Slave Select Input** Slave mode - Acts as the slave select input. Master mode- Optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	I/O	**Channel A Clock** Data and Frame Sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	I/O	**Channel A Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AD1	I/O	**Channel A Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AFS	I/O	**Channel A Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
SPT_BCLK	I/O	**Channel B Clock** Data and Frame Sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BD1	I/O	**Channel B Data 1** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BFS	I/O	**Channel B Frame Sync** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SYS_BMODEn	Input	**Boot Mode Control n** Selects the boot mode of the processor.
SYS_CLKIN	Input	**Clock/Crystal Input** Connect to an external clock source or crystal.
SYS_CLKOUT	Output	**Processor Clock Output** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the HRM for more details.
SYS_EXTWAKE	Output	**External Wake Control** Drives low during hibernate and high all other times. Typically connected to the enable input of the voltage regulator controlling the VDD_INT supply.
$\overline{\text{SYS_FAULT}}$	I/O	**Active-Low Fault Output** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS_HWRST}}$	Input	**Processor Hardware Reset Control** Resets the device when asserted.
$\overline{\text{SYS_NMI}}$	Input	**Non-maskable Interrupt** See the processor hardware and programming references for more details.
$\overline{\text{SYS_RESOUT}}$	Output	**Reset Output** Indicates that the device is in the reset state.
SYS_WAKEn	Input	**Power Saving Mode Wakeup n** Wake-up source input for deep sleep and/or hibernate mode.
SYS_XTAL	Output	**Crystal Output** Drives an external crystal. Must be left unconnected if an external clock is driving CLKIN.
JTG_SWCLK	I/O	**Serial Wire Clock** Clocks data into and out of the target during debug.
JTG_SWDIO	I/O	**Serial Wire DIO** Sends and receives serial data to and from the target during debug.
JTG_SWO	Output	**Serial Wire Out** Provides trace data to the emulator.
JTG_TCK	Input	**JTAG Clock** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select** JTAG test access port mode select.
$\overline{\text{JTG_TRST}}$	Input	**JTAG Reset** JTAG test access port reset.
TM_ACIn	Input	**Alternate Capture Input n** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLKn	Input	**Alternate Clock n** Provides an additional time base for use by an individual timer.
TM_CLK	Input	**Clock** Provides an additional global time base for use by all the GP timers.
TM_TMRn	I/O	**Timer n** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock** Clock output/
TRACE_Dnn	Output	**Trace Data n** Unidirectional data bus.
TWI_SCL	I/O	**Serial Clock** Clock output when master, clock input when slave
TWI_SDA	I/O	**Serial Data** Receives or transmits data
$\overline{\text{UART_CTS}}$	Input	**Clear to Send** Flow control signal.
$\overline{\text{UART_RTS}}$	Output	**Request to Send** Flow control signal.
$\overline{\text{UART_RX}}$	Input	**Receive** Receive input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART_TX}}$	Output	**Transmit** Transmit output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
USB_DM	I/O	**Data -** Bi-directional differential data line
USB_DP	I/O	**Data +** Bi-directional differential data line
USB_ID	Input	**OTG ID** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control** Controls an external voltage source to supply VBUS when in host mode. May be configured as open-drain. Polarity is configurable as well.
USB_VBUS	I/O	**Bus Voltage** Connects to bus voltage in host and device modes.
USB_XTAL	Output	**Crystal** Drives an external crystal. Must be left unconnected if an external clock is driving USB_CLKIN.

184-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name - The *Signal Name* column in the table includes the *Signal Name* for every pin and (where applicable) the *GP I/O Multiplexed Pin Function* for every pin.
- Description and Notes - The *Description* column in the table provides a verbose (descriptive) name for the signal.
- Type - The *Pin Type* column in the table identifies the I/O type or supply type of the pin.
- Type - The *Pin Type* column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (None), I/O (input/output), a (Analog), s (Supply), and g (Ground).
- Port - The *General-Purpose I/O Port* column in the table whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name - The *Pin Name* column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_BA0	DMC0 Bank Address Input 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address Input 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address Input 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0_CK}}$
$\overline{\text{DMC0_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0_LDQS}}$
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0_RAS}}$	DMC0 Row Address Strobe	Not Muxed	$\overline{\text{DMC0_RAS}}$
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0_UDQS}}$	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0_UDQS}}$
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
$\overline{\text{DMC0_WE}}$	DMC0 Write Enable	Not Muxed	$\overline{\text{DMC0_WE}}$
GND	Ground	Not Muxed	GND
GND_HADC	Ground HADC	Not Muxed	GND_HADC
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG_TRST}}$
$\overline{\text{MSI0_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
MSI0_D5	MSI0 Data 5	C	PC_11
MSI0_D6	MSI0 Data 6	C	PC_12
MSI0_D7	MSI0 Data 7	C	PC_13
$\overline{\text{MSI0_INT}}$	MSI0 eSDIO Interrupt Input	C	PC_14
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_14	Position 00 through Position 14	C	PC_00-PC_14
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input / external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0_AMS0}}$	SMC0 Memory Select 0	A	PA_15

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_AMS1	SMC0 Memory Select 1	A	PA_02
SMC0_AOE	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03
SMC0_ARE	SMC0 Read Enable	A	PA_13
SMC0_AWE	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_12
SMC0_D13	SMC0 Data 13	B	PB_13
SMC0_D14	SMC0 Data 14	B	PB_14
SMC0_D15	SMC0 Data 15	B	PB_15
SPI0_CLK	SPI0 Clock	B	PB_00
SPI0_CLK	SPI0 Clock	C	PC_04
SPI0_D2	SPI0 Data 2	B	PB_03
SPI0_D2	SPI0 Data 2	C	PC_08
SPI0_D3	SPI0 Data 3	B	PB_07
SPI0_D3	SPI0 Data 3	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	B	PB_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_06
SPI0_MOSI	SPI0 Master Out, Slave In	B	PB_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_07
SPI0_RDY	SPI0 Ready	A	PA_06
SPI0_SEL1	SPI0 Slave Select Output 1	A	PA_05
SPI0_SEL2	SPI0 Slave Select Output 2	A	PA_06
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_11
SPI0_SEL4	SPI0 Slave Select Output 4	B	PB_04
SPI0_SEL5	SPI0 Slave Select Output 5	B	PB_05
SPI0_SEL6	SPI0 Slave Select Output 6	B	PB_06
SPI0_SS	SPI0 Slave Select Input	A	PA_05
SPI1_CLK	SPI1 Clock	A	PA_00
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_01
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_02
SPI1_RDY	SPI1 Ready	A	PA_03
SPI1_SEL1	SPI1 Slave Select Output 1	A	PA_04
SPI1_SEL2	SPI1 Slave Select Output 2	A	PA_03
SPI1_SEL3	SPI1 Slave Select Output 3	C	PC_10

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPI1_SEL4	SPI1 Slave Select Output 4	A	PA_14
SPI1_SS	SPI1 Slave Select Input	A	PA_04
SPI2_CLK	SPI2 Clock	B	PB_10
SPI2_D2	SPI2 Data 2	B	PB_13
SPI2_D3	SPI2 Data 3	B	PB_14
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_11
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_12
SPI2_RDY	SPI2 Ready	A	PA_04
SPI2_SEL1	SPI2 Slave Select Output 1	B	PB_15
SPI2_SEL2	SPI2 Slave Select Output 2	B	PB_08
SPI2_SEL3	SPI2 Slave Select Output 3	B	PB_09
SPI2_SS	SPI2 Slave Select Input	B	PB_15
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	C	PC_08
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_00
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_05
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	A	PA_15
SPT0_BCLK	SPORT0 Channel B Clock	B	PB_04
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_04
SPT0_BD0	SPORT0 Channel B Data 0	B	PB_05
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_06
SPT0_BD1	SPORT0 Channel B Data 1	B	PB_07
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_01
SPT0_BFS	SPORT0 Channel B Frame Sync	B	PB_06
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_07
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	A	PA_15
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_08
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_10
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_11
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_09
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	A	PA_07
SPT1_BCLK	SPORT1 Channel B Clock	B	PB_00
SPT1_BCLK	SPORT1 Channel B Clock	C	PC_10
SPT1_BD0	SPORT1 Channel B Data 0	B	PB_02
SPT1_BD0	SPORT1 Channel B Data 0	C	PC_12
SPT1_BD1	SPORT1 Channel B Data 1	B	PB_03
SPT1_BD1	SPORT1 Channel B Data 1	C	PC_13
SPT1_BFS	SPORT1 Channel B Frame Sync	B	PB_01
SPT1_BFS	SPORT1 Channel B Frame Sync	C	PC_11
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	A	PA_07
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	C	PC_14
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_FAULT	Active-Low Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Non-maskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_WAKE0	Power Saving Mode Wakeup 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wakeup 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wakeup 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wakeup 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wakeup 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
UART0_CTS	UART0 Clear to Send	C	PC_03
UART0_RTS	UART0 Request to Send	C	PC_02

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
UART0_RX	UART0 Receive	B	PB_09
UART0_TX	UART0 Transmit	B	PB_08
UART1_CTS	UART1 Clear to Send	B	PB_14
UART1_RTS	UART1 Request to Send	B	PB_13
UART1_RX	UART1 Receive	C	PC_01
UART1_TX	UART1 Transmit	C	PC_00
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data -	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB0_XTAL
VDD_DMC	VDD for DMC	Not Muxed	VDD_DMC
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_HADC	VDD for HADC	Not Muxed	VDD_HADC
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_OTP	VDD for OTP	Not Muxed	VDD_OTP
VDD_RTC	VDD for RTC	Not Muxed	VDD_RTC
VDD_USB	VDD for USB	Not Muxed	VDD_USB

GP I/O MULTIPLEXING FOR 184-BALL CSP_BGA

Table 8 through Table 10 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 184-Ball CSP_BGA package.

Table 8. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	SPI1_CLK		TRACE0_D07	SMC0_ABE0	
PA_01	SPI1_MISO		TRACE0_D06	SMC0_ABE1	
PA_02	SPI1_MOSI		TRACE0_D05	SMC0_AMS1	
PA_03	SPI1_SEL2	SPI1_RDY		SMC0_ARDY	
PA_04	SPI1_SEL1	TM0_TMR7	SPI2_RDY	SMC0_A08	SPI1_SS
PA_05	TM0_TMR0	SPI0_SEL1		SMC0_A07	SPI0_SS
PA_06	TM0_TMR1	SPI0_SEL2	SPI0_RDY	SMC0_A06	
PA_07	TM0_TMR2	SPT1_BTDV	SPT1_ATDV	SMC0_A05	CNT0_DG
PA_08	PPI0_D11	MSI0_CD	SPT1_ACLK	SMC0_A01	
PA_09	PPI0_D10	TM0_TMR4	SPT1_AFS	SMC0_A02	
PA_10	PPI0_D09	TM0_TMR5	SPT1_AD0	SMC0_A03	
PA_11	PPI0_D08	TM0_TMR6	SPT1_AD1	SMC0_A04	
PA_12	PPI0_FS1	CAN1_RX		SMC0_AOE	TM0_ACI6/SYS_WAKE4
PA_13	PPI0_FS2	CAN1_TX		SMC0_ARE	CNT0_ZM
PA_14	PPI0_CLK	SPI1_SEL4		SMC0_AWE	TM0_ACLK5
PA_15	PPI0_FS3	SPT0_ATDV	SPT0_BTDV	SMC0_AMS0	CNT0_UD

Table 9. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PPI0_D07	SPT1_BCLK	SPI0_CLK	SMC0_D07	TM0_ACLK3
PB_01	PPI0_D06	SPT1_BFS	SPI0_MISO	SMC0_D06	TM0_ACI1
PB_02	PPI0_D05	SPT1_BD0	SPI0_MOSI	SMC0_D05	
PB_03	PPI0_D04	SPT1_BD1	SPI0_D2	SMC0_D04	
PB_04	PPI0_D03	SPT0_BCLK	SPI0_SEL4	SMC0_D03	TM0_ACLK6
PB_05	PPI0_D02	SPT0_BD0	SPI0_SEL5	SMC0_D02	
PB_06	PPI0_D01	SPT0_BFS	SPI0_SEL6	SMC0_D01	TM0_CLK
PB_07	PPI0_D00	SPT0_BD1	SPI0_D3	SMC0_D00	SYS_WAKE0
PB_08	UART0_TX	PPI0_D16	SPI2_SEL2	SMC0_D08	SYS_WAKE1
PB_09	UART0_RX	PPI0_D17	SPI2_SEL3	SMC0_D09	TM0_ACI3
PB_10	SPI2_CLK		TRACE0_CLK	SMC0_D10	TM0_ACLK4
PB_11	SPI2_MISO		TRACE0_D04	SMC0_D11	
PB_12	SPI2_MOSI		TRACE0_D03	SMC0_D12	SYS_WAKE2
PB_13	SPI2_D2	UART1_RTS	TRACE0_D02	SMC0_D13	
PB_14	SPI2_D3	UART1_CTS	TRACE0_D01	SMC0_D14	
PB_15	SPI2_SEL1		TRACE0_D00	SMC0_D15	SPI2_SS

Table 10. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	UART1_TX	SPT0_AD1	PPI0_D15		
PC_01	UART1_RX	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	UART0_RTS	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	UART0_CTS	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	SPI1_SEL3		TM0_ACLK1
PC_11	SPT1_BFS	MSI0_D5	SPI0_SEL3		
PC_12	SPT1_BD0	MSI0_D6			
PC_13	SPT1_BD1	MSI0_D7			
PC_14	SPT1_BTDV	MSI0_INT			

12 MM × 12 MM 88-LEAD LFCSP (QFN) SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 11. The columns in this table provide the following information:

- Signal Name - The *Signal Name* column in the table includes the *Signal Name* for every pin and (where applicable) the *GP I/O Multiplexed Pin Function* for every pin.
- Description and Notes - The *Description* column in the table provides a verbose (descriptive) name for the signal.
- Type - The *Pin Type* column in the table identifies the I/O type or supply type of the pin.
- Type - The *Pin Type* column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (None), I/O (input/output), a (Analog), s (Supply), and g (Ground).
- Port - The *General-Purpose I/O Port* column in the table whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name - The *Pin Name* column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
GND	Ground	Not Muxed	GND
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG_TRST}}$
$\overline{\text{MSI0_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_10	Position 00 through Position 10	C	PC_00-PC_10
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input / external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03
$\overline{\text{SMC0_ARE}}$	SMC0 Read Enable	A	PA_13
$\overline{\text{SMC0_AWE}}$	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_12
SMC0_D13	SMC0 Data 13	B	PB_13
SMC0_D14	SMC0 Data 14	B	PB_14
SMC0_D15	SMC0 Data 15	B	PB_15
SPI0_CLK	SPI0 Clock	B	PB_00
SPI0_CLK	SPI0 Clock	C	PC_04
SPI0_D2	SPI0 Data 2	B	PB_03
SPI0_D2	SPI0 Data 2	C	PC_08
SPI0_D3	SPI0 Data 3	B	PB_07
SPI0_D3	SPI0 Data 3	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	B	PB_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_06
SPI0_MOSI	SPI0 Master Out, Slave In	B	PB_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_07
SPI0_RDY	SPI0 Ready	A	PA_06
$\overline{\text{SPI0_SEL1}}$	SPI0 Slave Select Output 1	A	PA_05
$\overline{\text{SPI0_SEL2}}$	SPI0 Slave Select Output 2	A	PA_06
$\overline{\text{SPI0_SEL4}}$	SPI0 Slave Select Output 4	B	PB_04
$\overline{\text{SPI0_SEL5}}$	SPI0 Slave Select Output 5	B	PB_05
$\overline{\text{SPI0_SEL6}}$	SPI0 Slave Select Output 6	B	PB_06
$\overline{\text{SPI0_SS}}$	SPI0 Slave Select Input	A	PA_05
SPI1_CLK	SPI1 Clock	A	PA_00
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_01
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_02
SPI1_RDY	SPI1 Ready	A	PA_03
$\overline{\text{SPI1_SEL1}}$	SPI1 Slave Select Output 1	A	PA_04
$\overline{\text{SPI1_SEL2}}$	SPI1 Slave Select Output 2	A	PA_03
$\overline{\text{SPI1_SEL3}}$	SPI1 Slave Select Output 3	C	PC_10
$\overline{\text{SPI1_SEL4}}$	SPI1 Slave Select Output 4	A	PA_14
$\overline{\text{SPI1_SS}}$	SPI1 Slave Select Input	A	PA_04
SPI2_CLK	SPI2 Clock	B	PB_10
SPI2_D2	SPI2 Data 2	B	PB_13
SPI2_D3	SPI2 Data 3	B	PB_14
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_11
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_12
SPI2_RDY	SPI2 Ready	A	PA_04
$\overline{\text{SPI2_SEL1}}$	SPI2 Slave Select Output 1	B	PB_15
$\overline{\text{SPI2_SEL2}}$	SPI2 Slave Select Output 2	B	PB_08
$\overline{\text{SPI2_SEL3}}$	SPI2 Slave Select Output 3	B	PB_09
$\overline{\text{SPI2_SS}}$	SPI2 Slave Select Input	B	PB_15
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	C	PC_08

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_00
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_05
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	A	PA_15
SPT0_BCLK	SPORT0 Channel B Clock	B	PB_04
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_04
SPT0_BD0	SPORT0 Channel B Data 0	B	PB_05
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_06
SPT0_BD1	SPORT0 Channel B Data 1	B	PB_07
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_01
SPT0_BFS	SPORT0 Channel B Frame Sync	B	PB_06
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_07
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	A	PA_15
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_08
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_10
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_11
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_09
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	A	PA_07
SPT1_BCLK	SPORT1 Channel B Clock	B	PB_00
SPT1_BCLK	SPORT1 Channel B Clock	C	PC_10
SPT1_BD0	SPORT1 Channel B Data 0	B	PB_02
SPT1_BD1	SPORT1 Channel B Data 1	B	PB_03
SPT1_BFS	SPORT1 Channel B Frame Sync	B	PB_01
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	A	PA_07
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE
$\overline{\text{SYS_FAULT}}$	Active-Low Fault Output	Not Muxed	$\overline{\text{SYS_FAULT}}$
$\overline{\text{SYS_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS_HWRST}}$
$\overline{\text{SYS_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS_NMI}}$
$\overline{\text{SYS_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS_RESOUT}}$
SYS_WAKE0	Power Saving Mode Wakeup 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wakeup 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wakeup 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wakeup 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wakeup 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0_CTS}}$	UART0 Clear to Send	C	PC_03
$\overline{\text{UART0_RTS}}$	UART0 Request to Send	C	PC_02
$\overline{\text{UART0_RX}}$	UART0 Receive	B	PB_09
$\overline{\text{UART0_TX}}$	UART0 Transmit	B	PB_08
$\overline{\text{UART1_CTS}}$	UART1 Clear to Send	B	PB_14
$\overline{\text{UART1_RTS}}$	UART1 Request to Send	B	PB_13
$\overline{\text{UART1_RX}}$	UART1 Receive	C	PC_01
$\overline{\text{UART1_TX}}$	UART1 Transmit	C	PC_00
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data -	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB0_XTAL
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_OTP	VDD for OTP	Not Muxed	VDD_OTP
VDD_RTC	VDD for RTC	Not Muxed	VDD_RTC
VDD_USB	VDD for USB	Not Muxed	VDD_USB

GP I/O MULTIPLEXING FOR 12 MM × 12 MM 88-LEAD LFCSP (QFN)

Table 12 through Table 14 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 12 mm × 12 mm 88-Lead LFCSP (QFN) package.

Table 12. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	SPI1_CLK		TRACE0_D07	SMC0_ABE0	
PA_01	SPI1_MISO		TRACE0_D06	SMC0_ABE1	
PA_02	SPI1_MOSI		TRACE0_D05	SMC0_AMS1	
PA_03	SPI1_SEL2	SPI1_RDY		SMC0_ARDY	
PA_04	SPI1_SEL1	TM0_TMR7	SPI2_RDY	SMC0_A08	SPI1_SS
PA_05	TM0_TMR0	SPI0_SEL1		SMC0_A07	SPI0_SS
PA_06	TM0_TMR1	SPI0_SEL2	SPI0_RDY	SMC0_A06	
PA_07	TM0_TMR2	SPT1_BTDV	SPT1_ATDV	SMC0_A05	CNT0_DG
PA_08	PPI0_D11	MSI0_CD	SPT1_ACLK	SMC0_A01	
PA_09	PPI0_D10	TM0_TMR4	SPT1_AFS	SMC0_A02	
PA_10	PPI0_D09	TM0_TMR5	SPT1_AD0	SMC0_A03	
PA_11	PPI0_D08	TM0_TMR6	SPT1_AD1	SMC0_A04	
PA_12	PPI0_FS1	CAN1_RX		SMC0_AOE	TM0_ACI6/SYS_WAKE4
PA_13	PPI0_FS2	CAN1_TX		SMC0_ARE	CNT0_ZM
PA_14	PPI0_CLK	SPI1_SEL4		SMC0_AWE	TM0_ACLK5
PA_15	PPI0_FS3	SPT0_ATDV	SPT0_BTDV	SMC0_AMS0	CNT0_UD

Table 13. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PPI0_D07	SPT1_BCLK	SPI0_CLK	SMC0_D07	TM0_ACLK3
PB_01	PPI0_D06	SPT1_BFS	SPI0_MISO	SMC0_D06	TM0_ACI1
PB_02	PPI0_D05	SPT1_BD0	SPI0_MOSI	SMC0_D05	
PB_03	PPI0_D04	SPT1_BD1	SPI0_D2	SMC0_D04	
PB_04	PPI0_D03	SPT0_BCLK	SPI0_SEL4	SMC0_D03	TM0_ACLK6
PB_05	PPI0_D02	SPT0_BD0	SPI0_SEL5	SMC0_D02	
PB_06	PPI0_D01	SPT0_BFS	SPI0_SEL6	SMC0_D01	TM0_CLK
PB_07	PPI0_D00	SPT0_BD1	SPI0_D3	SMC0_D00	SYS_WAKE0
PB_08	UART0_TX	PPI0_D16	SPI2_SEL2	SMC0_D08	SYS_WAKE1
PB_09	UART0_RX	PPI0_D17	SPI2_SEL3	SMC0_D09	TM0_ACI3
PB_10	SPI2_CLK		TRACE0_CLK	SMC0_D10	TM0_ACLK4
PB_11	SPI2_MISO		TRACE0_D04	SMC0_D11	
PB_12	SPI2_MOSI		TRACE0_D03	SMC0_D12	SYS_WAKE2
PB_13	SPI2_D2	UART1_RTS	TRACE0_D02	SMC0_D13	
PB_14	SPI2_D3	UART1_CTS	TRACE0_D01	SMC0_D14	
PB_15	SPI2_SEL1		TRACE0_D00	SMC0_D15	SPI2_SS

Table 14. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	UART1_TX	SPT0_AD1	PPI0_D15		
PC_01	UART1_RX	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	UART0_RTS	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	UART0_CTS	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	SPI1_SEL3		TM0_ACLK1

ADSP-BF70X DESIGNER QUICK REFERENCE

Table 15 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name - The *Signal Name* column in the table includes the *Signal Name* for every pin and (where applicable) the *GP I/O Multiplexed Pin Function* for every pin.
- Type - The *Pin Type* column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (None), I/O (input/output), a (Analog), s (Supply), and g (Ground).
- Driver Type - The *Driver Type* column in the table identifies the driver type used by the pin. The driver types are defined in the Output Drive currents section of this data sheet.
- Int Term - The *Internal Termination* column in the table specifies the termination present when the processor is not in the reset or hibernate state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up), or pd (Pull-down).
- Reset Term - The *Reset Termination* column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up), or pd (Pull-down).
- Reset Drive - The *Reset Drive* column in the table specifies the active drive on the signal when the processor is in the reset state.
- Hiber Term - The *Hibernate Termination* column in the table specifies the termination present when the processor is in the hibernate state. The abbreviations used in this column are wk (Weak Keeper, weakly retains previous value driven on the pin), pu (Pull-up), or pd (Pull-down).
- Hiber Drive - The *Hibernate Drive* column in the table specifies the active drive on the signal when the processor is in the hibernate state.
- Power Domain - The *Power Domain* column in the table specifies the power supply domain in which the signal resides.
- Description and Notes - The *Description and Notes* column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Note that for Ports A, B, and C (PA00 to PC14), when $\overline{\text{SYS_HWRST}}$ is low, these pads are three-state. After $\overline{\text{SYS_HWRST}}$ is released, but before code execution begins, these pins are internally pulled up. Subsequently, the state depends on the input enable and output enable which are controlled by software.

Table 15. ADSP-BF70x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 0 Notes: No notes
DMC0_A01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 1 Notes: No notes
DMC0_A02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 2 Notes: No notes
DMC0_A03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 3 Notes: No notes
DMC0_A04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 4 Notes: No notes
DMC0_A05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 5 Notes: No notes
DMC0_A06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 6 Notes: No notes
DMC0_A07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 7 Notes: No notes
DMC0_A08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 8 Notes: No notes
DMC0_A09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 9 Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 10 Notes: No notes
DMC0_A11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 11 Notes: No notes
DMC0_A12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 12 Notes: No notes
DMC0_A13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 13 Notes: No notes
DMC0_BA0	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 0 Notes: No notes
DMC0_BA1	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 1 Notes: No notes
DMC0_BA2	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 2 Notes: For LPDDR leave unconnected.
$\overline{\text{DMC0_CAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes
DMC0_CK	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes
$\overline{\text{DMC0_CK}}$	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock (complement) Notes: No notes
DMC0_CKE	I/O	B	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock enable Notes: No notes
$\overline{\text{DMC0_CS0}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Chip Select 0 Notes: No notes
DMC0_DQ00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 0 Notes: No notes
DMC0_DQ01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 1 Notes: No notes
DMC0_DQ02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 2 Notes: No notes
DMC0_DQ03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 3 Notes: No notes
DMC0_DQ04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 4 Notes: No notes
DMC0_DQ05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 5 Notes: No notes
DMC0_DQ06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 6 Notes: No notes
DMC0_DQ07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 7 Notes: No notes
DMC0_DQ08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 8 Notes: No notes
DMC0_DQ09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 9 Notes: No notes
DMC0_DQ10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 10 Notes: No notes
DMC0_DQ11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_DQ12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes
DMC0_DQ13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes
DMC0_DQ14	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes
DMC0_DQ15	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes
DMC0_LDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes
DMC0_LDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: For LPDDR a 100k pull-down is required.
$\overline{\text{DMC0_LDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: For single ended DDR2 connect to DMC0_VREF. For LPDDR leave unconnected.
DMC0_ODT	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: For LPDDR leave unconnected.
$\overline{\text{DMC0_RAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes
DMC0_UDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes
DMC0_UDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: For LPDDR a 100k pull-down is required.
$\overline{\text{DMC0_UDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: For single ended DDR2 connect to DMC0_VREF. For LPDDR leave unconnected.
DMC0_VREF	a	na	none	none	none	none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: No notes
$\overline{\text{DMC0_WE}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes
GND	g	na	none	none	none	none	none	na	Desc: Ground Notes: No notes
GND_HADC	g	na	none	none	none	none	none	na	Desc: Ground HADC Notes: If HADC is not used connect to ground.
HADC0_VIN0	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If HADC is not used connect to ground.
HADC0_VIN1	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If HADC is not used connect to ground.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
HADC0_VIN2	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If HADC is not used connect to ground.
HADC0_VIN3	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If HADC is not used connect to ground.
HADC0_VREFN	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: If HADC is not used connect to ground.
HADC0_VREFP	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: If HADC is not used connect to ground.
JTG_TCK_ SWCLK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Clock | Serial Wire Clock Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: Functional during reset.
JTG_TDO_SWO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out | Serial Wire Out Notes: Functional during reset, three-state when $\overline{\text{JTG_TRST}}$ is asserted.
JTG_TMS_ SWDIO	I/O	A	pu	none	none	none	none	VDD_EXT	Desc: JTAG Mode Select | Serial Wire DIO Notes: Functional during reset.
$\overline{\text{JTG_TRST}}$	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Reset Notes: Functional during reset, External pull-up is required.
PA_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Clock | TRACE0 Trace Data 7 | SMC0 Byte Enable 0 Notes: No notes
PA_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master In, Slave Out | TRACE0 Trace Data 6 | SMC0 Byte Enable 1 Notes: No notes
PA_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master Out, Slave In | TRACE0 Trace Data 5 | SMC0 Memory Select 1 Notes: No notes
PA_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 2 | SPI1 Ready | SMC0 Asynchronous Ready Notes: No notes
PA_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 1 | TM0 Timer 7 | SPI2 Ready | SMC0 Address 8 | SPI1 Slave Select Input Notes: No notes
PA_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 0 | SPI0 Slave Select Output 1 | SMC0 Address 7 | SPI0 Slave Select Input Notes: No notes
PA_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 1 | SPI0 Slave Select Output 2 | SPI0 Ready | SMC0 Address 6 Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 2 | SPT1 Channel B Transmit Data Valid | SPT1 Channel A Transmit Data Valid | SMC0 Address 5 | CNT0 Count Down and Gate Notes: No notes
PA_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 11 | MSI0 Card Detect | SPT1 Channel A Clock | SMC0 Address 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PA_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 10 | TM0 Timer 4 | SPT1 Channel A Frame Sync | SMC0 Address 2 Notes: No notes
PA_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 9 | TM0 Timer 5 | SPT1 Channel A Data 0 | SMC0 Address 3 Notes: No notes
PA_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 8 | TM0 Timer 6 | SPT1 Channel A Data 1 | SMC0 Address 4 Notes: No notes
PA_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 1 (HSYNC) | CAN1 Receive | SMC0 Output Enable | SYS Power Saving Mode Wakeup 4 | TM0 Alternate Capture Input 6 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PA_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 2 (VSYNC) | CAN1 Transmit | SMC0 Read Enable | CNT0 Count Zero Marker Notes: No notes
PA_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Clock | SPI1 Slave Select Output 4 | SMC0 Write Enable | TM0 Alternate Clock 5 Notes: No notes
PA_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 3 (FIELD) | SPT0 Channel A Transmit Data Valid | SPT0 Channel B Transmit Data Valid | SMC0 Memory Select 0 | CNT0 Count Up and Direction Notes: No notes
PB_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 7 | SPT1 Channel B Clock | SPI0 Clock | SMC0 Data 7 | TM0 Alternate Clock 35 Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 6 | SPT1 Channel B Frame Sync | SPI0 Master In, Slave Out | SMC0 Data 6 | TM0 Alternate Capture Input 1 Notes: No notes
PB_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 5 | SPT1 Channel B Data 0 | SPI0 Master Out, Slave In | SMC0 Data 5 Notes: No notes
PB_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 4 | SPT1 Channel B Data 1 | SPI0 Data 2 | SMC0 Data 4 Notes: No notes
PB_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 3 | SPT0 Channel B Clock | SPI0 Slave Select Output 4 | SMC0 Data 3 | TM0 Alternate Clock 6 Notes: No notes
PB_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 2 | SPT0 Channel B Data 0 | SPI0 Slave Select Output 5 | SMC0 Data 2 Notes: No notes
PB_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 1 | SPT0 Channel B Frame Sync | SPI0 Slave Select Output 6 | SMC0 Data 1 | TM0 Clock Notes: No notes
PB_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 0 | SPT0 Channel B Data 1 | SPI0 Data 3 | SMC0 Data 0 | SYS Power Saving Mode Wakeup 0 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Transmit | PPI0 Data 16 | SPI2 Slave Select Output 2 | SMC0 Data 8 | SYS Power Saving Mode Wakeup 1 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Receive | PPI0 Data 17 | SPI2 Slave Select Output 3 | SMC0 Data 9 | TM0 Alternate Capture Input 3 Notes: No notes
PB_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Clock | TRACE0 Trace Clock | SMC0 Data 10 | TM0 Alternate Clock 4 Notes: No notes
PB_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master In, Slave Out | TRACE0 Trace Data 4 | SMC0 Data 11 Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master Out, Slave In | TRACE0 Trace Data 3 | SMC0 Data 12 | SYS Power Saving Mode Wakeup 2 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 2 | UART1 Request to Send | TRACE0 Trace Data 2 | SMC0 Data 13 Notes: No notes
PB_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 3 | UART1 Clear to Send | TRACE0 Trace Data 1 | SMC0 Data 14 Notes: No notes
PB_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Slave Select Output 1 | TRACE0 Trace Data 0 | SMC0 Data 15 | SPI2 Slave Select Input Notes: No notes
PC_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Transmit | SPT0 Channel A Data 1 | PPI0 Data 15 Notes: No notes
PC_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Receive | SPT0 Channel B Data 1 | PPI0 Data 14 | SMC0 Address 9 | TM0 Alternate Capture Input 4 Notes: No notes
PC_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Request to Send | CAN0 Receive | PPI0 Data 13 | SMC0 Address 10 | SYS Power Saving Mode Wakeup 3 | TM0 Alternate Capture Input 5 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PC_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Clear to Send | CAN0 Transmit | PPI0 Data 12 | SMC0 Address 11 | TM0 Alternate Capture Input 0 Notes: No notes
PC_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Clock | SPI0 Clock | MSI0 Data 1 | SMC0 Address 12 | TM0 Alternate Clock 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Frame Sync | TM0 Timer 3 | MSI0 Command Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Data 0 | SPI0 Master In, Slave Out | MSI0 Data 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Frame Sync | SPI0 Master Out, Slave In | MSI0 Data 2 | TM0 Alternate Capture Input 2 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Data 0 | SPI0 Data 2 | MSI0 Data 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Clock | SPI0 Data 3 | MSI0 Clock | TM0 Alternate Clock 2 Notes: No notes
PC_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Clock | MSI0 Data 4 | SPI1 Slave Select Output 3 | TM0 Alternate Clock 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Frame Sync | MSI0 Data 5 | SPI0 Slave Select Output 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 0 | MSI0 Data 6 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 1 | MSI0 Data 7 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Transmit Data Valid | MSI0 eSDIO Interrupt Input Notes: No notes

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
RTC0_CLKIN	a	na	none	none	none	none	none	VDD_RTC	Desc: RTC0 Crystal input / external oscillator connection Notes: If RTC is not used connect to ground.
RTC0_XTAL	a	na	none	none	none	none	none	VDD_RTC	Desc: RTC0 Crystal output Notes: No notes
SYS_BMODE0	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 0 Notes: A pull-down is required for setting to 0 and a pull-up is required for setting to 1.
SYS_BMODE1	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 1 Notes: A pull-down is required for setting to 0 and a pull-up is required for setting to 1.
SYS_CLKIN	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Clock/Crystal Input Notes: No notes
SYS_CLKOUT	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Processor Clock Output Notes: During reset, SYS_CLKOUT drives out SYS_CLKIN Frequency.
SYS_EXTWAKE	I/O	A	none	none	H	none	L	VDD_EXT	Desc: SYS External Wake Control Notes: Drives low during hibernate and high all other times.
$\overline{\text{SYS_FAULT}}$	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SYS Complementary Fault Output Notes: Open drain, requires an external pull-up resistor.
$\overline{\text{SYS_HWRST}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Processor Hardware Reset Control Notes: Active during reset
$\overline{\text{SYS_NMI}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Non-maskable Interrupt Notes: Requires an external pull-up resistor.
$\overline{\text{SYS_RESOUT}}$	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Reset Output Notes: Active during reset
SYS_XTAL	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Crystal Output Notes: Leave unconnected if an oscillator is used to provide SYS_CLKIN. Active during reset. State during hibernate is controlled by DPM_HIB_DIS
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used connect to ground.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input Notes: If USB is not used connect to ground. Active during reset
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data - Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used see the USB chapter in the HRM.
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used see the USB chapter in the HRM.
USB0_ID	I/O	na	none	none	none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: If USB is not used connect to ground. When USB is being used the internal pull-up that is present during hibernate is programmable. See the USB chapter in the HRM. Active during reset.
USB0_VBC	I/O	E	none	none	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: If USB is not used pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: If USB is not used connect to ground.
USB0_XTAL	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Crystal Notes: No notes
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC Notes: If the DMC is not used connect to VDD_INT
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD Notes: Must be powered
VDD_HADC	s	na	none	none	none	none	none	na	Desc: VDD for HADC Notes: If HADC is not used connect to ground.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD Notes: Must be powered.
VDD_OTP	s	na	none	none	none	none	none	na	Desc: VDD for OTP Notes: Must be powered.
VDD_RTC	s	na	none	none	none	none	none	na	Desc: VDD for RTC Notes: If RTC is not used connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB Notes: If USB is not used connect to VDD_EXT.

SPECIFICATIONS

For information about product specifications please contact your ADI representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}[1]	Internal Supply Voltage	CCLK ≤ 400 MHz	TBD	TBD	TBD	V
V_{DD_EXT}[2]	External Supply Voltage		1.7	1.8	1.9	V
V_{DD_EXT}[2]	External Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[3]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DD_RTC}	Real-Time Clock Supply Voltage		2.0	3.3	3.47	V
V_{DD_HADC}	Housekeeping ADC Supply Voltage		3.13	3.3	3.47	V
V_{DD_OTP}[2]	OTP Supply Voltage					
	For Reads		2.25	3.3	3.47	V
	For Writes		3.13	3.3	3.47	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 1.9 V	0.7 × V_{DD_EXT}			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = Maximum	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[7, 8]		V_{DD_DMC} = 1.9 V	V_{DDR_REF} + 0.25			V
V_{IH_LPDDR}[9]		V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
V_{ID_DDR2}[10]	Differential Input Voltage	V_{IX} = TBD V	TBD			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 1.7 V			0.3 × V_{DD_EXT}	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = Minimum			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7, 8]		V_{DD_DMC} = 1.7 V			V_{DDR_REF} – 0.25	V
V_{IL_LPDDR}[9]		V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] The expected nominal value is 1.1 V ±5%, and initial customer designs should design with a programmable regulator that can be adjusted from 0.95 V to 1.25 V in 50 mV steps.
[2] Must remain powered (even if the associated function is not used).
[3] If not used, connect to 1.8 V or 3.3 V.
[4] Parameter value applies to all input and bidirectional signals except TWI signals, DMC0 signals and USB0 signals.
[5] Parameter applies to TWI signals.
[6] TWI signals are pulled up to V_{BUSTWI}. See Table 16.
[7] Parameter applies to DMC0 signals in DDR2 mode.
[8] V_{DDR_REF} is the voltage applied to pin V_{REF_DMC}, nominally V_{DD_DMC}/2.
[9] Parameter applies to DMC0 signals in LPDDR mode.
[10] Parameter applies to signals DMC0_CK, $\overline{\text{DMC0_CK}}$, DMC0_LDQS, $\overline{\text{DMC0_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0_UDQS}}$ when used in DDR2 differential input mode.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nom	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$			400	MHz
f_{SYSCLK}	SYSCLK Frequency				200	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$	30		100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2/LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$			200	MHz
f_{OCLK}	Output Clock Frequency				50	MHz
$f_{SYS_CLKOUTJ}$	SYS_CLKOUT Period Jitter[2, 3]			TBD		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				50	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				50	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[4, 5]	$f_{PCLKEXT} \leq f_{SCLK0}$			50	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[4, 5]	$f_{PCLKEXT} \leq f_{SCLK0}$			50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[4, 5]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[4, 5]	$f_{SPTCLKEXT} \leq f_{SCLK0}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[4, 5]	$f_{SPICLKEXT} \leq f_{SCLK0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[4, 5]	$f_{SPICLKEXT} \leq f_{SCLK0}$			50	MHz

[1] The minimum frequency for SCLK0 applies only when the USB is used.
[2] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this typical specification for each end application.
[3] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[4] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the AC timing specifications section for that peripheral. Pay particular attention to setup and hold times for VDD_EXT = 1.8V which may preclude the maximum frequency listed here.
[5] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} that clocks the peripheral.

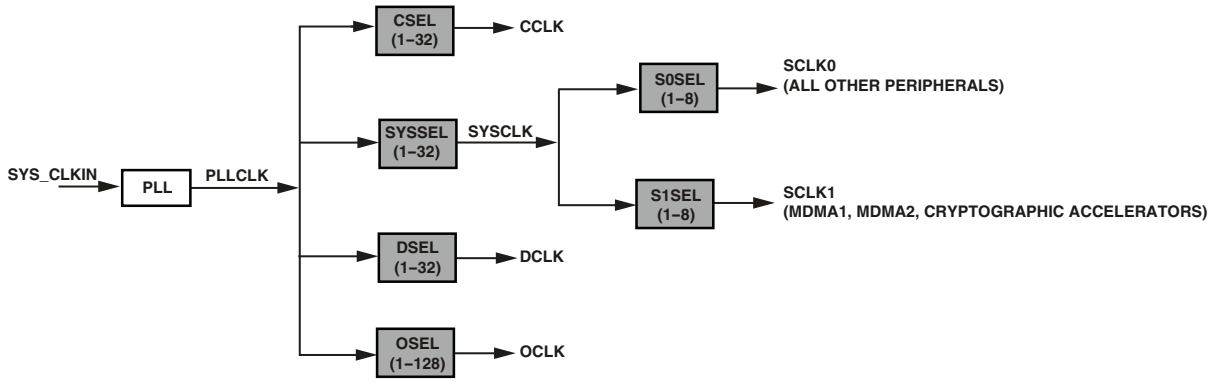


Figure 6. Clock Relationships and Divider Values

Table 18. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	200	800	MHz

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OH} = –1.5 mA	0.9 × V_{DD_EXT}			V
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OH} = –2.0 mA	0.9 × V_{DD_EXT}			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 34 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 40 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 50 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 60 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA	V_{DD_DMC} – 0.320			V
V_{OH_LPDDR}[2]	High Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA	V_{DD_DMC} – 0.320			V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OL} = 1.5 mA			0.200	V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OL} = 2.0 mA			0.200	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 34 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 40 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 50 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 60 ohms	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA			0.320	V
V_{OL_LPDDR}[2]	Low Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OH} = TBD mA			0.320	V
I_{IH}[4]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{IH_PD}[5]	High Level Input Current with Pull-down Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			TBD	µA
I_{IL}[6]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{IL_PU}[7]	Low Level Input Current with Pull-up Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			TBD	µA
I_{IH_USB0}[8]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			TBD	µA
I_{IL_USB0}[8]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			TBD	µA
I_{OZH}[9]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{OZH}[10]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 1.9 V			10	µA
I_{OZL}[11]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{OZL_PU}[12]	Three-State Leakage Current with Pull-up Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			TBD	µA
I_{OZH_TWI}[13]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 5.5 V			10	µA
C_{IN}[14, 15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		TBD	TBD	pF
C_{IN_TWI}[13, 15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		TBD	TBD	pF
C_{IN_DDR}[15, 16]	Input Capacitance	$T_{AMBIENT}$ = 25°C		TBD	TBD	pF
$I_{DD_DEEPSLEEP}$[17, 18]	V_{DD_INT} Current in Deep Sleep Mode	Clocks Disabled T_J = 25°C		1.4		mA
I_{DD_IDLE}[18]	V_{DD_INT} Current in Idle	TBD		TBD		mA

Parameter		Test Conditions	Min	Typical	Max	Unit
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 400 MHz f_{CCLK} = 400 MHz ASF = 1.0 (Full-on Typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = DISABLED Peripherals Disabled T_J = 25°C		86		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 300 MHz ASF = 1.0 (Full-on Typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = DISABLED Peripherals Disabled T_J = 25°C		67		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 200 MHz f_{CCLK} = 200 MHz ASF = 1.0 (Full-on Typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = DISABLED Peripherals Disabled T_J = 25°C		48		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 100 MHz f_{CCLK} = 100 MHz ASF = 1.0 (Full-on Typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = DISABLED Peripherals Disabled T_J = 25°C		29		mA
$I_{DD_HIBERNATE}$[17, 19]	Hibernate State Current	TBD	TBD	TBD		µA
$I_{DD_HIBERNATE}$[17, 19]	Hibernate State Current Without USB	TBD		TBD		µA
I_{DD_INT}[18]	V_{DD_INT} Current	TBD			See I_{DDINT_TOT} equation on page TBD	mA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals and USB0 signals.
[2] Applies to signals DMC0_A[00:13], DMC0_CAS, DMC0_CKE, DMC0_CK, DMC0_CK, DMC0_CS, DMC0_DQ[00:15], DMC0_LDM, DMC0_LDQS, DMC0_LDQS, DMC0_ODT, DMC0_RAS, DMC0_UDM, DMC0_UDQS, DMC0_UDQS, and DMC0_WE.
[3] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.
[4] Applies to signals SMC0_ARDY, SMC0_BR, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TDI, and JTG_TMS_SWDIO.
[5] Applies to signals JTG_TCK_SWCLK and JTG_TRST.
[6] Applies to signals SMC0_ARDY, SMC0_BR, SYS_BMODE0–2, SYS_CLKIN, SYS_HWRST, SYS_PWRGD, JTG_TCK, and JTG_TRST.
[7] Applies to signals JTG_TDI and JTG_TMS_SWDIO.
[8] Applies to signal USB0_CLKIN.
[9] Applies to signals PA0–15, PB0–15, PC0–14, SMC0_AMS0, SMC0_ARE, SMC0_AWE, SMC0_A0E, SMC0_A01–02, SMC0_D00–15, SYS_FAULT, JTG_EMU, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS.
[10] Applies to DMC0_A[00:13], DMC0_BA[0:2], DMC0_CAS, DMC0_CS0, DMC0_DQ[00:15], DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, and DMC0_WE.
[11] Applies to signals PA0–15, PB0–15, PC0–14, SMC0_A0E, SMC0_A01–12, SMC0_D00–15, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_A00–13, DMC0_BA0–2, DMC0_CAS, DMC0_CS0, DMC0_DQ00–15, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, DMC0_WE, and TWI signals.
[12] Applies to TBD signals.
[13] Applies to all TWI signals.

[14]Applies to all signals, except DMC0 and TWI signals.
[15]Guaranteed, but not tested.
[16]Applies to all DMC0 signals.
[17]See the *ADSP-BF70x Blackfin+ Processor Hardware Reference Manual* for definition of deep sleep and hibernate operating modes.
[18]Additional information can be found at Total Internal Power Dissipation.
[19]Applies to V_{DD_EXT}, V_{DD_DMC}, and V_{DD_USB} supply signals only. Clock inputs are tied high or low.

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current (deep sleep)
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DDINT} = I_{DDINT_DEEPSLEEP} + I_{DDINT_PLL_DYN} + I_{DDINT_CCLK_DYN} + I_{DDINT_SYSCLK_DYN} + I_{DDINT_SCLK0_DYN} + I_{DDINT_SCLK1_DYN} + I_{DDINT_DCLK_DYN} + I_{DDINT_USBCLK_DYN} + I_{DDINT_DMA_DR_DYN}$$

For details on using this equation, use the Advanced Search in EngineerZone, searching on the string **power consumption** and restricting the search to the **ADSP-BF70x** Group or Space.

HADC

HADC Electrical Characteristics

Parameter	Test Conditions	Typ	Unit
$I_{DD_HADC_IDLE}$	Current Consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD_HADC_ACTIVE}$	Current Consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD_HADC_POWERDOWN}$	Current Consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down	10	µA

HADC DC Accuracy

Parameter	Typ	Unit
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB[1]
Differential Nonlinearity (DNL)	±2	LSB[1]
Offset Error	±8	LSB[1]
Offset Error Matching	±10	LSB[1]
Gain Error	±4	LSB[1]
Gain Error Matching	±4	LSB[1]

[1] LSB = HADC0_VREFP ÷ 4096

HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

PACKAGE INFORMATION

The information presented in Figure 7 and Table 19 provides details about package branding. For a complete listing of product availability, see the Ordering Guide.

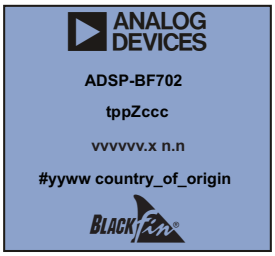


Figure 7. Product Information on Package

Table 19. Package Brand Information

Brand Key	Field Description
ADSP-BF702	Product Model
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 20. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to 1.20 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to 3.60 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to 1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to 3.60 V
Real-Time Clock Supply Voltage (V_{DD_RTC})	–0.33 V to 3.60 V
Housekeeping ADC Supply Voltage (V_{DD_HADC})	–0.33 V to 3.60 V
One-Time Programmable Memory Supply Voltage (V_{DD_OTP})	–0.33 V to 3.60 V
Input Voltage[1, 2, 3]	–0.33 V to 3.60 V
TWI Input Voltage[2, 4]	–0.33 V to 5.50 V

Table 20. Absolute Maximum Ratings (Continued)

Parameter	Rating
USB0_Dx Input Voltage[5]	–0.33 V to 5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to TBD V
DDR2 Input Voltage[6]	–0.33 V to 1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	TBD mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] For other duty cycles see Table 21.
[4] Applies to balls TWI_SCL and TWI_SDA.
[5] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 37.
[6] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

Table 21. Maximum Duty Cycle for Input Transient Voltage[1, 2]

Maximum Duty Cycle (%)[2]	V_{IN} Min (V)[3]	V_{IN} Max (V)[3]
100	TBD	TBD
50	TBD	TBD
40	TBD	TBD
25	TBD	TBD
20	TBD	TBD
15	TBD	TBD
10	TBD	TBD

[1] Applies to all signal balls with the exception of SYS_CLKIN, SYS_XTAL, SYS_EXT_WAKE, USB0_DP, USB0_DM, USB0_VBUS, TWI signals, and DMC0 signals.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the specified voltages, and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 22 and Figure 8 describe clock and reset operations. Per the CCLK, SYSCLK, SCLK0, SCLK1, DCLK, and OCLK timing specifications in Table 17 on Page 48, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the processor's maximum instruction rate.

Table 22. Clock and Reset Timing

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{CKIN}	SYS_CLKIN Frequency (CGU_CTL.DF = 0)[1, 2, 3]	20	50	MHz
f_{CKIN}	SYS_CLKIN Frequency (CGU_CTL.DF = 1)[1, 2, 3]	40	50	MHz
t_{CKINL}	SYS_CLKIN Low Pulse[1]	10		ns
t_{CKINH}	SYS_CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{SYS_HWRST}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] The t_{CKIN} period (see Figure 8) equals $1/f_{CKIN}$.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{PLLCLK} setting discussed in Table 18.
[4] Applies after power-up sequence is complete. See Table 23 and Figure 9 for power-up reset timing.

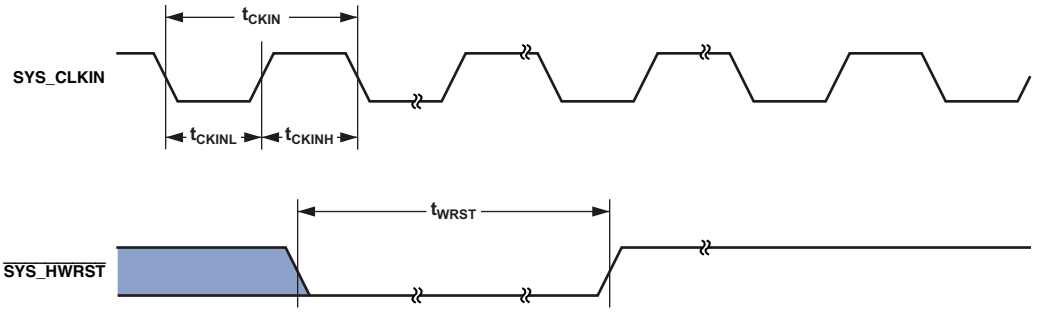


Figure 8. Clock and Reset Timing

Power-Up Reset Timing

In Figure 9, $V_{DD_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, and V_{DD_HADC}.

Table 23. Power-Up Reset Timing

All specifications are based on simulation data and are subject to change without notice.			
Parameter	**Min**	**Max**	**Unit**
Timing Requirement			
$t_{RST_IN_PWR}$ $\overline{\text{SYS_HWRST}}$ Deasserted after V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, V_{DD_HADC}, and SYS_CLKIN are Stable and Within Specification	$11 \times t_{CKIN}$		ns

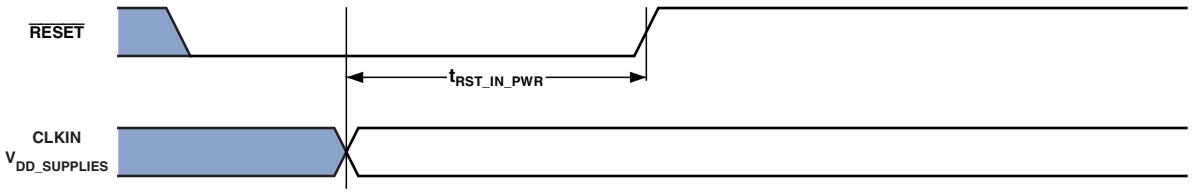


Figure 9. Power-Up Reset Timing

Asynchronous Read

Table 24. Asynchronous Memory Read (BxMODE = b#00)

All specifications are based on simulation data and are subject to change without notice.						
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
$t_{SDATARE}$	DATA in Setup Before $\overline{SMC0_ARE}$ High	11.8		10.8		ns
$t_{HDATARE}$	DATA in Hold After $\overline{SMC0_ARE}$ High	0		0		ns
$t_{DARDYARE}$	SMC0_ARDY Valid After $\overline{SMC0_ARE}$ Low[1, 2]		(RAT – 2.5) × t_{SCLK0} – 17.5		(RAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics						
t_{AMSARE}	SMC0_Ax/$\overline{SMC0_AMSx}$ Assertion Before $\overline{SMC0_ARE}$ Low[3]	(PREST + RST + PREAT) × t_{SCLK0} – 2		(PREST + RST + PREAT) × t_{SCLK0} – 2		ns
$t_{DADVARE}$	SMC0_ARE Low Delay From ADV High	PREAT × t_{SCLK0} – 2		PREAT × t_{SCLK0} – 2		
t_{AOEARE}	$\overline{SMC0_AOE}$ Assertion Before $\overline{SMC0_ARE}$ Low	(RST + PREAT) × t_{SCLK0} – 2		(RST + PREAT) × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{SMC0_ARE}$ High[5]	RHT × t_{SCLK0} –2		RHT × t_{SCLK0} –2		ns
t_{WARE}	$\overline{SMC0_ARE}$ Active Low Width[6]	RAT × t_{SCLK0} – 2		RAT × t_{SCLK0} – 2		ns
$t_{DAREARDY}$	$\overline{SMC0_ARE}$ High Delay After SMC0_ARDY Assertion[1]	TBD	TBD	TBD	TBD	ns

[1] SMC0_BxCTL.ARDYEN bit = 1.
[2] RAT value set using the SMC_BxTIM.RAT bits.
[3] PREST, RST, and PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, and the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{SMC0_AMS}$, $\overline{SMC0_AOE}$, $\overline{SMC0_ABEx}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.

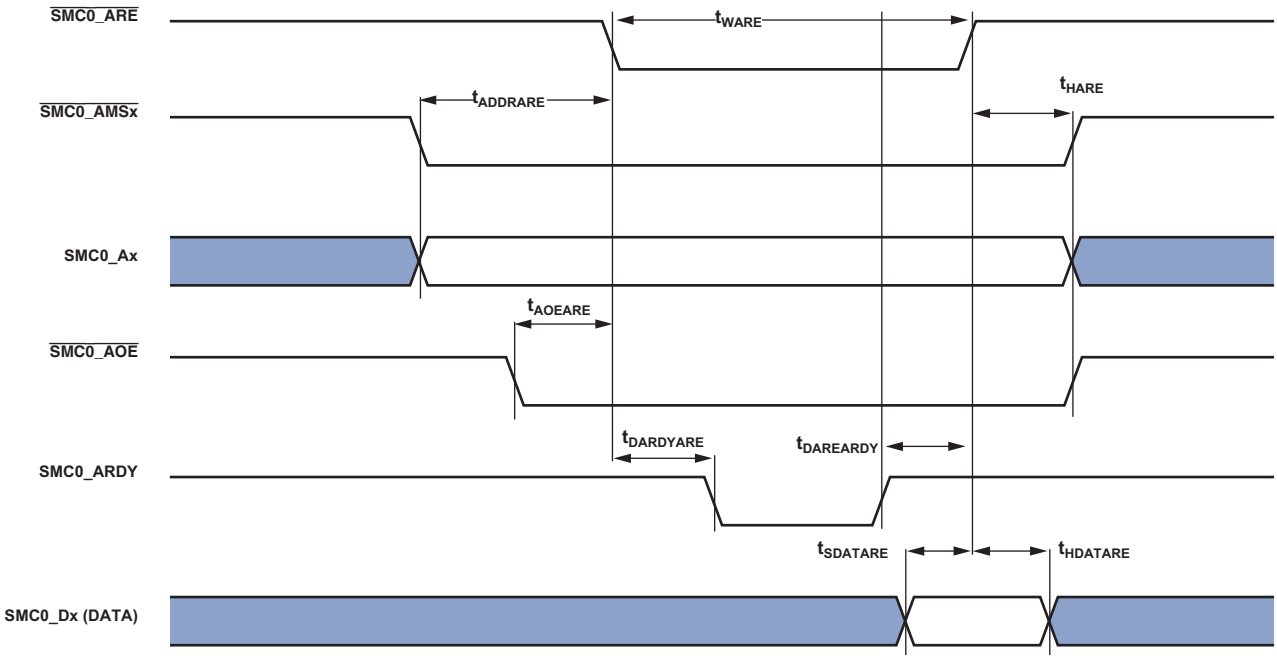


Figure 10. Asynchronous Read

Asynchronous Flash Read

Table 25. Asynchronous Flash Read

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0_AMSx}}$ Assertion Before SMC0_NORDV Low[1]	PREST × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
$t_{DADVARE}$	$\overline{\text{SMC0_ARE}}$ Low Delay From SMC0_NORDV High[3]	PREAT × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0_ARE}}$ High[5]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0_ARE}}$ Active Low Width[7]	RAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0_AMS}}$, $\overline{\text{SMC0_AOE}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

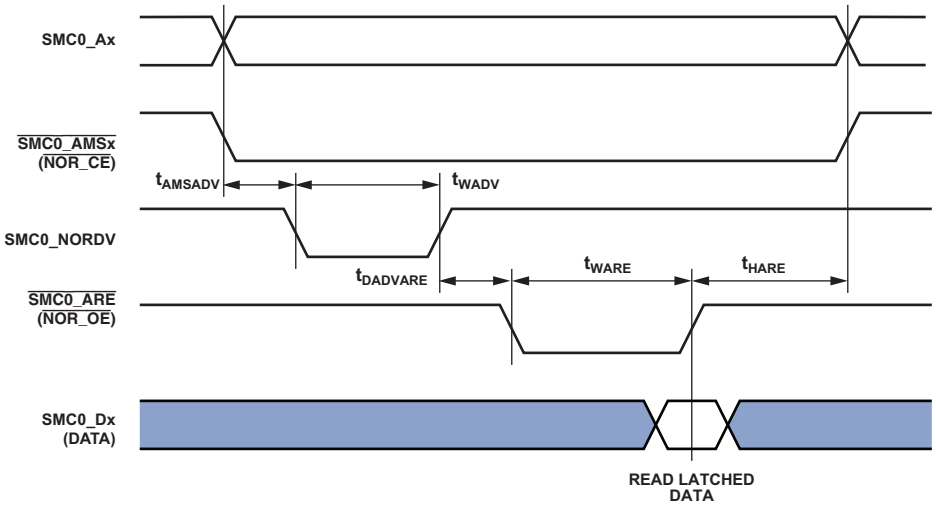


Figure 11. Asynchronous Flash Read

Asynchronous Page Mode Read

Table 26. Asynchronous Page Mode Read

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V /3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AV}	SMC0_Ax (Address) Valid for First Address Min Width[1]	(PREST + RST + PREAT + RAT) × t_{SCLK0} – 2		ns
t_{AV1}	SMC0_Ax (Address) Valid for Subsequent SMC0_Ax (Address) Min Width	PGWS × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
t_{HARE}	Output[3] Hold After $\overline{\text{SMC0_ARE}}$ High[4]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[5]	$\overline{\text{SMC0_ARE}}$ Active Low Width[6]	(RAT + (Nw – 1) × PGWS) × t_{SCLK0} – 2		ns

[1] PREST, RST, PREAT and RAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] Output signals are SMC0_Ax, $\overline{\text{SMC0_AMSx}}$, $\overline{\text{SMC0_AOE}}$.
[4] RHT value set using the SMC_BxTIM.RHT bits.
[5] SMC_BxCTL.ARDYEN bit = 0.
[6] RAT value set using the SMC_BxTIM.RAT bits.

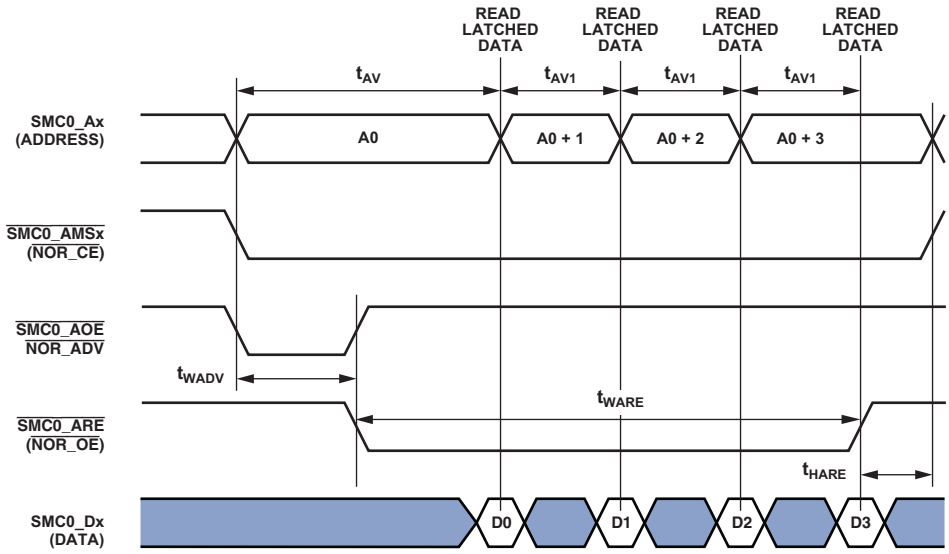


Figure 12. Asynchronous Page Mode Read

Asynchronous Write

Table 27. Asynchronous Memory Write (BxMODE = b#00)

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirement						
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{\text{SMC0_AWE}}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics						
t_{ENDAT}	DATA Enable After $\overline{\text{SMC0_AMSx}}$ Assertion	–3		–3		ns
t_{DDAT}	DATA Disable After $\overline{\text{SMC0_AMSx}}$ Deassertion		4.5		4	ns
t_{AMSAWE}	SMC0_Ax/$\overline{\text{SMC0_AMSx}}$ Assertion Before $\overline{\text{SMC0_AWE}}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		(PREST + WST + PREAT) × t_{SCLK0} – 2		ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0_AWE}}$ High[5]	WHT × t_{SCLK0}		WHT × t_{SCLK0} – 2		ns
t_{WAWE}[6]	$\overline{\text{SMC0_AWE}}$ Active Low Width[6]	WAT × t_{SCLK0} – 2		WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{\text{SMC0_AWE}}$ High Delay After SMC0_ARDY Assertion		3.5 × t_{SCLK0} + 17.5		3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0_AMSx}}$, $\overline{\text{SMC0_ABEx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

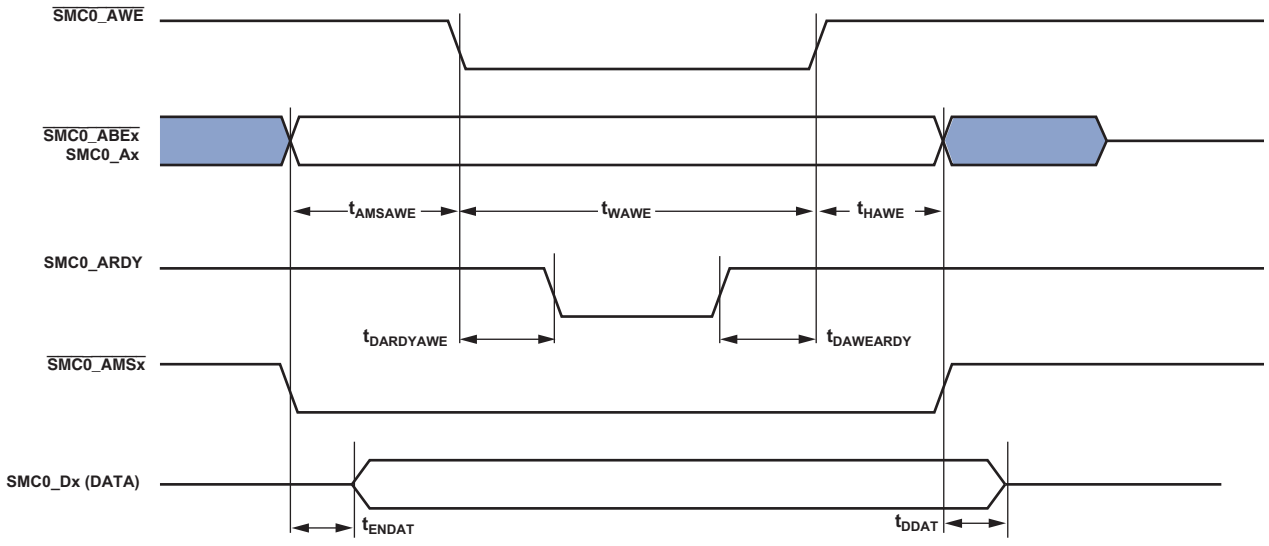


Figure 13. Asynchronous Write

Asynchronous Flash Write

Table 28. Asynchronous Flash Write

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{AMSADV}	SMC0_Ax/$\overline{\text{SMC0_AMSx}}$ Assertion Before ADV Low[1]	PREST × t_{SCLK0} – 2		ns
$t_{DADVAWE}$	$\overline{\text{SMC0_AWE}}$ Low Delay From ADV High[2]	PREAT × t_{SCLK0} – 2		ns
t_{WADV}	NR_ADV Active Low Width[3]	WST × t_{SCLK0} – 2		ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0_AWE}}$ High[5]	WHT × t_{SCLK0} – 2		ns
t_{WAWE}[6]	$\overline{\text{SMC0_AWE}}$ Active Low Width[7]	WAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] PREAT value set using the SMC_BxETIM.PREAT bits.
[3] WST value set using the SMC_BxTIM.WST bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0_AMSx}}$, $\overline{\text{SMC0_ABEx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.
[7] WAT value set using the SMC_BxTIM.WAT bits.

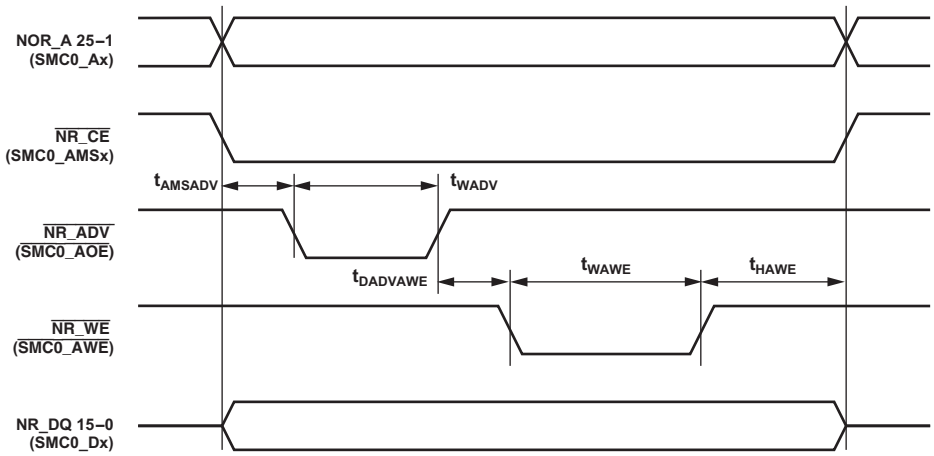


Figure 14. Asynchronous Flash Write

All Accesses

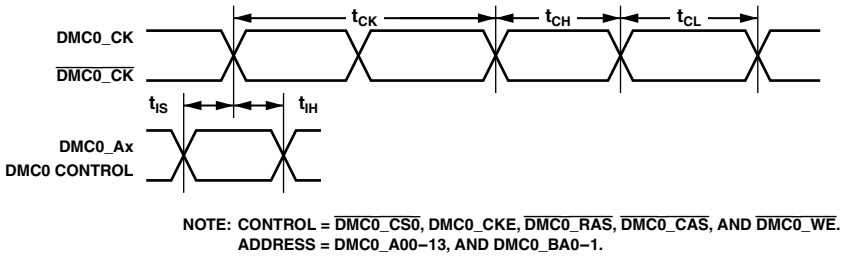
Table 29. All Accesses

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristic						
t_{TURN}	$\overline{\text{SMC0_AMSx}}$ Inactive Width	(IT + TT) × t_{SCLK0} – 2		(IT + TT) × t_{SCLK0} – 2		ns

DDR2 SDRAM Clock and Control Cycle Timing

Table 30. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	350		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	475		ps



NOTE: CONTROL = DMC0_CS0, DMC0_CKE, DMC0_RAS, DMC0_CAS, AND DMC0_WE.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–1.

Figure 15. DDR2 SDRAM Clock and Control Cycle Timing

DDR2 SDRAM Read Cycle Timing

Table 31. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz[1]		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_ DQ Signals		0.35	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.8		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] In order to ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.

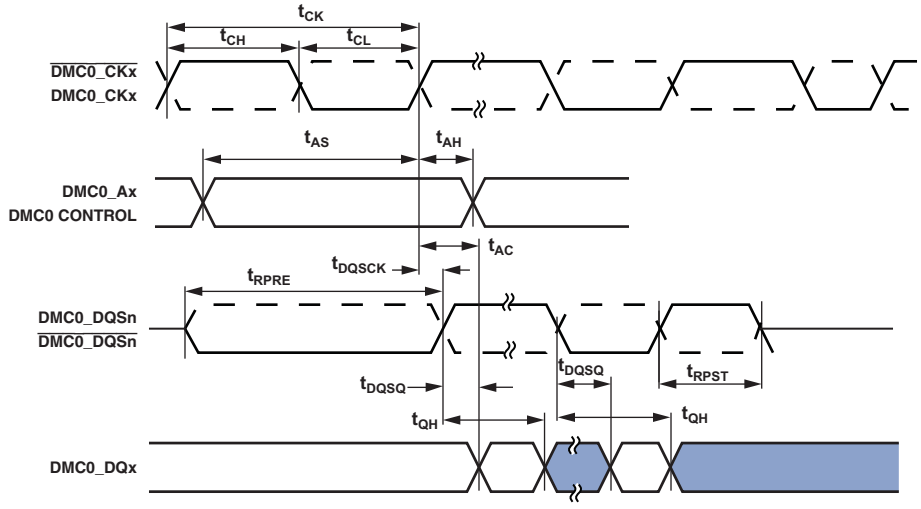


Figure 16. DDR2 SDRAM Controller Input AC Timing

DDR2 SDRAM Write Cycle Timing

Table 32. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz[1]		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	–0.25	0.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.15		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.275		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] In order to ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

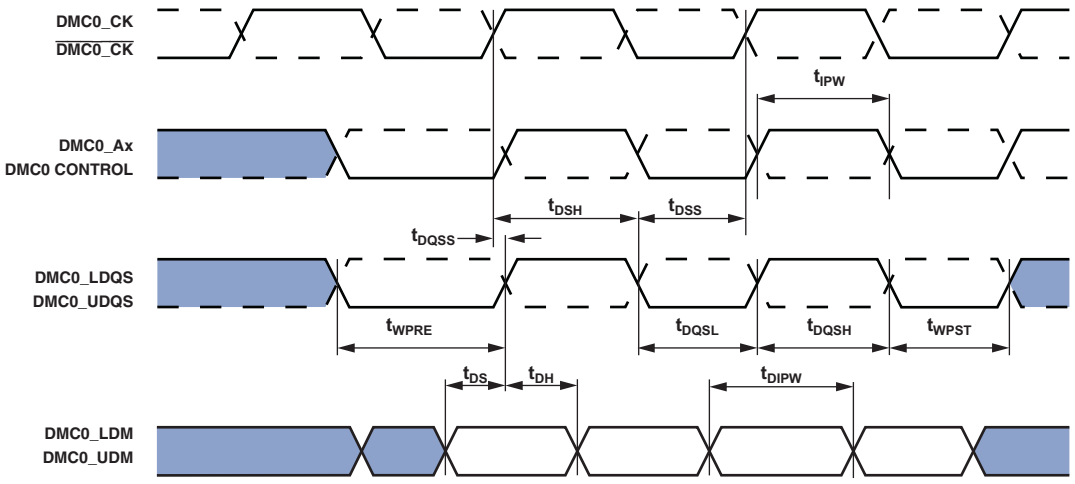
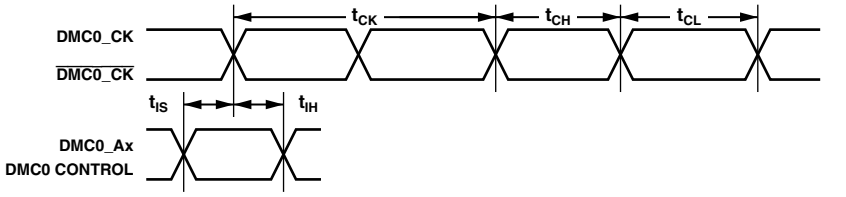


Figure 17. DDR2 SDRAM Controller Output AC Timing

Mobile DDR SDRAM Clock and Control Cycle Timing

Table 33. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	0.9		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	0.9		ns



NOTE: CONTROL = DMC0_CS0, DMC0_CKE, DMC0_RAS, DMC0_CAS, AND DMC0_WE.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–1.

Figure 18. Mobile DDR SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Read Cycle Timing

Table 34. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.75		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.4	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

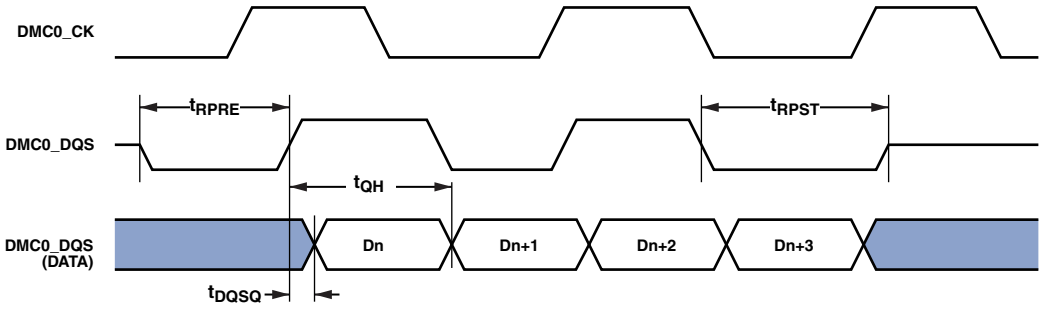


Figure 19. Mobile DDR SDRAM Controller Input AC Timing

Mobile DDR SDRAM Write Cycle Timing

Table 35. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

All specifications are based on simulation data and are subject to change without notice.				
		200 MHz		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DQSS}[1]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	1.8		ns

[1] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

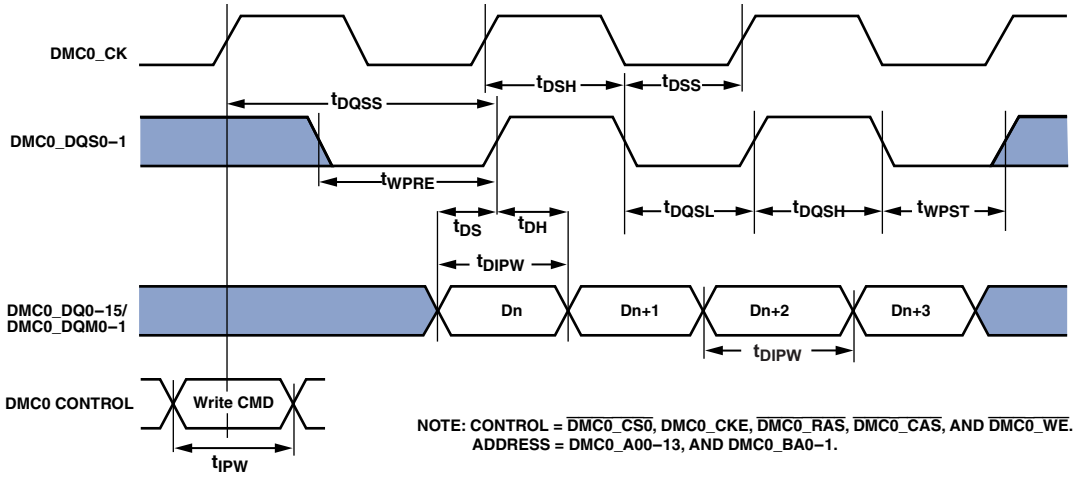


Figure 20. Mobile DDR SDRAM Controller Output AC Timing

General-Purpose Port Timing

Table 36 and Figure 21 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

All specifications are based on simulation data and are subject to change without notice.			
	V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter	Min	Max	Unit
Timing Requirement			
t_{WFI} General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

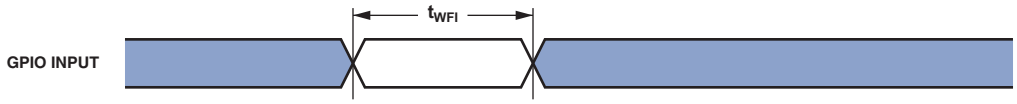


Figure 21. General-Purpose Port Timing

Timer Cycle Timing

Table 37 and Figure 22 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an ideal maximum input frequency of (f_{SCLK0}/4) MHz. The Period Value (VALUE) is the timer period assigned in the TMx_TMRn_PER register and can range from 2 to $2^{32} - 1$.

Table 37. Timer Cycle Timing

All specifications are based on simulation data and are subject to change without notice.					
	V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter	Min	Max	Min	Max	Unit
Timing Requirements					
t_{WL} Timer Pulse Width Input Low[1]	$2 \times t_{SCLK0} - 1.5$		$2 \times t_{SCLK0} - 1.5$		ns
t_{WH} Timer Pulse Width Input High[1]	$2 \times t_{SCLK0} - 1.5$		$2 \times t_{SCLK0} - 1.5$		ns
Switching Characteristic					
t_{HTO} Timer Pulse Width Output	$t_{SCLK0} \times VALUE - 1.5$		$t_{SCLK0} \times VALUE - 1.5$		ns

[1] This specification indicates the minimum instantaneous width that can be tolerated due to duty cycle variation or jitter for TMx signals in width capture and external clock modes. The ideal maximum frequency for TMx signals is listed in Timer Cycle Timing on this page.

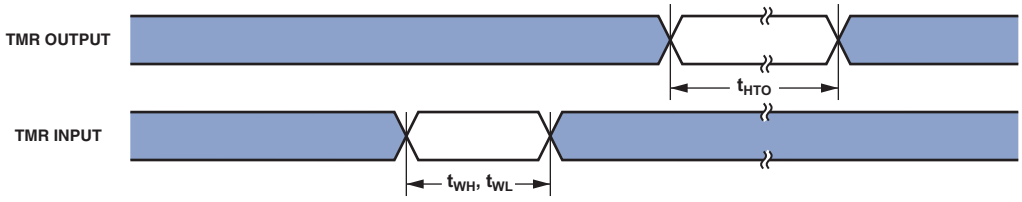


Figure 22. Timer Cycle Timing

Up/Down Counter/Rotary Encoder Timing

Table 38. Up/Down Counter/Rotary Encoder Timing

All specifications are based on simulation data and are subject to change without notice.					
	V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirement					
t_{WCOUNT} Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

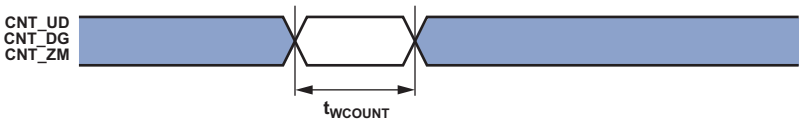


Figure 23. Up/Down Counter/Rotary Encoder Timing

JTAG Test And Emulation Port Timing

Table 39 and Figure 24 describe JTAG port operations.

Table 39. JTAG Port Timing

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	5		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	4		4		ns
t_{TRSTW}	$\overline{\text{JTG_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		4		T_{CK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		16.5		14.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		18		16.5	ns
t_{DTMS}	TMS Delay After TCK high in SWD Mode	3.5	16.5	3.5	14.5	ns

[1] System Inputs = DMC0_DQ00–15, DMC0_LDQS, $\overline{\text{DMC0_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0_UDQS}}$, PA_15–0, PB_15–0, PC_14–0, SYS_BMODE0–1, $\overline{\text{SYS_HWRST}}$, $\overline{\text{SYS_FAULT}}$, $\overline{\text{SYS_NMI}}$, TWI0_SCL, TWI0_SDA, SYS_EXTWAKE.

[2] 50 MHz Maximum.

[3] System Outputs = DMC0_A00–13, DMC0_BA0–2, $\overline{\text{DMC0_CAS}}$, DMC0_CK, $\overline{\text{DMC0_CK}}$, DMC0_CKE, $\overline{\text{DMC0_CS0}}$, DMC0_DQ00–15, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0_UDQS}}$, $\overline{\text{DMC0_WE}}$, PA_15–0, PB_15–0, PC_14–0, SYS_CLKOUT, $\overline{\text{SYS_FAULT}}$, $\overline{\text{SYS_RESOUT}}$, $\overline{\text{SYS_NMI}}$.

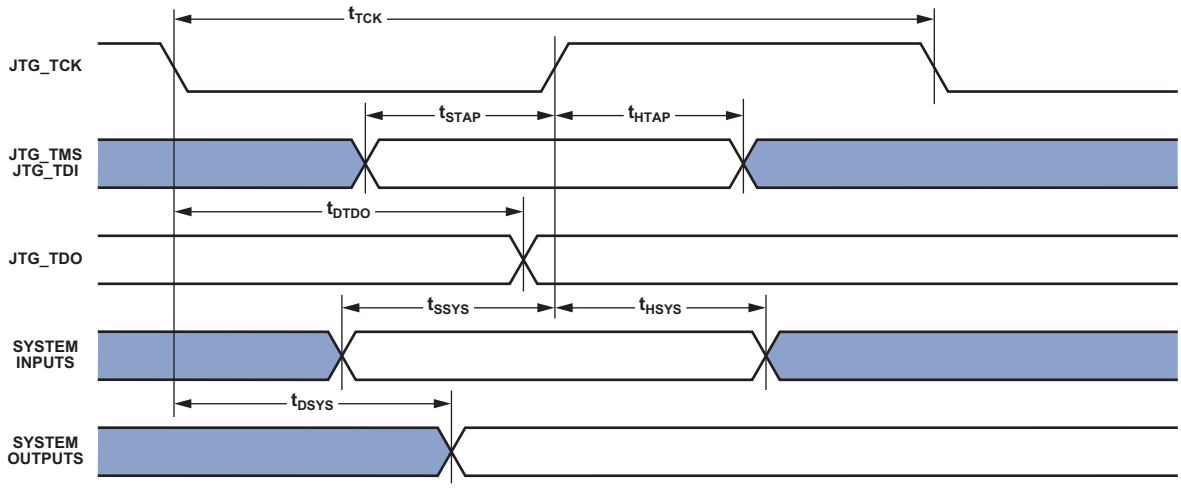


Figure 24. JTAG Port Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SPT_CLK) width. In Figure 25 either the rising edge or the falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK0}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 40. Serial Ports—External Clock

All specifications are based on simulation data and are subject to change without notice.

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	1.5		1		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	3		3		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	1.5		1		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	3		3		ns
t_{SCLKW}	SPT_CLK Width[2]	$(0.5 \times t_{SPTCLKEXT}) - 1$		$(0.5 \times t_{SPTCLKEXT}) - 1$		ns
t_{SPTCLK}	SPT_CLK Period[2]	$t_{SPTCLKEXT} - 1$		$t_{SPTCLKEXT} - 1$		ns
Switching Characteristics						
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]		17.5		14.5	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]	2.5		2.5		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		17.5		14.5	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	2.5		2.5		ns

[1] Referenced to sample edge.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK. For the external SPT_CLK ideal maximum frequency see the $f_{SPTCLKEXT}$ specification in Table 17 on Page 48 in Clock Related Operating Conditions.

[3] Referenced to drive edge.

Table 41. Serial Ports—Internal Clock

All specifications are based on simulation data and are subject to change without notice.

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSI}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	16.5		14		ns
t_{HFSI}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	–0.5		–0.5		ns
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	6.5		5		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	1.5		1		ns
Switching Characteristics						
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		2		2	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–4.5		–3.5		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		2		2	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–4.5		–3.5		ns
t_{SCLKIW}	SPT_CLK Width[3]	$0.5 \times t_{SPTCLKPROG} - 1.5$		$0.5 \times t_{SPTCLKPROG} - 1.5$		ns
t_{SPTCLK}	SPT_CLK Period[3]	$t_{SPTCLKPROG} - 1.5$		$t_{SPTCLKPROG} - 1.5$		ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] See Table 17 on Page 48 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SPTCLKPROG}$.

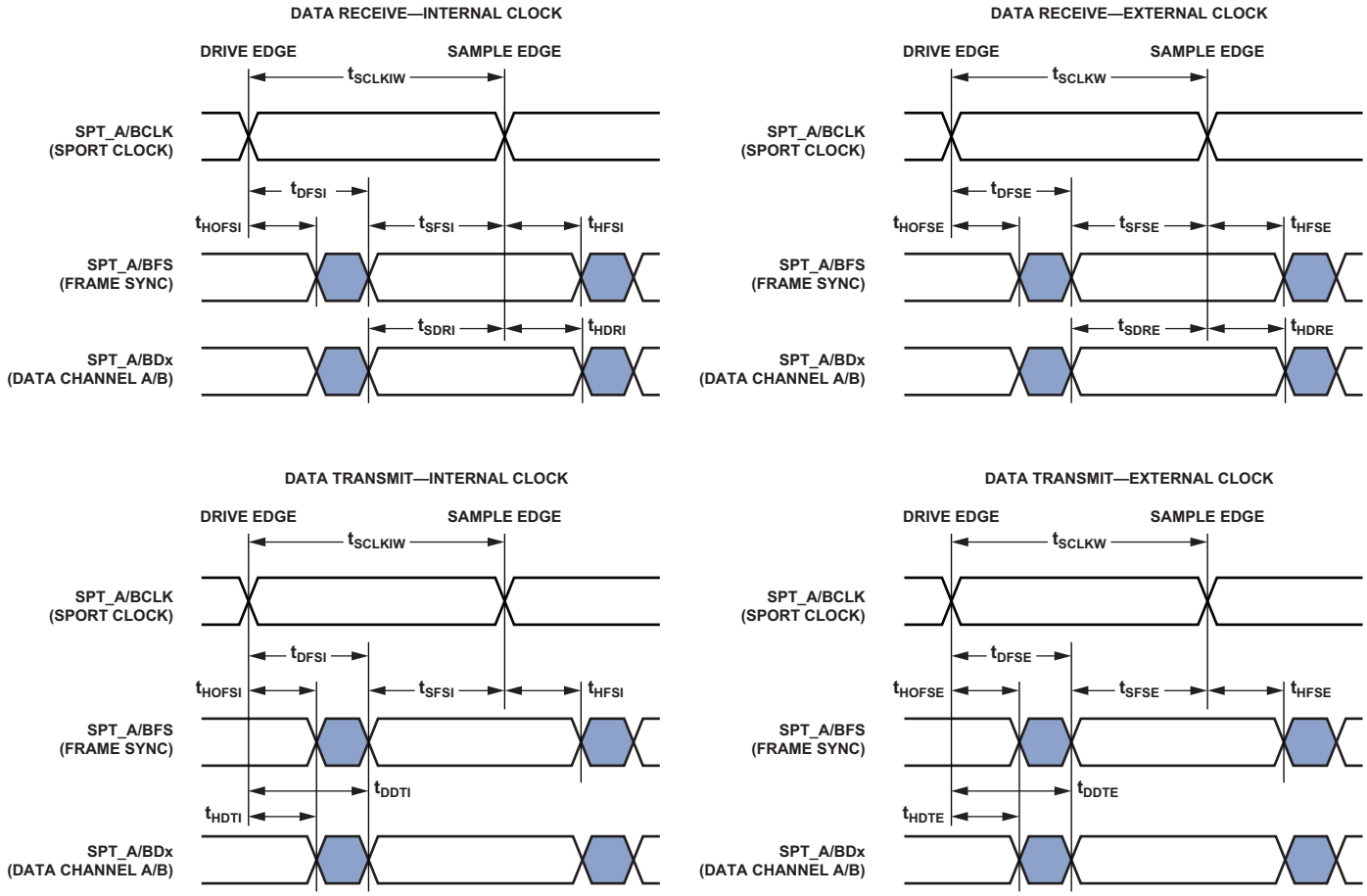


Figure 25. Serial Ports

Table 42. Serial Ports—Enable and Three-State

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		14		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1		–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8		2.8	ns

[1] Referenced to drive edge.

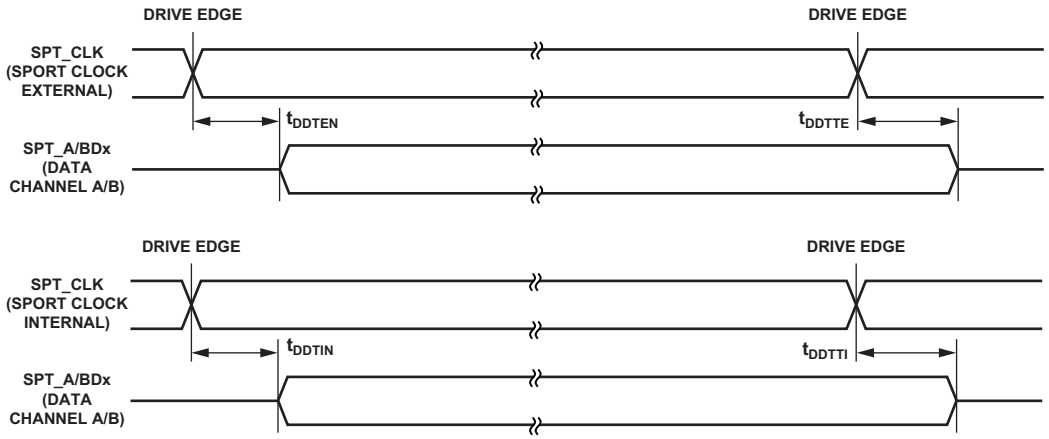


Figure 26. Serial Ports—Enable and Three-State

The SPT_TDV output signal becomes active in SPORT multi-channel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 43. Serial Ports—TDV (Transmit Data Valid)

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
t_{DRDVEN}	Data-Valid Enable Delay from Drive Edge of External Clock[1]	2.5		2.5		ns
t_{DFDVEN}	Data-Valid Disable Delay from Drive Edge of External Clock[1]		17.5		14.5	ns
t_{DRDVIN}	Data-Valid Enable Delay from Drive Edge of Internal Clock[1]	–4.5		–3.5		ns
t_{DFDVIN}	Data-Valid Disable Delay from Drive Edge of Internal Clock[1]		2		2	ns

[1] Referenced to drive edge.

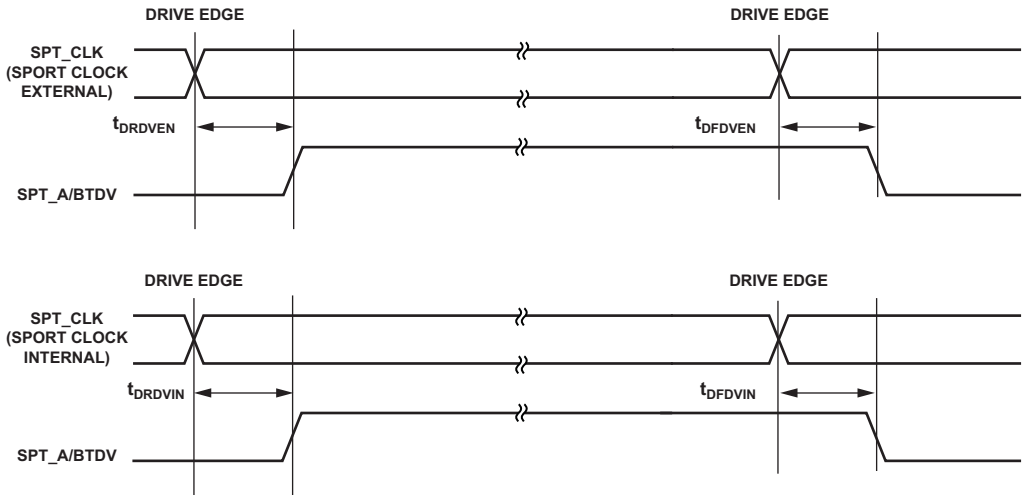


Figure 27. Serial Ports—Transmit Data Valid Internal and External Clock

Table 44. Serial Ports—External Late Frame Sync

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
$t_{DDTLFSE}$	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0[1]		19		15.5	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as standard serial mode, and MCE = 1, MFD = 0.

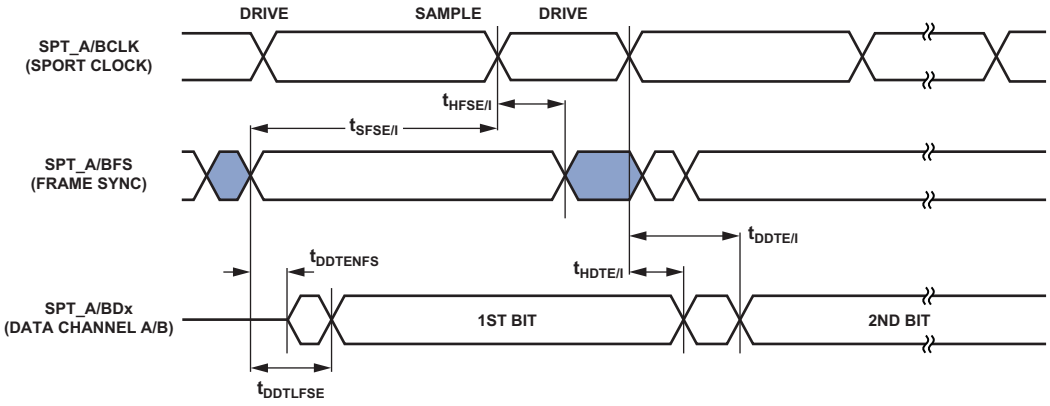


Figure 28. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 45 and Figure 29 describe SPI port master operations.

When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in MHz is set by the following equation where BAUD is a field in the SPI_CLK register that can be set from 0 to 65535:

$$f_{SPICLKPROG} = \frac{f_{SCLK0}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

Note that:

- In dual mode data transmit the SPI_MISO signal is also an output.
- In quad mode data transmit the SPI_MISO, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive the SPI_MOSI signal is also an input.
- In quad mode data receive the SPI_MOSI, SPI_D2, and SPI_D3 signals are also inputs.
- To add additional frame delays see the documentation for the SPI_DLY register in the hardware reference manual.

Table 45. Serial Peripheral Interface (SPI) Port—Master Timing

All specifications are based on simulation data and are subject to change without notice.

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	6.5		5.5		ns
t_{HSPIDM}	SPI_CLK Sampling Edge to Data Input Invalid	1		1		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPI_SEL}$ low to First SPI_CLK Edge	$0.5 \times t_{SCLK0} - 1.5$		$0.5 \times t_{SCLK0} - 1.5$		ns
t_{SPICHM}	SPI_CLK High Period[1]	$0.5 \times t_{SPICLKPROG} - 1.5$		$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLM}	SPI_CLK Low Period[1]	$0.5 \times t_{SPICLKPROG} - 1.5$		$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKPROG} - 1.5$		$t_{SPICLKPROG} - 1.5$		ns
t_{HDSM}	Last SPI_CLK Edge to $\overline{SPI_SEL}$ High	$(0.5 \times t_{SCLK0}) - 1.5$		$(0.5 \times t_{SCLK0}) - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$t_{SCLK0} - 1.5$		$t_{SCLK0} - 1.5$		ns
$t_{DDSPIDM}$	SPI_CLK Edge to Data Out Valid (Data Out Delay)		2.5		2	ns
$t_{HDSPIDM}$	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	–4.5		–3.5		ns

[1] See Table 17 on Page 48 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.

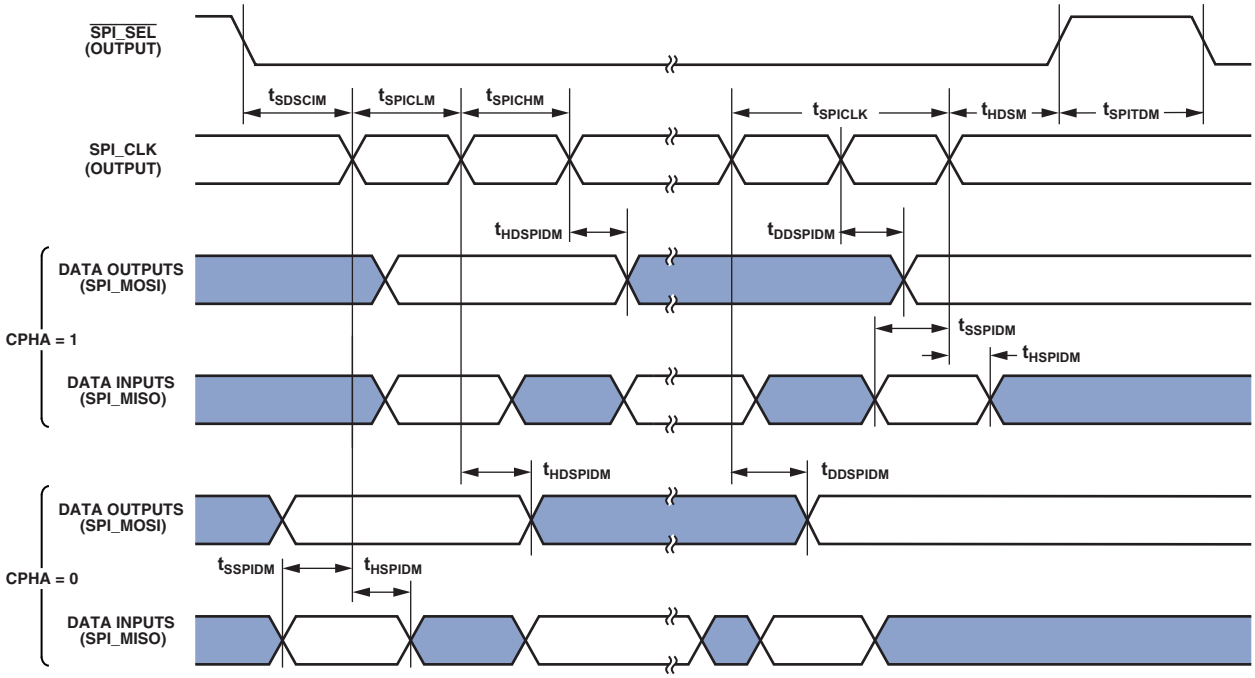


Figure 29. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 46 and Figure 30 describe SPI port slave operations. Note that:

- In dual mode data transmit the SPI_MOSI signal is also an output.
- In quad mode data transmit the SPI_MOSI, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive the SPI_MISO signal is also an input.
- In quad mode data receive the SPI_MISO, SPI_D2, and SPI_D3 signals are also inputs.
- In SPI slave mode the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

Table 46. Serial Peripheral Interface (SPI) Port—Slave Timing

All specifications are based on simulation data and are subject to change without notice.

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SPICHS}	SPI_CLK High Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1$		$(0.5 \times t_{SPICLKEXT}) - 1$		ns
t_{SPICLS}	SPI_CLK Low Period[1]	$(0.5 \times t_{SPICLKEXT}) - 1$		$(0.5 \times t_{SPICLKEXT}) - 1$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKEXT} - 1$		$t_{SPICLKEXT} - 1$		ns
t_{HDS}	Last SPI_CLK Edge to $\overline{\text{SPI_SS}}$ Not Asserted (non-SPIHP)	5		5		ns
t_{HDS}	Last SPI_CLK Edge to $\overline{\text{SPI_SS}}$ Not Asserted (using SPIHP)	$1.5 \times t_{SCLK0}$		$1.5 \times t_{SCLK0}$		ns
t_{SPITDS}	Sequential Transfer Delay (non-SPIHP)	$0.5 \times t_{SPICLK} - 1.5$		$0.5 \times t_{SPICLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay (using SPIHP)	$3 \times t_{SCLK0}$		$3 \times t_{SCLK0}$		ns
t_{SDSCI}	$\overline{\text{SPI_SS}}$ Assertion to First SPI_CLK Edge	11.5		11.5		ns
t_{SSPID}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	1.5		1		ns
t_{HSPID}	SPI_CLK Sampling Edge to Data Input Invalid	3		3		ns
Switching Characteristics						
t_{DSOE}	$\overline{\text{SPI_SS}}$ Assertion to Data Out Active	0	17.5	0	14.5	ns
t_{DSDHI}	$\overline{\text{SPI_SS}}$ Deassertion to Data High Impedance	0	13	0	11.5	ns
t_{DDSPID}	SPI_CLK Edge to Data Out Valid (Data Out Delay)		17.5		14.5	ns
t_{HDSPID}	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	2.5		2.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPI_CLK. For the external SPI_CLK ideal maximum frequency see the $f_{SPICLKTEXT}$ specification in the Clock Related Operating Conditions table on Page 48.

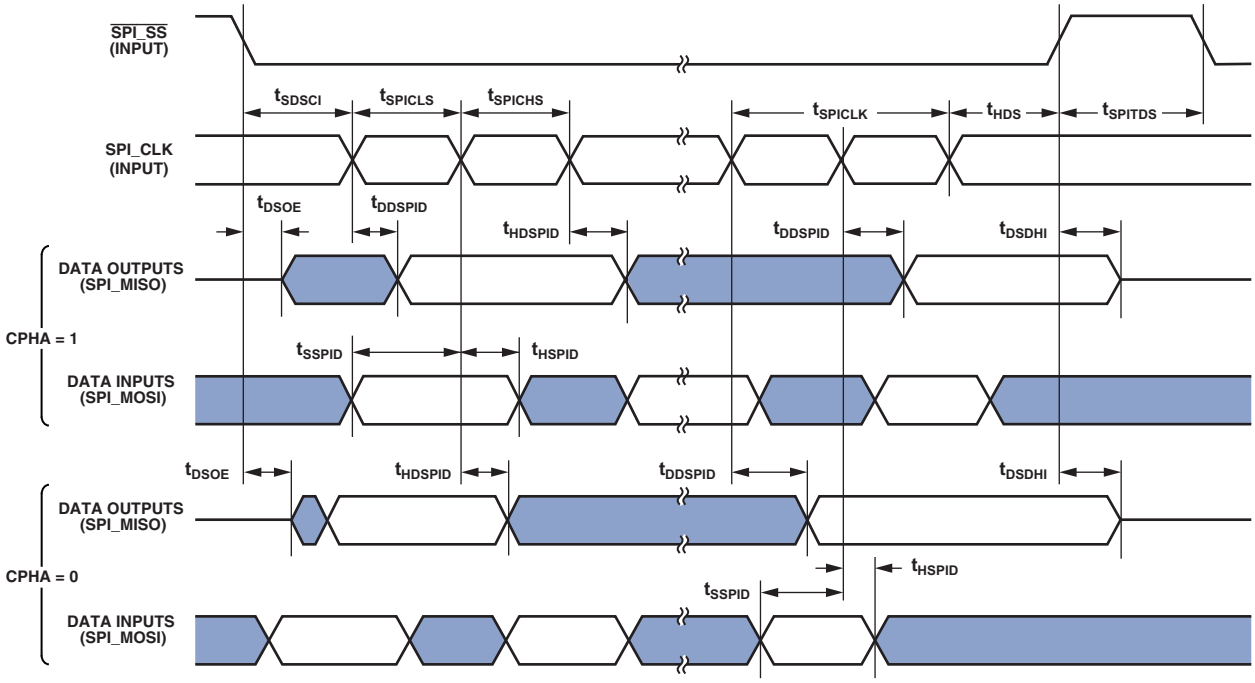


Figure 30. Serial Peripheral Interface (SPI) Port—Slave Timing

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 47. SPI Port—SPI_RDY Slave Timing

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

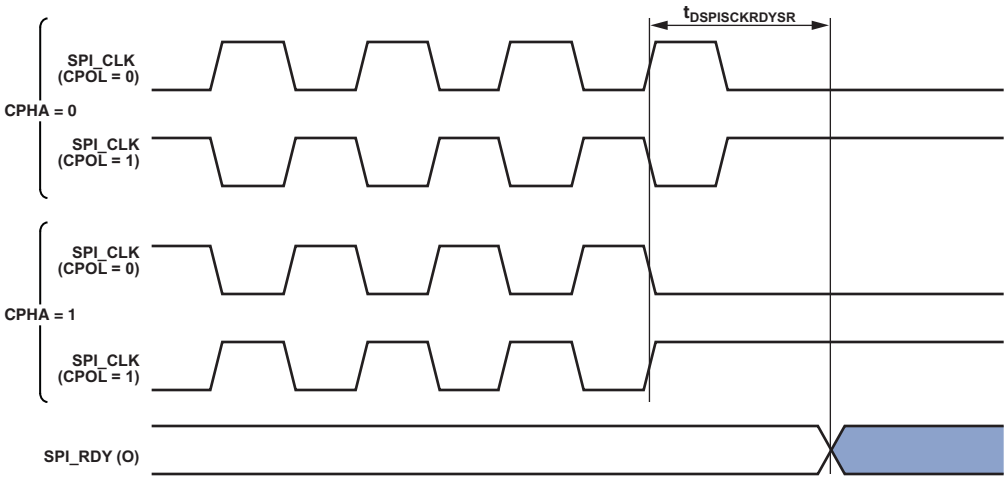


Figure 31. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

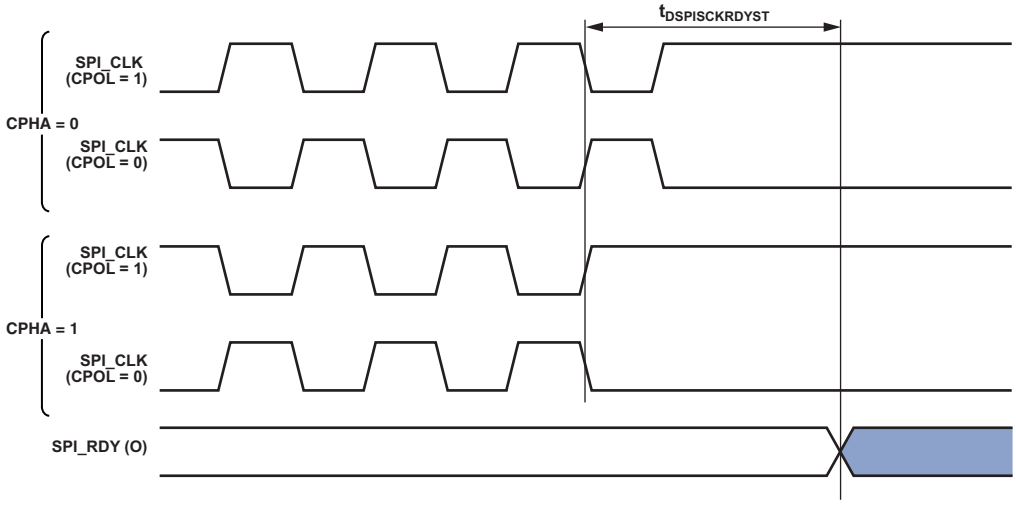


Figure 32. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

Serial Peripheral Interface (SPI) Port—Open Drain Mode Timing

In Figure 33 and Figure 34, the outputs can be SPI_MOSI SPI_MISO, SPI_D2, and/or SPI_D3 depending on the mode of operation.

Table 48. SPI Port ODM Master Mode Timing

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		**V_{DD_EXT} 3.3 V Nominal**		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
$t_{HDSPIODMM}$	SPI_CLK Edge to High Impedance from Data Out Valid	–4.5		–3.5		ns
$t_{DDSPIODMM}$	SPI_CLK Edge to Data Out Valid from High Impedance		2.5		2	ns

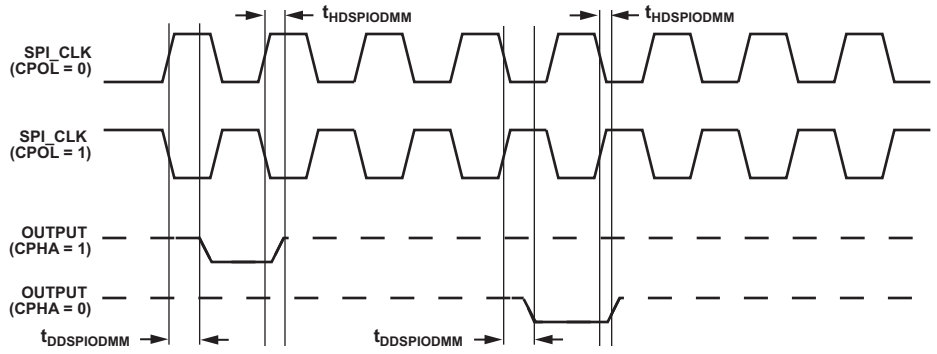


Figure 33. ODM Master

Table 49. SPI Port—ODM Slave Mode

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
$t_{HDSPIODMS}$	SPI_CLK Edge to High Impedance from Data Out Valid	2.5		2.5		ns
$t_{DDSPIODMS}$	SPI_CLK Edge to Data Out Valid from High Impedance		17.5		14.5	ns

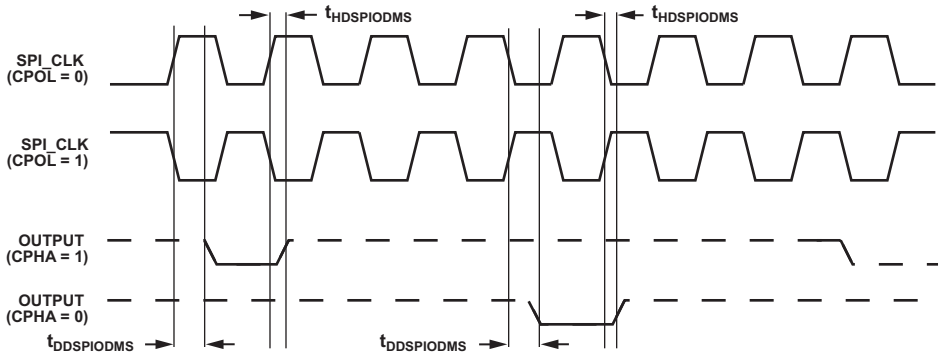


Figure 34. ODM Slave

Serial Peripheral Interface (SPI) Port—SPI_RDY Timing

SPI_RDY is used to provide flow control. The CPOL and CPHA bits are set in SPI_CTL, while LEADX, LAGX, and STOP are in SPI_DLY.

Table 50. SPI Port—SPI_RDY Timing

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_EXT} 1.8 V/3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{SRDYSCKM0}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 0	$(2.5 + 1.5 \times BAUD^{1}) \times t_{SCLK0} + 14.5$		ns
$t_{SRDYSCKM1}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	$(1.5 + BAUD^{1}) \times t_{SCLK0} + 14.5$		ns
Switching Characteristic				
$t_{SRDYSCKM}$	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 0 and BAUD = 0 (STOP, LEADX, LAGX = 0)	$3 \times t_{SCLK0}$	$4 \times t_{SCLK0} + 17.5$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 0 and BAUD ≥ 1 (STOP, LEADX, LAGX = 0)	$(4 + 1.5 \times BAUD^{1}) \times t_{SCLK0}$	$(5 + 1.5 \times BAUD^{1}) \times t_{SCLK0} + 17.5$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 1 (STOP, LEADX, LAGX = 0)	$(3 + 0.5 \times BAUD^{1}) \times t_{SCLK0}$	$(4 + 0.5 \times BAUD^{1}) \times t_{SCLK0} + 17.5$	ns

[1] BAUD value set using the SPI_CLK.BAUD bits.

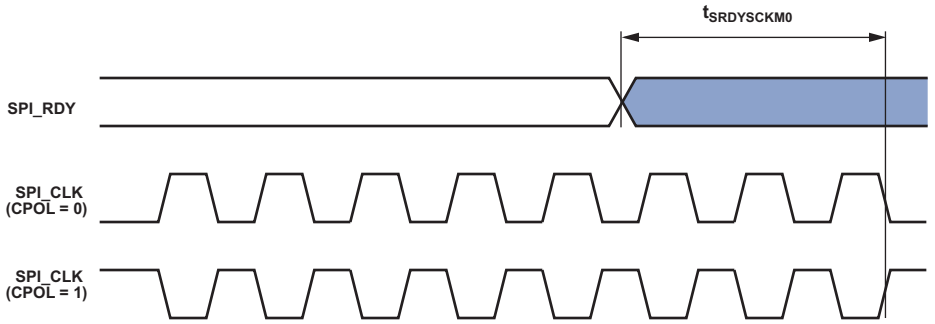


Figure 35. SPI_RDY Setup Before SPI_CLK with CPHA = 0

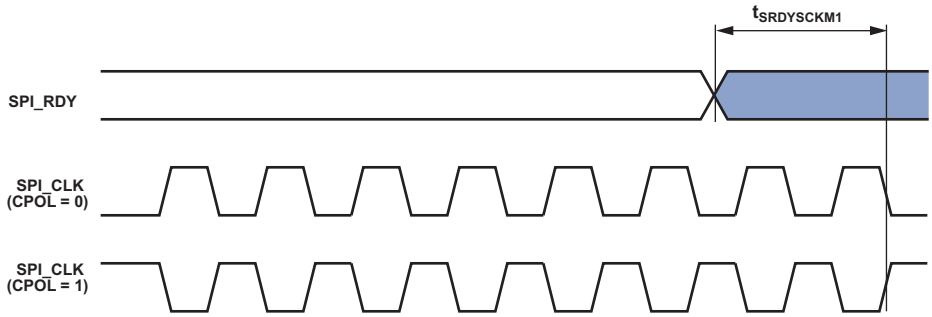


Figure 36. SPI_RDY Setup Before SPI_CLK with CPHA = 1

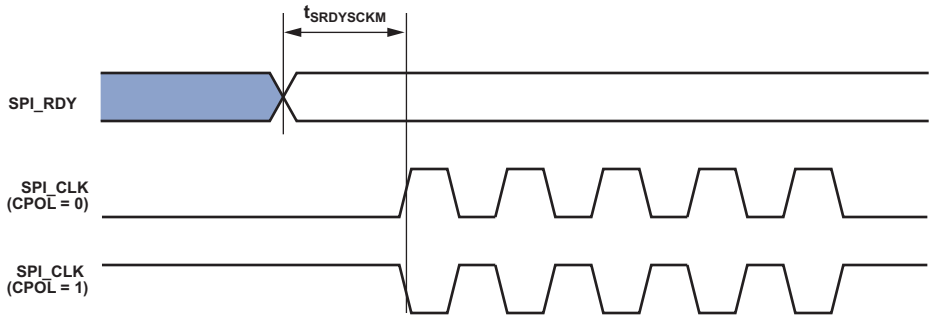


Figure 37. SPI_CLK Switching Diagram after SPI_RDY Assertion, CPHA = x

Enhanced Parallel Peripheral Interface Timing

The following tables and figures describe enhanced parallel peripheral interface timing operations. The POLC bits in the EPPI_CTL register may be used to set the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 51. Enhanced Parallel Peripheral Interface—Internal Clock

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		**V_{DD_EXT} 3.3 V Nominal**		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	1.5		0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.5		6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	1.5		0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	16.5		14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	1.5		0		ns
Switching Characteristics						
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 2$		$0.5 \times t_{PCLKPROG} - 2$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 2$		$t_{PCLKPROG} - 2$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		1.7		1.5	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–3.5		–2.5		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		1.7		1.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–3.5		–2.5		ns

[1] See Table 17 on Page 48 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{PCLKPROG}$.

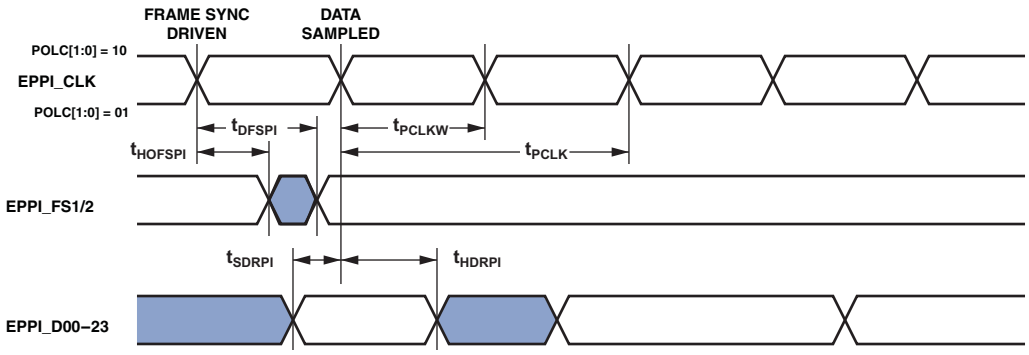


Figure 38. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

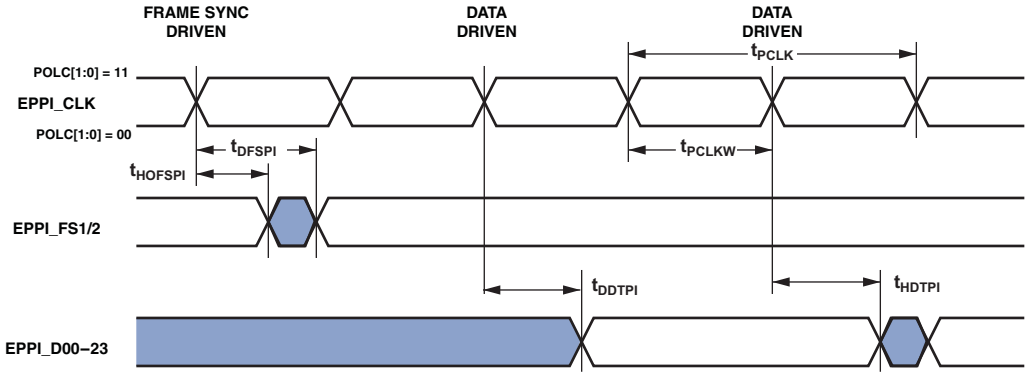


Figure 39. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

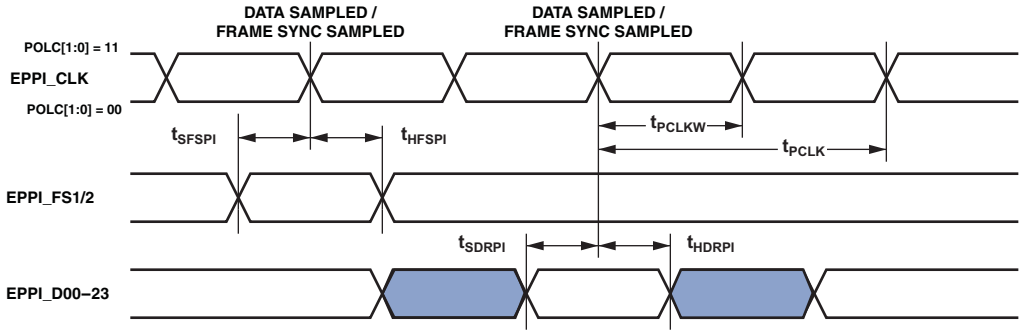


Figure 40. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

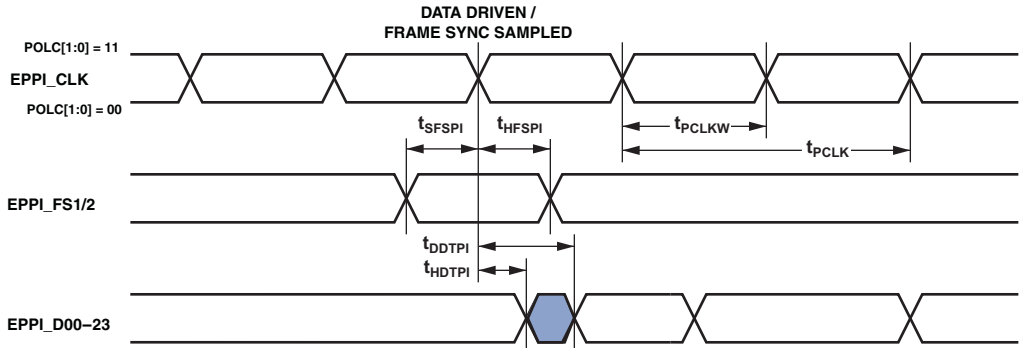


Figure 41. PPI Internal Clock GP Transmit Mode with External Frame Sync Timing

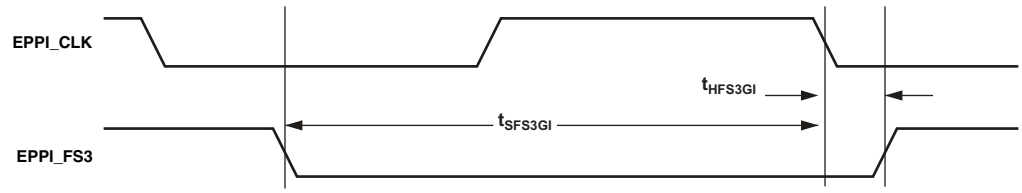


Figure 42. Clock Gating Mode with Internal Clock and External Frame Sync Timing

Table 52. Enhanced Parallel Peripheral Interface—External Clock

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{PCLKW}	EPPI_CLK Width[1]	$(0.5 \times t_{PCLKEXT}) - 1$		$(0.5 \times t_{PCLKEXT}) - 1$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKEXT} - 1$		$t_{PCLKEXT} - 1$		ns
t_{SFSPE}	External FS Setup Before EPPI_CLK	1.5		1		ns
t_{HFSPE}	External FS Hold After EPPI_CLK	3		3		ns
t_{SDRPE}	Receive Data Setup Before EPPI_CLK	1.5		1		ns
t_{HDRPE}	Receive Data Hold After EPPI_CLK	3		3		ns
Switching Characteristics						
t_{DFSPE}	Internal FS Delay After EPPI_CLK		17.5		14.5	ns
t_{HOFSPE}	Internal FS Hold After EPPI_CLK	2.5		2.5		ns
t_{DDTPE}	Transmit Data Delay After EPPI_CLK		17.5		14.5	ns
t_{HDTPE}	Transmit Data Hold After EPPI_CLK	2.5		2.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external EPPI_CLK. For the external EPPI_CLK ideal maximum frequency see the $f_{PCLKEXT}$ specification in Table 17 on Page 48.

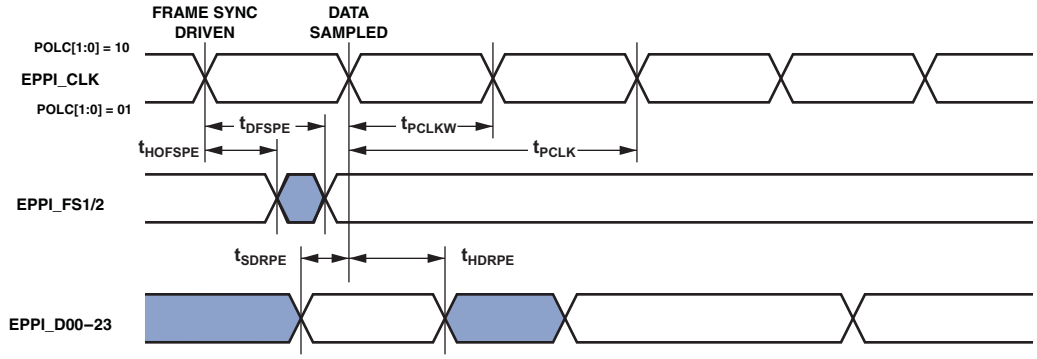


Figure 43. PPI External Clock GP Receive Mode with Internal Frame Sync Timing

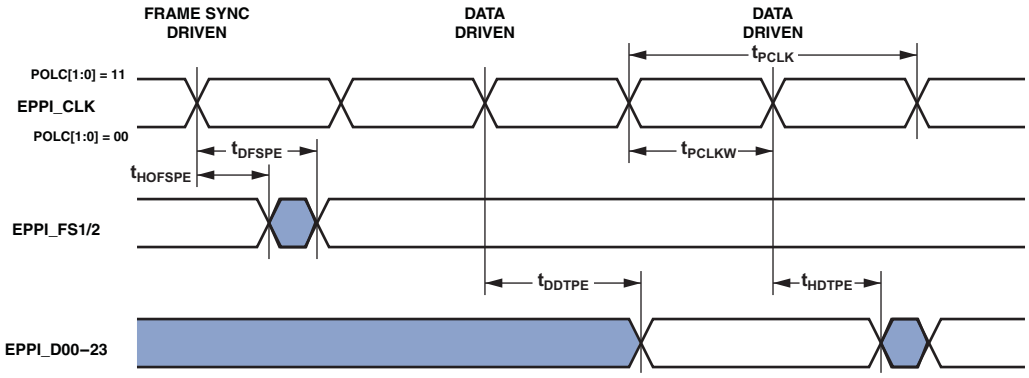


Figure 44. PPI External Clock GP Transmit Mode with Internal Frame Sync Timing

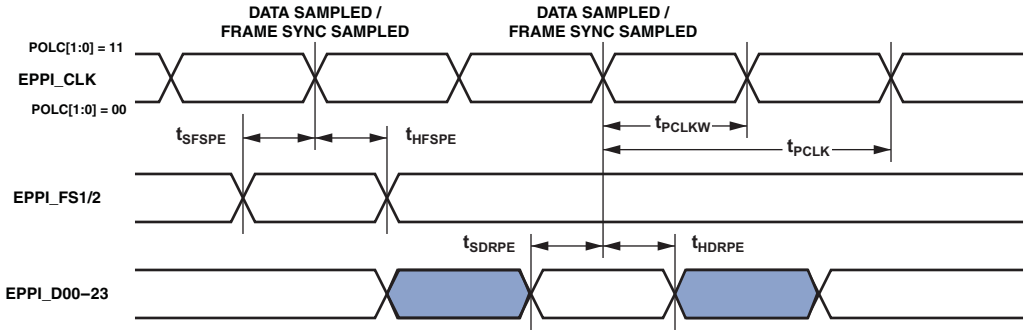


Figure 45. PPI External Clock GP Receive Mode with External Frame Sync Timing

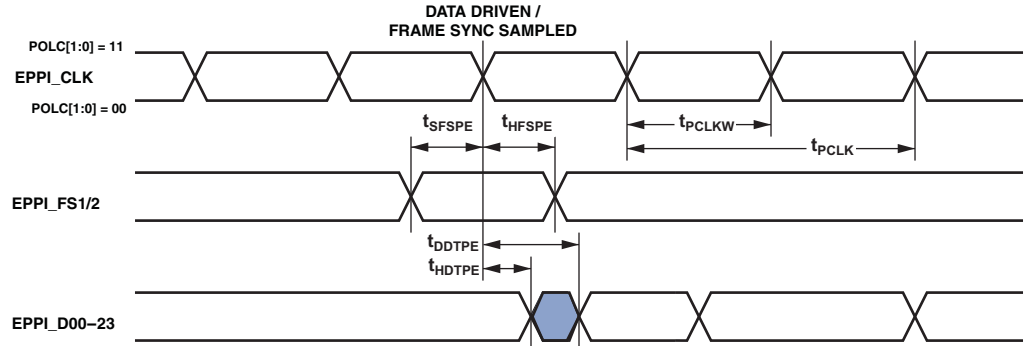


Figure 46. PPI External Clock GP Transmit Mode with External Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference Manual*.

CAN Interface

The CAN interface timing is described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference Manual*.

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 53 describes the USB On-The-Go receive and transmit operations.

Table 53. USB On-The-Go—Receive and Transmit Timing

All specifications are based on simulation data and are subject to change without notice.				
		V_{DD_USB} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{USBS}	USB_XI Frequency	24	24	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

MSI Controller Timing

Table 54 and Figure 47 describe RSI controller timing.

Table 54. MSI Controller Timing

All specifications are based on simulation data and are subject to change without notice.						
		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{ISU}	Input Setup Time	5		4.5		ns
t_{IH}	Input Hold Time	2		0.5		ns
Switching Characteristics						
f_{PP}	Clock Frequency Data Transfer Mode[1]		50		50	MHz
t_{WL}	Clock Low Time	7		7		ns
t_{WH}	Clock High Time	7		7		ns
t_{TLH}	Clock Rise Time		3		3	ns
t_{THL}	Clock Fall Time		3		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		3		4	ns
t_{OH}	Output Hold Time	–4		–3		ns

[1] $t_{PP} = 1/f_{PP}$

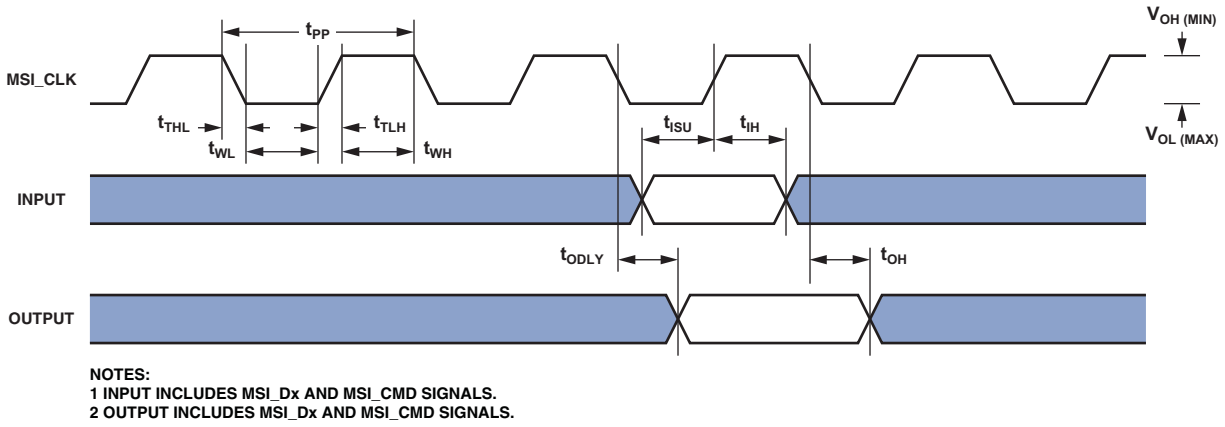


Figure 47. MSI Controller Timing

OUTPUT DRIVE CURRENTS

Figure TBD through Figure TBD show typical current-voltage characteristics for the output drivers of the ADSP-BF70x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

TEST CONDITIONS

All Timing Requirements appearing in this data sheet were measured under the conditions described in this section. Figure 48 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ for V_{DDEXT} (nominal) = 1.8 V/3.3 V.

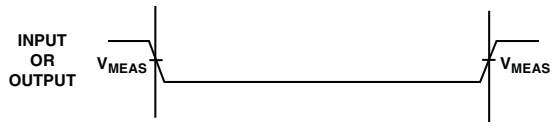


Figure 48. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output balls are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 49.

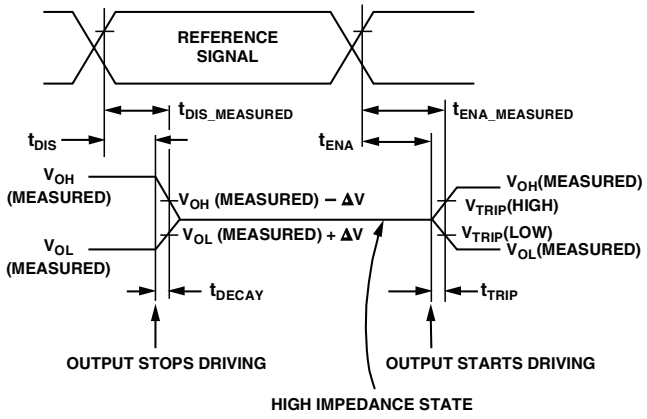


Figure 49. Output Enable/Disable

The time $t_{ENA_MEASURED}$ is the interval *from when* the reference signal switches *to when* the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). For V_{DDEXT} (nominal) = 1.8 V, V_{TRIP} (high) is 1.05 V, and V_{TRIP} (low) is 0.75 V. For V_{DDEXT} (nominal) = 3.3 V, V_{TRIP} (high) is 1.9 V, and V_{TRIP} (low) is 1.4 V. Time t_{TRIP} is the interval *from when* the output starts driving *to when* the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$$

If multiple balls (such as the data bus) are enabled, the measurement value is that of the first ball to start driving.

Output Disable Time Measurement

Output balls are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 49.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DDEXT} (nominal) = 3.3 V and 0.15 V for V_{DDEXT} (nominal) = 1.8V.

The time $t_{DIS_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 54.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 50). V_{LOAD} is equal to V_{DDEXT} /2. The graphs of TBD through TBD show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

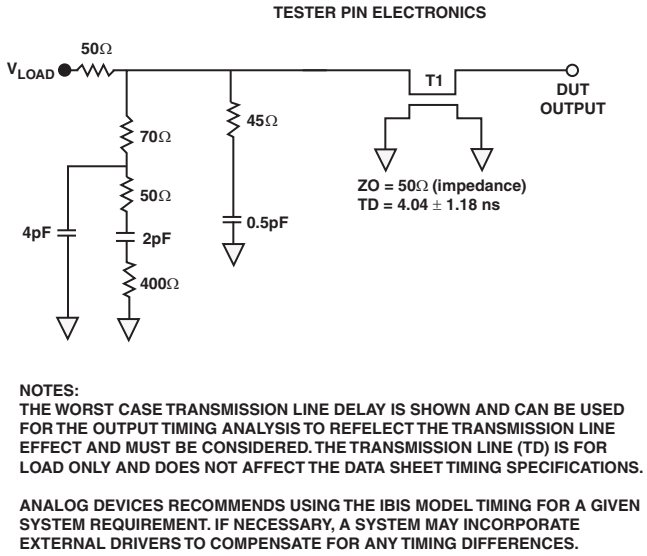


Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 55 and Table 56

P_D = Power dissipation (see Total Internal Power Dissipation on Page TBD for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

In Table 55 and Table 56, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 55. Thermal Characteristics for CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	28.7	°C/W
θ_{JMA}	1 linear m/s air flow	26.2	°C/W
θ_{JMA}	2 linear m/s air flow	25.2	°C/W
θ_{JC}		10.1	°C/W
Ψ_{JT}	0 linear m/s air flow	0.24	°C/W
Ψ_{JT}	1 linear m/s air flow	0.40	°C/W
Ψ_{JT}	2 linear m/s air flow	0.51	°C/W

Table 56. Thermal Characteristics for LFCSP (QFN)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	22.9	°C/W
θ_{JMA}	1 linear m/s air flow	17.9	°C/W
θ_{JMA}	2 linear m/s air flow	16.4	°C/W
θ_{JC}		2.26	°C/W
Ψ_{JT}	0 linear m/s air flow	0.14	°C/W
Ψ_{JT}	1 linear m/s air flow	0.27	°C/W
Ψ_{JT}	2 linear m/s air flow	0.30	°C/W

ADSP-BF70X 184-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Figure 51 shows an overview of signal placement on the 184-Ball CSP_BGA.

Table 57 lists the 184-Ball CSP_BGA package by ball number for the ADSP-BF70x. Table 58 lists the 184-Ball CSP_BGA package by signal.

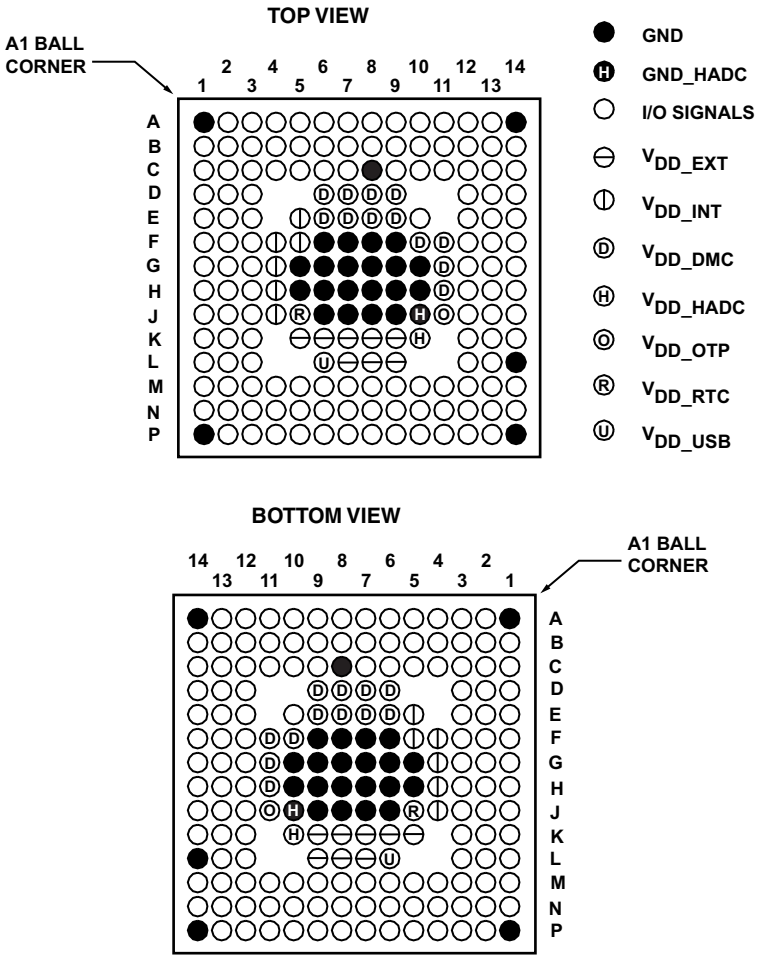


Figure 51. 184-Ball CSP_BGA Configuration

Table 57. 184-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A01	GND	D08	VDD_DMC	H03	SYS_CLKOUT	L14	GND
A02	DMC0_A09	D09	VDD_DMC	H04	VDD_INT	M01	PC_00
A03	DMC0_BA0	D12	PA_08	H05	GND	M02	RTC0_CLKIN
A04	DMC0_BA1	D13	DMC0_DQ06	H06	GND	M03	PB_15
A05	DMC0_BA2	D14	DMC0_DQ05	H07	GND	M04	PB_12
A06	$\overline{\text{DMC0_CAS}}$	E01	DMC0_A06	H08	GND	M05	PC_12
A07	$\overline{\text{DMC0_RAS}}$	E02	DMC0_A05	H09	GND	M06	USB0_VBUS
A08	DMC0_A13	E03	JTG_TDI	H10	GND	M07	USB0_VBC
A09	PA_03	E05	VDD_INT	H11	VDD_DMC	M08	PB_09
A10	DMC0_CK	E06	VDD_DMC	H12	PA_10	M09	PB_05
A11	$\overline{\text{DMC0_CK}}$	E07	VDD_DMC	H13	PA_11	M10	PB_04
A12	DMC0_LDQS	E08	VDD_DMC	H14	$\overline{\text{DMC0_UDQS}}$	M11	PB_01
A13	$\overline{\text{DMC0_LDQS}}$	E09	VDD_DMC	J01	PC_05	M12	PB_03
A14	GND	E10	DMC0_VREF	J02	PC_06	M13	DMC0_LDM
B01	DMC0_A07	E12	SYS_BMODE0	J03	$\overline{\text{SYS_RESOUT}}$	M14	SYS_CLKIN
B02	DMC0_A08	E13	DMC0_DQ08	J04	VDD_INT	N01	RTC0_XTAL
B03	DMC0_A11	E14	DMC0_DQ07	J05	VDD_RTC	N02	PB_14
B04	DMC0_A10	F01	DMC0_A01	J06	GND	N03	PB_11
B05	DMC0_A12	F02	DMC0_A02	J07	GND	N04	PC_14
B06	$\overline{\text{DMC0_WE}}$	F03	PC_09	J08	GND	N05	PC_11
B07	$\overline{\text{DMC0_CS0}}$	F04	VDD_INT	J09	GND	N06	USB0_ID
B08	DMC0_ODT	F05	VDD_INT	J10	GND_HADC	N07	USB0_DP
B09	DMC0_CKE	F06	GND	J11	VDD_OTP	N08	PB_08
B10	DMC0_DQ00	F07	GND	J12	PA_13	N09	PB_06
B11	DMC0_DQ02	F08	GND	J13	DMC0_DQ13	N10	PB_00
B12	DMC0_DQ01	F09	GND	J14	DMC0_UDQS	N11	HADC0_VIN2
B13	DMC0_DQ04	F10	VDD_DMC	K01	PC_04	N12	HADC0_VIN1
B14	DMC0_DQ03	F11	VDD_DMC	K02	PC_01	N13	PA_15
C01	JTG_TDO_SWO	F12	$\overline{\text{SYS_FAULT}}$	K03	PC_02	N14	SYS_XTAL
C02	JTG_TMS_SWDIO	F13	DMC0_DQ10	K05	VDD_EXT	P01	GND
C03	JTG_TCK_SWCLK	F14	DMC0_DQ09	K06	VDD_EXT	P02	PB_13
C04	PA_01	G01	DMC0_A03	K07	VDD_EXT	P03	PB_10
C05	SYS_EXTWAKE	G02	PA_00	K08	VDD_EXT	P04	PC_13
C06	PA_02	G03	PC_08	K09	VDD_EXT	P05	USB0_XTAL
C07	$\overline{\text{SYS_NMI}}$	G04	VDD_INT	K10	VDD_HADC	P06	USB0_CLKIN
C08	GND	G05	GND	K12	PA_12	P07	USB0_DM
C09	PA_04	G06	GND	K13	DMC0_DQ15	P08	PB_07
C10	PA_05	G07	GND	K14	DMC0_DQ14	P09	HADC0_VREFN
C11	PA_06	G08	GND	L01	PC_03	P10	HADC0_VREFP
C12	PA_07	G09	GND	L02	TWI0_SDA	P11	HADC0_VIN3
C13	$\overline{\text{SYS_HWRST}}$	G10	GND	L03	TWI0_SCL	P12	HADC0_VIN0
C14	SYS_BMODE1	G11	VDD_DMC	L06	VDD_USB	P13	PA_14
D01	DMC0_A00	G12	PA_09	L07	VDD_EXT	P14	GND
D02	DMC0_A04	G13	DMC0_DQ11	L08	VDD_EXT		
D03	$\overline{\text{JTG_TRST}}$	G14	DMC0_DQ12	L09	VDD_EXT		
D06	VDD_DMC	H01	PC_07	L12	PB_02		
D07	VDD_DMC	H02	PC_10	L13	DMC0_UDM		

Table 58. ADSP-BF70x 184-Ball CSP_BGA Ball Assignments (Alphabetical by Signal Name)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
DMC0_A00	D01	DMC0_WE	B06	PA_08	D12	SYS_HWRST	C13
DMC0_A01	F01	GND	C08	PA_09	G12	SYS_NMI	C07
DMC0_A02	F02	GND	A01	PA_10	H12	SYS_RESOUT	J03
DMC0_A03	G01	GND	A14	PA_11	H13	SYS_XTAL	N14
DMC0_A04	D02	GND	F06	PA_12	K12	TWI0_SCL	L03
DMC0_A05	E02	GND	F07	PA_13	J12	TWI0_SDA	L02
DMC0_A06	E01	GND	F08	PA_14	P13	USB0_CLKIN	P06
DMC0_A07	B01	GND	F09	PA_15	N13	USB0_DM	P07
DMC0_A08	B02	GND	G05	PB_00	N10	USB0_DP	N07
DMC0_A09	A02	GND	G06	PB_01	M11	USB0_ID	N06
DMC0_A10	B04	GND	G07	PB_02	L12	USB0_VBC	M07
DMC0_A11	B03	GND	G08	PB_03	M12	USB0_VBUS	M06
DMC0_A12	B05	GND	G09	PB_04	M10	USB0_XTAL	P05
DMC0_A13	A08	GND	G10	PB_05	M09	VDD_DMC	D06
DMC0_BA0	A03	GND	H05	PB_06	N09	VDD_DMC	D07
DMC0_BA1	A04	GND	H06	PB_07	P08	VDD_DMC	D08
DMC0_BA2	A05	GND	H07	PB_08	N08	VDD_DMC	D09
DMC0_CAS	A06	GND	H08	PB_09	M08	VDD_DMC	E06
DMC0_CK	A10	GND	H09	PB_10	P03	VDD_DMC	E07
DMC0_CKE	B09	GND	H10	PB_11	N03	VDD_DMC	E08
DMC0_CK	A11	GND	J06	PB_12	M04	VDD_DMC	E09
DMC0_CS0	B07	GND	J07	PB_13	P02	VDD_DMC	F10
DMC0_DQ00	B10	GND	J08	PB_14	N02	VDD_DMC	F11
DMC0_DQ01	B12	GND	J09	PB_15	M03	VDD_DMC	G11
DMC0_DQ02	B11	GND	L14	PC_00	M01	VDD_DMC	H11
DMC0_DQ03	B14	GND	P01	PC_01	K02	VDD_EXT	K05
DMC0_DQ04	B13	GND	P14	PC_02	K03	VDD_EXT	K06
DMC0_DQ05	D14	GND_HADC	J10	PC_03	L01	VDD_EXT	K07
DMC0_DQ06	D13	HADC0_VIN0	P12	PC_04	K01	VDD_EXT	K08
DMC0_DQ07	E14	HADC0_VIN1	N12	PC_05	J01	VDD_EXT	K09
DMC0_DQ08	E13	HADC0_VIN2	N11	PC_06	J02	VDD_EXT	L07
DMC0_DQ09	F14	HADC0_VIN3	P11	PC_07	H01	VDD_EXT	L08
DMC0_DQ10	F13	HADC0_VREFN	P09	PC_08	G03	VDD_EXT	L09
DMC0_DQ11	G13	HADC0_VREFP	P10	PC_09	F03	VDD_HADC	K10
DMC0_DQ12	G14	JTG_TCK_SWCLK	C03	PC_10	H02	VDD_INT	E05
DMC0_DQ13	J13	JTG_TDI	E03	PC_11	N05	VDD_INT	F04
DMC0_DQ14	K14	JTG_TDO_SWO	C01	PC_12	M05	VDD_INT	F05
DMC0_DQ15	K13	JTG_TMS_SWDIO	C02	PC_13	P04	VDD_INT	G04
DMC0_LDM	M13	JTG_TRST	D03	PC_14	N04	VDD_INT	H04
DMC0_LDQS	A12	PA_00	G02	RTC0_CLKIN	M02	VDD_INT	J04
DMC0_LDQS	A13	PA_01	C04	RTC0_XTAL	N01	VDD_OTP	J11
DMC0_ODT	B08	PA_02	C06	SYS_BMODE0	E12	VDD_RTC	J05
DMC0_RAS	A07	PA_03	A09	SYS_BMODE1	C14	VDD_USB	L06
DMC0_UDM	L13	PA_04	C09	SYS_CLKIN	M14		
DMC0_UDQS	J14	PA_05	C10	SYS_CLKOUT	H03		
DMC0_UDQS	H14	PA_06	C11	SYS_EXTWAKE	C05		
DMC0_VREF	E10	PA_07	C12	SYS_FAULT	F12		

ADSP-BF70X 12 MM × 12 MM 88-LEAD LFCSP (QFN) LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

Figure 52 shows an overview of signal placement on the 12 mm × 12 mm 88-Lead LFCSP (QFN).

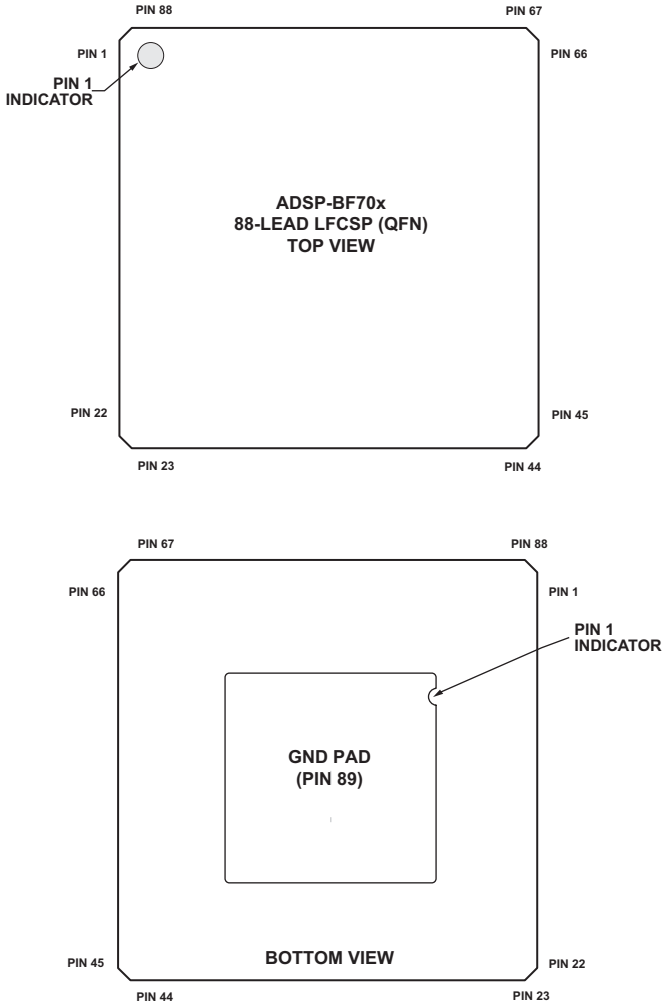


Figure 52. 12 mm × 12 mm 88-Lead LFCSP (QFN) Configuration

Table 59 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by lead number for the ADSP-BF70x. Table 60 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by signal.

Table 59. 12 mm × 12 mm 88-Lead LFCSP(QFN) Lead Assignment (Numerical by Lead Number)

Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name
1	PC_10	24	PB_14	47	PB_02	70	PA_07
2	PC_09	25	PB_13	48	PB_01	71	PA_06
3	PC_08	26	VDD_EXT	49	VDD_OTP	72	VDD_EXT
4	VDD_EXT	27	PB_12	50	VDD_EXT	73	PA_05
5	PC_07	28	PB_11	51	VDD_INT	74	PA_04
6	PC_06	29	PB_10	52	PB_00	75	PA_03
7	PC_05	30	VDD_INT	53	PA_15	76	GND
8	PC_04	31	USB0_XTAL	54	PA_14	77	$\overline{\text{SYS_NMI}}$
9	PC_03	32	USB0_CLKIN	55	VDD_EXT	78	PA_02
10	PC_02	33	USB0_ID	56	SYS_XTAL	79	SYS_EXTWAKE
11	VDD_EXT	34	USB0_VBUS	57	SYS_CLKIN	80	PA_01
12	SYS_CLKOUT	35	USB0_DP	58	PA_13	81	VDD_INT
13	PC_01	36	VDD_USB	59	PA_12	82	VDD_EXT
14	VDD_INT	37	USB0_DM	60	PA_11	83	JTG_TDO_SWO
15	$\overline{\text{SYS_RESOUT}}$	38	USB0_VBC	61	VDD_INT	84	JTG_TMS_SWDIO
16	PC_00	39	PB_09	62	VDD_EXT	85	JTG_TCK_SWCLK
17	VDD_EXT	40	PB_08	63	PA_10	86	JTG_TDI
18	TWI0_SDA	41	VDD_EXT	64	PA_09	87	$\overline{\text{JTG_TRST}}$
19	TWI0_SCL	42	PB_07	65	$\overline{\text{SYS_FAULT}}$	88	PA_00
20	RTC0_XTAL	43	PB_06	66	SYS_BMODE0	89*	GND
21	RTC0_CLKIN	44	PB_05	67	SYS_BMODE1		
22	VDD_RTC	45	PB_04	68	$\overline{\text{SYS_HWRST}}$		
23	PB_15	46	PB_03	69	PA_08		

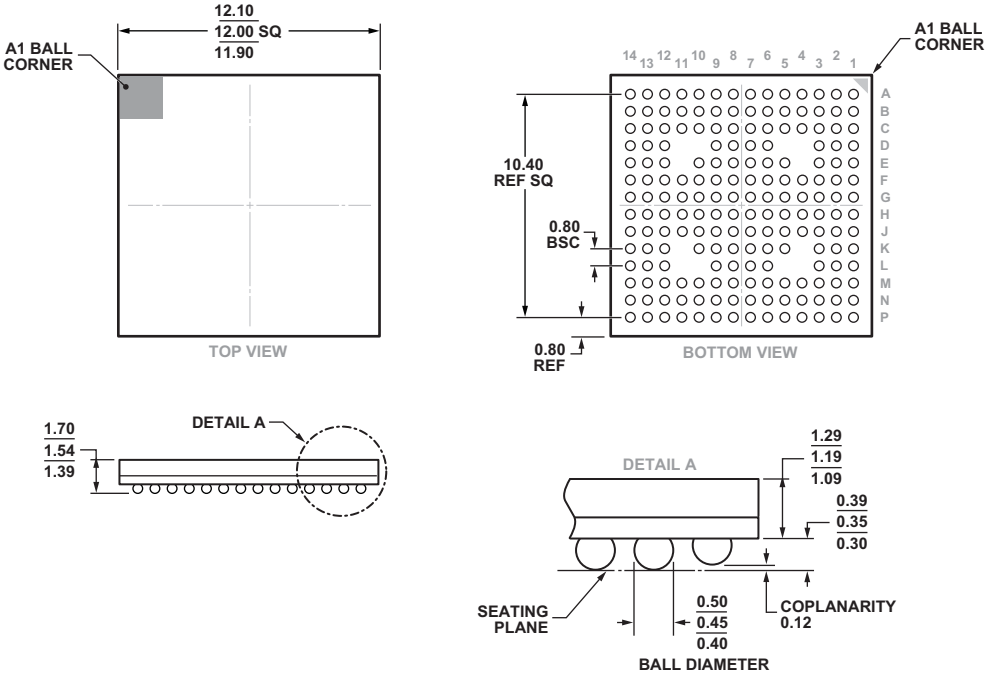
*Pin no. 89 is the GND supply (seeFigure 52) for the processor; this pad must connect to GND.

Table 60. ADSP-BF70x 12 mm × 12 mm 88 -Lead LFCSP(QFN) Lead Assignments (Alphabetical by Signal Name)

Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.
GND	76	PB_00	52	PC_07	5	USB0_VBUS	34
GND	89	PB_01	48	PC_08	3	USB0_XTAL	31
JTG_TCK_SWCLK	85	PB_02	47	PC_09	2	VDD_EXT	4
JTG_TDI	86	PB_03	46	PC_10	1	VDD_EXT	11
JTG_TDO_SWO	83	PB_04	45	RTC0_CLKIN	21	VDD_EXT	17
JTG_TMS_SWDIO	84	PB_05	44	RTC0_XTAL	20	VDD_EXT	26
$\overline{\text{JTG_TRST}}$	87	PB_06	43	SYS_BMODE0	66	VDD_EXT	41
PA_00	88	PB_07	42	SYS_BMODE1	67	VDD_EXT	50
PA_01	80	PB_08	40	SYS_CLKIN	57	VDD_EXT	55
PA_02	78	PB_09	39	SYS_CLKOUT	12	VDD_EXT	62
PA_03	75	PB_10	29	SYS_EXTWAKE	79	VDD_EXT	72
PA_04	74	PB_11	28	$\overline{\text{SYS_FAULT}}$	65	VDD_EXT	82
PA_05	73	PB_12	27	$\overline{\text{SYS_HWRST}}$	68	VDD_INT	14
PA_06	71	PB_13	25	$\overline{\text{SYS_NMI}}$	77	VDD_INT	30
PA_07	70	PB_14	24	$\overline{\text{SYS_RESOUT}}$	15	VDD_INT	51
PA_08	69	PB_15	23	SYS_XTAL	56	VDD_INT	61
PA_09	64	PC_00	16	TWI0_SCL	19	VDD_INT	81
PA_10	63	PC_01	13	TWI0_SDA	18	VDD_OTP	49
PA_11	60	PC_02	10	USB0_CLKIN	32	VDD_RTC	22
PA_12	59	PC_03	9	USB0_DM	37	VDD_USB	36
PA_13	58	PC_04	8	USB0_DP	35		
PA_14	54	PC_05	7	USB0_ID	33		
PA_15	53	PC_06	6	USB0_VBC	38		

OUTLINE DIMENSIONS

Dimensions for the 12 mm × 12 mm CSP_BGA package in Figure 53 are shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MO-275-GGAA-1

Figure 53. 184-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-184-1) Dimensions shown in millimeters

Dimensions for the 12 mm × 12 mm LFCSP_VQ (QFN) package in Figure 54 are shown in millimeters.

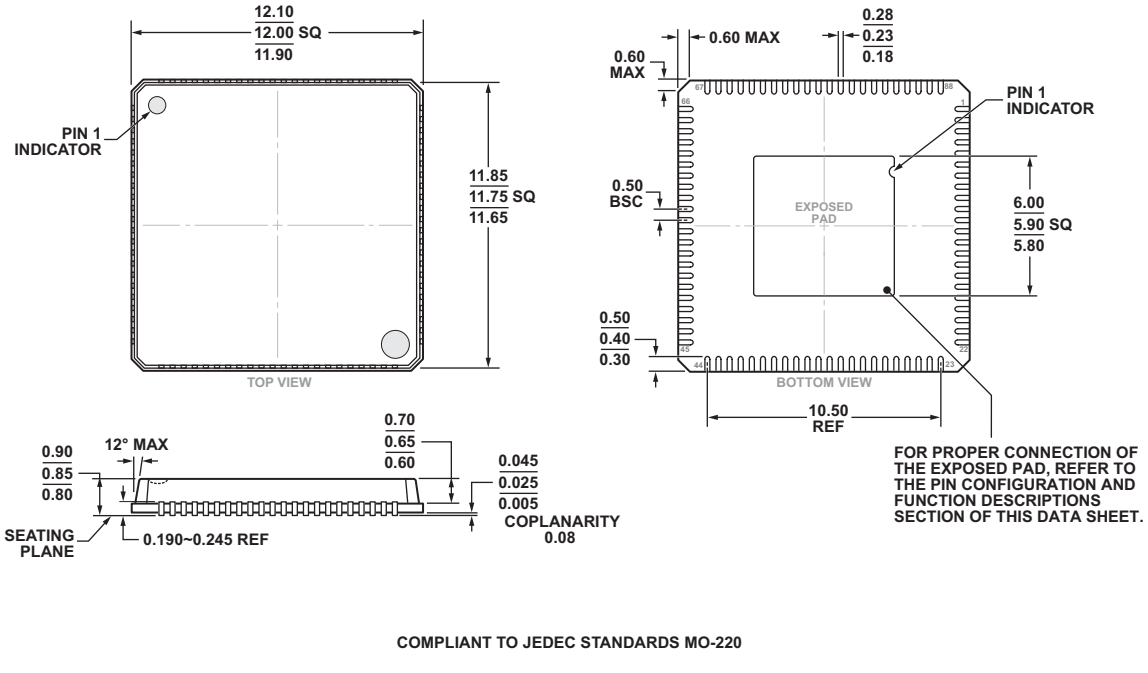


Figure 54. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ(QFN)]
(CP-88-8)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 61 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 61. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-184-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter

PRE RELEASE PRODUCTS

Model[1]	Max. Core Clock	Temperature Range[2, 3]	Package Description	Package Option
ADSP-BF707BBCZ-ENG	400 MHz	NA	184-Ball CSP_BGA	BC-184-1
ADSP-BF706BCPZ-ENG	400 MHz	NA	88-Lead LFCSP (QFN)	CP-88-8

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 47 for the junction temperature (T_J) specification which is the only temperature specification.

[3] These are pre production parts and are not guaranteed to meet the temperature specification. Test temperature will be provided for all samples.

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