AT30TSE752A, AT30TSE754A, AT30TSE758A

9- to 12-bit Selectable, ±0.5°C Accurate Digital Temperature Sensor with Nonvolatile Registers and Serial EEPROM

DATASHEET

Features

- Integrated Temperature Sensor + Nonvolatile Registers + Serial EEPROM
- 2-Wire I^2C and SMBus™ compatible serial interface
  - Supports SMBus Timeout
  - Supports SMBus Alert and Alert Response Address (ARA)
  - Selectable addressing allows up to eight devices on the same bus
- Single 1.7V to 5.5V supply
- 400kHz and 1MHz compatibility
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-lead SOIC (150-mil)
  - 8-lead MSOP (3.0 x 3.0mm)
  - 8-pad Ultra Thin DFN (UDFN — 2.0 x 3.0 x 0.6mm)

Digital Temperature Sensor Features

- Measures temperature from -55°C to +125°C
- Highly accurate temperature measurements requiring no external components
  - ±0.5°C accuracy (typical) over the 0°C to +85°C range
  - ±1.0°C accuracy (typical) over the -25°C to +105°C range
  - ±2.0°C accuracy (typical) over the -40°C to +125°C range
- Pin and software compatible to industry-standard LM75-type devices
- User-configurable resolution
  - 9 to 12 bits (0.5°C to 0.0625°C)
- User-configurable high and low temperature limits
- Nonvolatile registers to retain user-configured or pre-defined power-up defaults
- Register locking to prevent erroneous misconfiguration
- Register lockdown for permanent, non-changeable device configuration
- One-Shot mode for single temperature measurement while in Shutdown mode
- ALERT output pin for indicating temperature alarms
- Low power dissipation
  - 75µA active current (typical) during temperature measurements
- Shutdown mode to minimize power consumption
  - 1µA active current (typical)

Serial EEPROM Features

- Atmel® AT30TSE752A Integrates 2Kb of EEPROM
- Atmel AT30TSE754A Integrates 4Kb of EEPROM
- Atmel AT30TSE758A Integrates 8Kb of EEPROM
- Reversible software Write protection for full array
- Supports byte and Page Write operations
- Self-timed write cycle (5ms maximum)
- High-reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years

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1. Description

The Atmel® AT30TSE752A/754A/758A are a complete, precise temperature monitoring device designed for use in a variety of applications that require the measuring of local temperatures as an integral part of the system's function and/or reliability. The AT30TSE752A/754A/758A devices combine a high-precision digital temperature sensor, programmable high and low temperature alarms, and a 2-wire I^2C and SMBus (System Management Bus) compatible serial interface into a single, compact package.

The temperature sensor can measure temperatures over the full -55°C to +125°C temperature range and has a typical accuracy as precise as ±0.5°C from 0°C to +85°C. The result of the digitized temperature measurements are stored in one of the AT30TSE752A/754A/758A's internal registers, which is readable at any time through the device's serial interface.

The AT30TSE752A/754A/758A utilizes flexible, user-programmable internal registers to configure the temperature sensor's performance and response to high and low temperature conditions. The device also contains a set of Nonvolatile Registers to retain the configuration and temperature limit settings even after the device has been power cycled, thereby eliminating the need for the device to be reconfigured after each Power-up operation. This additional flexibility permits the device to run self-contained and not rely upon a host controller for device configuration.

In addition, the AT30TSE752A/754A/758A contain a 2Kb, 4Kb, or 8Kb Serial EEPROM that can be used to store vital user system configuration and preference data. This additional feature permits the device to replace an existing 2-wire I^2C Serial EEPROM in an application saving board space and component cost.

A dedicated alarm output activates if the temperature measurement exceeds the user-defined temperature and fault count limits. To reduce current consumption and save power, the AT30TSE752A/754A/758A features a Shutdown mode that turns off all internal circuitry except for the internal Power-On Reset (POR) and serial interface circuits. The device can also be configured to power-up in the Shutdown mode to ensure that the device remains in a low-power state until the user wishes to perform temperature measurements.

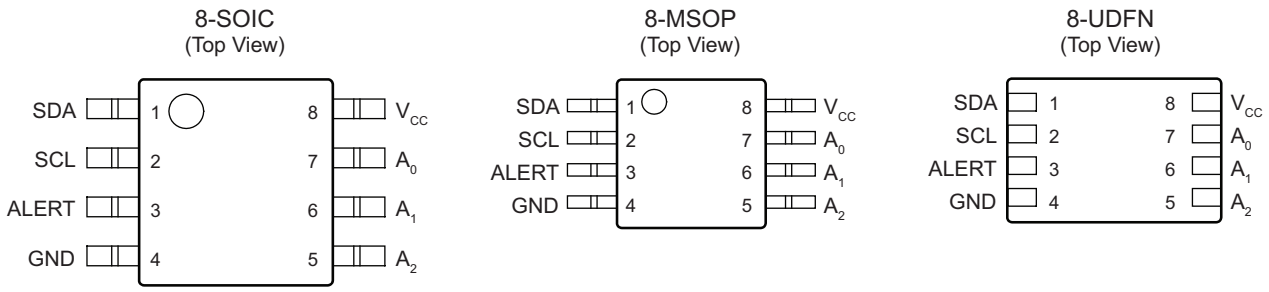
The AT30TSE752A/754A/758A are factory-calibrated and requires no external components to measure temperature. With its flexibility and high-degree of accuracy, the AT30TSE752A/754A/758A are ideal for extended temperature measurements in a wide variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

2. Pin Descriptions and Pinouts

Table 1. Pin Description

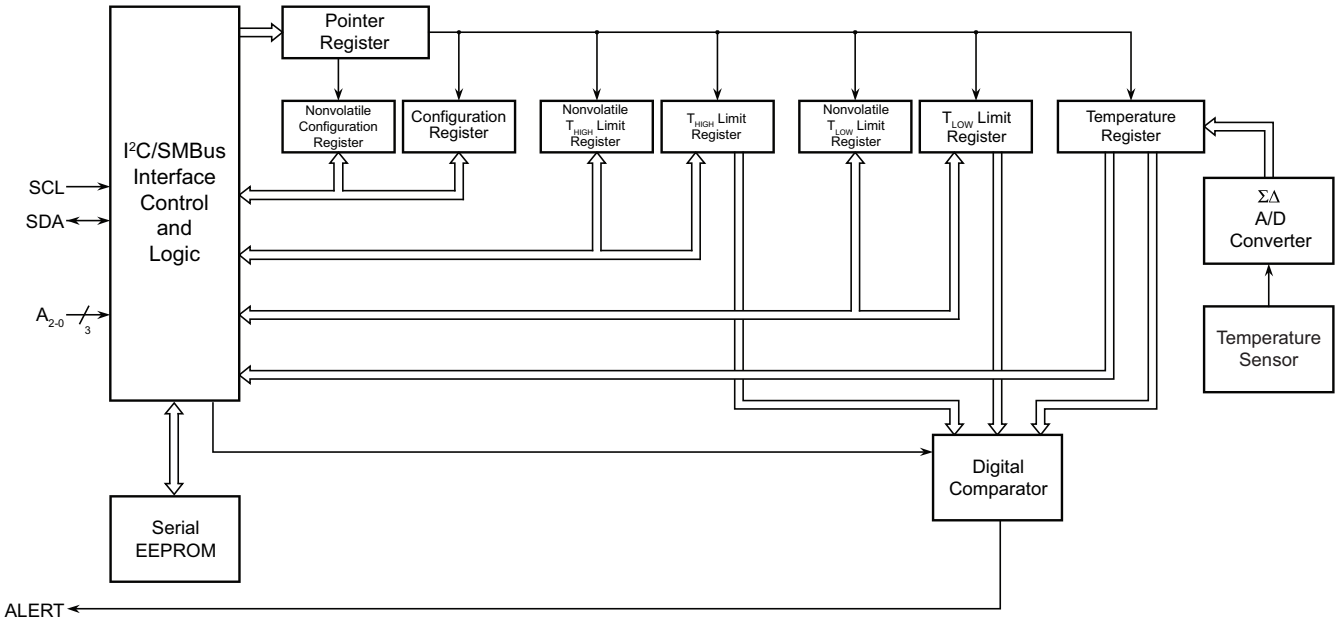
Symbol	Name and Function	Asserted State	Type
SCL	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor and may be wire-ANDed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/Output
ALERT	**ALERT:** The ALERT pin is an open-drain output pin used to indicate when the temperature goes beyond the user-programmed temperature limits. The ALERT pin can be operated in one of two different modes (Interrupt or Comparator mode) as defined by the CMP/INT bit in the Configuration Register. The ALERT pin defaults to an active-low output upon device power-up or reset but can be reconfigured as an active-high output by setting the POL bit in the Configuration Register. This pin can be wire-ANDed together with ALERT pins from other devices on the same bus. When wire-ANDing pins together, the ALERT pin should be configured as an active-low output so that when a single ALERT pin on the common alert bus goes active, the entire common alert bus will go low and the host controller will be properly notified since other ALERT pins that may be in the inactive-high state will not mask the true alert signal. In an SMBus environment, the SMBus host can respond by sending an SMBus ARA (Alert Response Address) command to determine which device on the SMBus generated the alert signal. The ALERT pin must be pulled-high using an external pull-up resistor even when it is not used. Care must also be taken to prevent this pin from being shorted directly to ground without a resistor at any time whether during testing or normal operation.	—	Output
A_{2-0}	**Address Inputs:** The A_{2-0} pins are used to select the device address and correspond to the three Least-Significant Bits (LSBs) of the I^2C/SMBus 7-bit slave address. These pins can be directly connected in any combination to V_{CC} or GND, and by utilizing the A_{2-0} pins, up to eight devices may be addressed on a single bus. The A_{2-0} pins are internally pulled to GND and may be left floating; however, it is highly recommended that the A_{2-0} pins always be directly connected to V_{CC} or GND to ensure a known address state.	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power

Figure 1. Pin Configurations



3. Block Diagram

Figure 3-1. Block Diagram



4. Device Communication

The AT30TSE752A/754A/758A operates as a slave device and utilizes a simple 2-wire I^2C and SMBus compatible digital serial interface to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master as well as to send data back to the Master. Data is always latched into the AT30TSE752A/754A/758A on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in the logic-high state. The Master uses a Start condition to initiate any data transfer sequence, and the Start condition must precede any command. The AT30TSE752A/754A/758A will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic-high state. The Master uses the Stop condition to end a data transfer sequence to the AT30TSE752A/754A/758A which will subsequently return to the idle state. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation.

4.3 Acknowledge (ACK)

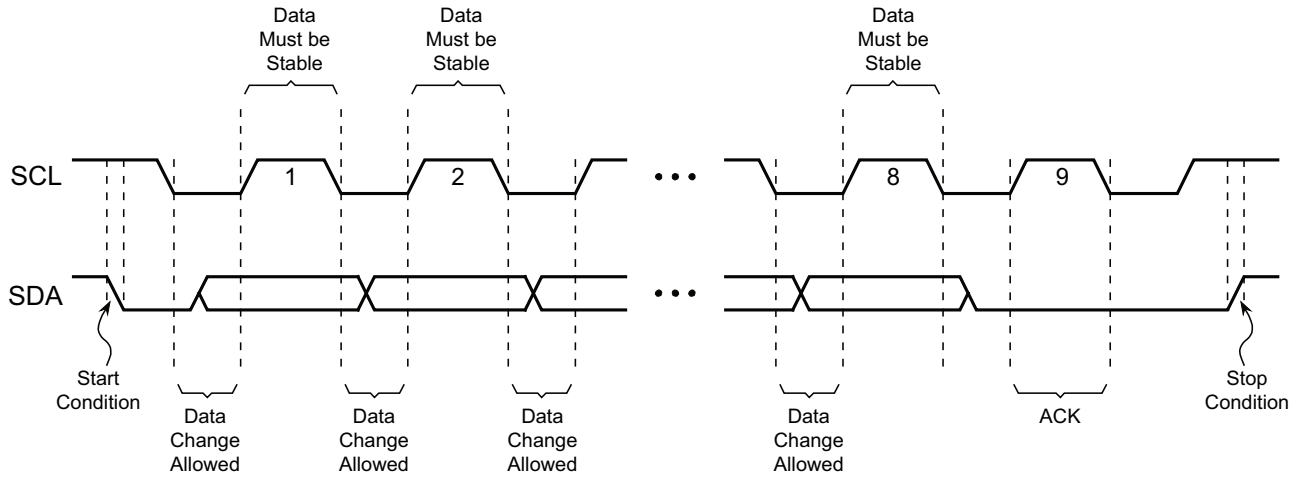
After every byte of data received, the AT30TSE752A/754A/758A must acknowledge to the Master that it has successfully received the data byte by responding with an ACK. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the AT30TSE752A/754A/758A must output a Logic 0 (ACK) for the entire clock cycle such that the SDA line must be stable in the logic-low state during the entire high period of the clock cycle.

4.4 No-Acknowledge (NACK)

When the AT30TSE752A/754A/758A are transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the AT30TSE752A/754A/758A instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the AT30TSE752A/754A/758A will release the SDA line so that the Master can then generate a Stop condition.

In addition, the AT30TSE752A/754A/758A can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to write to a Read-only Register (e.g. an attempt to write to the Temperature Register).

Figure 4-1. Start, Stop, and ACK



5. Device Operation

Commands used to configure and control the operation of the AT30TSE752A/754A/758A are sent to the device from the Master via the serial interface. Likewise, the Master can read the temperature data from the AT30TSE752A/754A/758A via the serial interface; however, since multiple slave devices can reside on the serial bus, each slave device must have its own unique 7-bit address so that the Master can access each device independently.

For the AT30TSE752A/754A/758A, the first four MSBs of its 7-bit address are the device type identifier and are fixed at 1001 for temperature sensor and 1010 for Serial EEPROM. The remaining three LSBs correspond to the states of the hard-wired A_{2-0} address pins.

Example: If the A_{2-0} pins are connected to GND, then the 7-bit device address would be 1001000 or 1010000.

In order for the Master to select and access the AT30TSE752A/754A/758A, the Master must first initiate a Start condition. Following the Start condition, the Master must output the device address byte. The device address byte consists of the 7-bit device address plus a Read/Write (R/$\overline{W}$) control bit, which indicates whether the Master will be performing a Read or a Write to the AT30TSE752A/754A/758A. If the R/$\overline{W}$ control bit is a Logic 1, then the Master will be reading data from the AT30TSE752A/754A/758A. Alternatively, if the R/$\overline{W}$ control bit is a Logic 0, then the Master will be writing data to the AT30TSE752A/754A/758A.

Table 5-1. AT30TSE752A/754A/758A Address Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Function	Device Type Identifier				Device Address			Read/Write
Temp Sensor	1	0	0	1	A2	A1	A0	R/$\overline{W}$
Serial EEPROM	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Software Write Protection[1]	0	1	1	0	A2	A1	A0	R/$\overline{W}$

Note: 1. See Section 10.5, “Software Write Protect” on page 40 for more information.

If the 7-bit address sent by the Master matches that of the AT30TSE752A/754A/758A, then the device will respond with an ACK after it has received the full address byte. If there is an address mismatch, then the AT30TSE752A/754A/758A will respond with a NACK and return to the idle state.

5.1 Temperature Measurements

The AT30TSE752A/754A/758A utilizes a band-gap type temperature sensor with an internal sigma-delta Analog-to-Digital Converter (ADC) to measure and convert the temperature reading into a digital value with a selectable resolution as high as 0.0625°C. The measured temperature is calibrated in degrees Celsius; therefore, a lookup table or conversion routine is necessary for applications that wish to deal in degrees Fahrenheit.

The result of the digitized temperature measurements are stored in the internal Temperature Register of the AT30TSE752A/754A/758A, which is readable at any time through the device's serial interface. When in the normal operating mode, the device performs continuous temperature measurements and updates the contents of the Temperature Register (see Section 6.2, “Temperature Register” on page 17) after each analog-to-digital conversion.

The resolution of the temperature measurement data can be configured to 9, 10, 11, or 12 bits which corresponds to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. Selecting the temperature resolution is done by setting the R1 and R0 bits in the Configuration Register (see Section 6.3, “Configuration Register” on page 19). The ADC conversion time does increase with each bit of higher resolution, so careful consideration should be given to the resolution versus conversion time relationship. The resolution after device power-up or reset will revert to what was previously selected using the NVR1 and NVR0 bits of the Nonvolatile Configuration Register bits prior to when the device was powered-down or reset.

With 12 bits of resolution, the AT30TSE752A/754A/758A can theoretically measure a temperature range of 255°C (-128°C to +127°C); however, the device is only designed to measure temperatures over a range of -55°C to +125°C.

5.2 Temperature Alarm

After the measured temperature value has been stored into the Temperature Register, the data will be compared with both the high and low temperature limits defined by the values stored in the T_{HIGH} Limit Register and T_{LOW} Limit Register. If the comparison results in a valid fault condition (see Section 5.2.1, “Fault Tolerance Limits” on page 11), then the device will activate the ALERT output pin.

The polarity and function of the ALERT pin can be configured by using specific bits in the Configuration Register. The polarity of the ALERT pin is controlled by the POL bit in the Configuration Register while the function of the ALERT pin changes based on the Alarm Thermostat mode, which can be configured to either Comparator mode (see Section 5.2.2, “Comparator Mode” on page 12) or Interrupt mode (see Section 5.2.3, “Interrupt Mode” on page 13) by using the CMP/INT bit in the Configuration Register. After the device powers up or resets, the NVPOL and NVCMP/INT bits of the Nonvolatile Configuration Register are automatically copied into the POL and CMP/INT bits of the Configuration Register; therefore, the ALERT pin polarity and function will revert back to the settings defined by the NVPOL and NVCMP/INT bits prior to when the device was powered-down or reset.

The value of the high temperature limit stored in the T_{HIGH} Limit Register must be greater than the value of the low temperature limit stored in the T_{LOW} Limit Register in order for the ALERT function to work properly; otherwise, the ALERT pin will output erroneous results and will falsely signal temperature alarms.

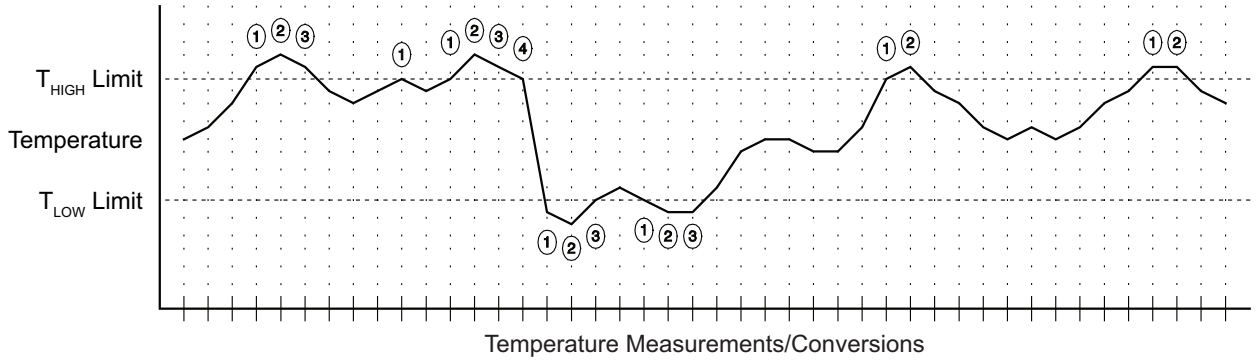
5.2.1 Fault Tolerance Limits

A temperature fault occurs if the measured temperature meets or exceeds either the high temperature limit set by the T_{HIGH} Limit Register or the low temperature limit set by the T_{LOW} Limit Register. To prevent false alarms due to environmental or temperature noise, the device incorporates a fault tolerance queue that requires consecutive temperature faults to occur before resulting in a valid fault condition. The fault tolerance queue value is controlled by the FT1 and FT0 bits in the Configuration Register and can be set to a single fault count of one or a count of two, four, or six consecutive faults.

An internal counter that automatically increments after a temperature fault is used to determine if the fault tolerance queue setting has been met. After incrementing the fault counter, the device will compare the count to the fault tolerance queue setting to see if a valid fault condition should be triggered. Once a valid fault condition occurs, the device will activate the ALERT output pin. If the most recent measured temperature does not meet or exceed the high or low temperature limit, then the internal fault counter will be reset back to zero.

Figure 5-1 shows a sample temperature profile and how each temperature fault would impact the internal fault counter.

Figure 5-1. Fault Count Example



After the device powers up or resets, the NVFT1 and NVFT0 bits of the Nonvolatile Configuration Register are automatically copied into the FT1 and FT0 bits of the Configuration Register; therefore, the Fault Tolerance Queue setting will revert back to the settings defined by the NVFT1 and NVFT0 bits prior to when the device was powered-down or reset.

5.2.2 Comparator Mode

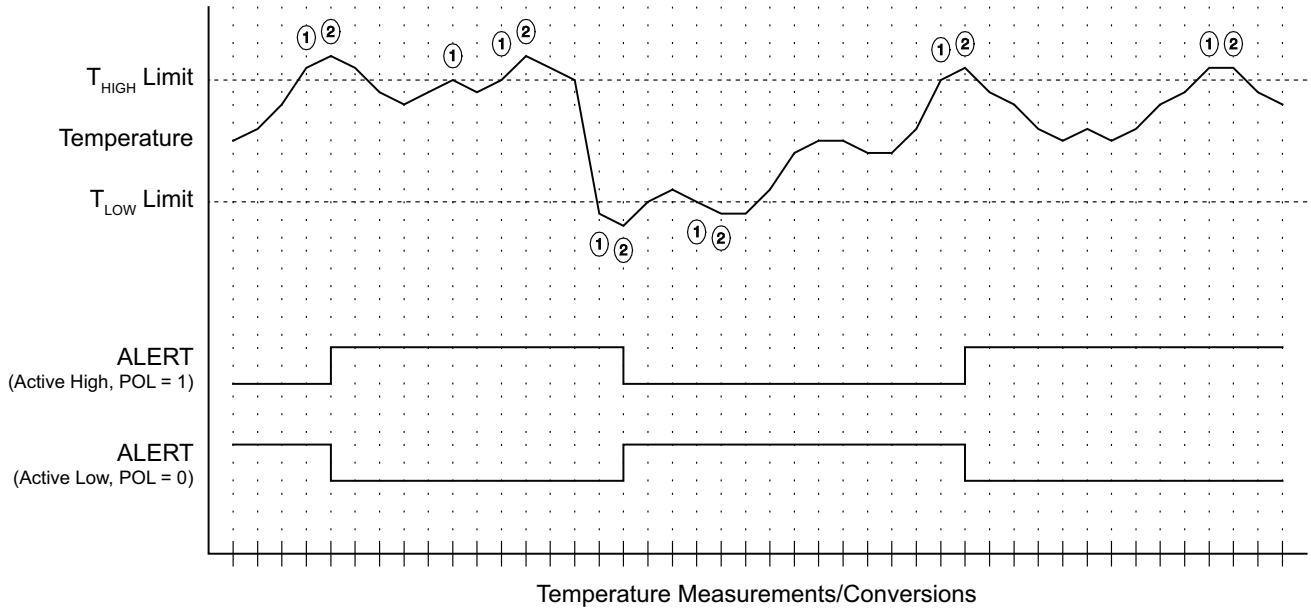
When the device operates in the Comparator mode, then the ALERT pin goes active if the measured temperature meets or exceeds the high temperature limit set by the T_{HIGH} Limit Register and a valid fault condition exists (the consecutive number of temperature faults has been reached). The ALERT pin will return to the inactive state after the measured temperature drops below the T_{LOW} Limit Register value the appropriate number of times to create a subsequent valid fault condition. The ALERT pin only changes state based on the high and low temperature limits and fault conditions; reading from or writing to any register or putting the device into Shutdown mode will not affect the state of the ALERT pin. The high temperature limit set by the T_{HIGH} Limit Register must be greater than the low temperature limit set by the T_{LOW} Limit Register in order for the ALERT pin to activate correctly.

If switching from Interrupt mode to Comparator mode while the ALERT pin is already active, then the ALERT pin will remain active until the measured temperature is below the T_{LOW} Limit Register value the appropriate number of times to create a valid fault condition.

The ALERT pin will return to the inactive state if the device receives the General Call Reset command. When reset, the contents of the Nonvolatile Configuration Register will be copied into the Configuration Register; therefore, the device may or may not return to the Comparator mode depending on the setting of the NVCMP/INT bit in the Nonvolatile Configuration Register.

Figure 5-2 illustrates both the active high and active low ALERT pin response for a sample temperature profile with the device configured for the Comparator mode and a fault tolerance queue setting of two.

Figure 5-2. Comparator Mode (Fault Tolerance Queue = 2)



5.2.3 Interrupt Mode

Similar to the Comparator mode, when the device operates in the Interrupt mode, the ALERT pin will go active if the measured temperature meets or exceeds the high temperature limit set by the T_{HIGH} Limit Register and a valid fault condition exists (the consecutive number of temperature faults has been reached). Unlike the Comparator mode, however, the ALERT pin will remain active until one of three normal operation events takes place: any one of the device's registers is read, the device responds to an SMBus Alert Response Address (ARA), or the device is put into Shutdown mode.

Once the ALERT pin returns to the inactive state, it will not go active again until the measured temperature drops below the low temperature limit set by the T_{LOW} Limit Register for the appropriate number of consecutive faults. Again, the ALERT pin will remain active until one of the device's registers is read, the device responds to an SMBus ARA, or the device is placed into the Shutdown mode.

After the ALERT pin becomes inactive again, the cycle will repeat itself with the ALERT pin going active after the measured temperature meets or exceeds the T_{HIGH} Limit Register value for the proper number of consecutive faults. This process is cyclical between T_{HIGH} and T_{LOW} temperature alarms (e.g. T_{HIGH} event, ALERT clear, T_{LOW} event, ALERT clear, T_{HIGH} event, ALERT clear, T_{LOW} event, etc.).

In order for the ALERT pin to normally become active for the first time in the Interrupt Mode, the first event must be a T_{HIGH} temperature alarm event; therefore, even if the measured temperature initially starts off between the T_{HIGH} and T_{LOW} limits and then drops below the T_{LOW} temperature limit and has met valid fault conditions, the ALERT pin will still not go active. The high temperature limit set by the T_{HIGH} Limit Register must be greater than the low temperature limit set by the T_{LOW} Limit Register in order for the ALERT pin to activate correctly.

If switching from Comparator mode to Interrupt Mode while the ALERT pin is already active, then the ALERT pin will remain active until it is cleared by one of the events already detailed: any one of the device's registers is read, the device responds to an SMBus Alert Response Address (ARA), or the device is put into Shutdown Mode. The ALERT pin will also return to the inactive state if the device receives the General Call Reset command. When reset, the contents of the Nonvolatile Configuration Register will be copied into the Configuration Register; therefore, the device may or may not return to the Interrupt mode depending on the setting of the NVCMP/INT bit in the Nonvolatile Configuration Register.

Figures 5-3 and Figure 5-4 show both the active high and active low ALERT pin response for a sample temperature profile with the device configured for the Interrupt mode and a fault tolerance queue setting of two. Figure 5-4 illustrates how the ALERT pin output would look if there was a longer delay between the ALERT trigger and the reading of a register.

Figure 5-3. Interrupt Mode (Fault Tolerance Queue = 2)

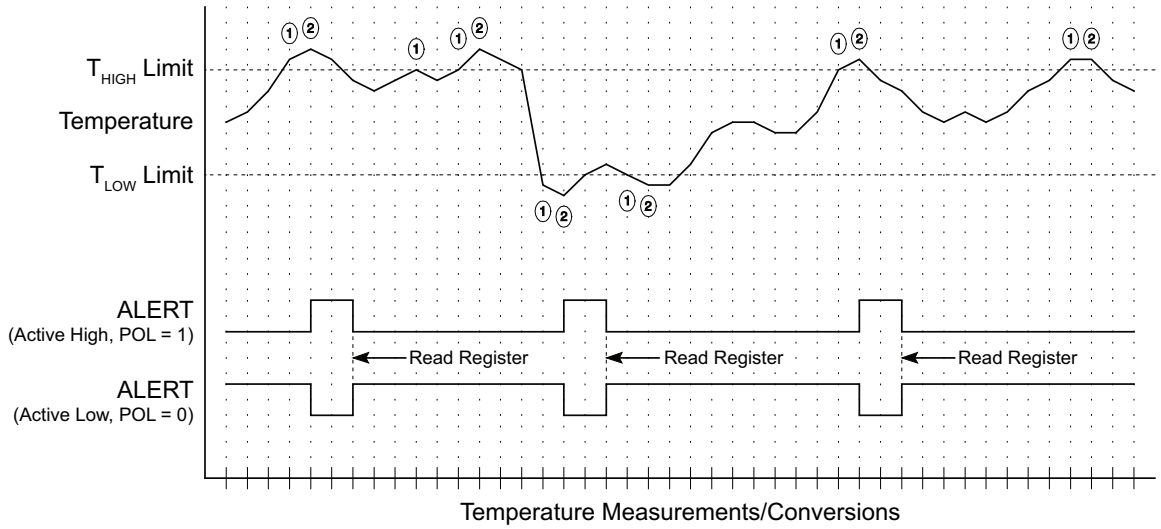
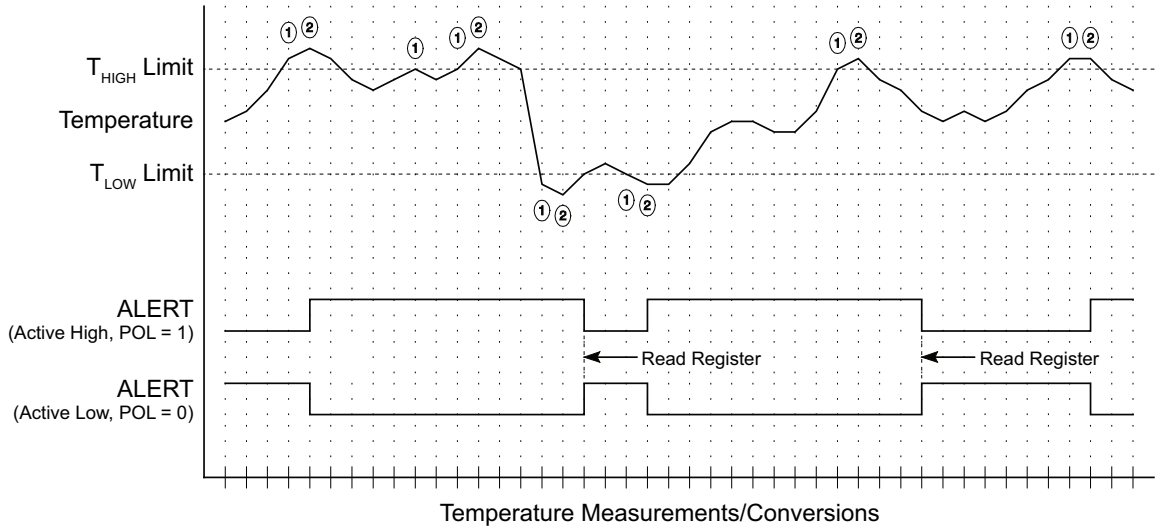


Figure 5-4. Interrupt Mode (Fault Tolerance Queue = 2) Delay Before Reading Register



5.3 Shutdown Mode

To reduce current consumption and save power, the device features a Shutdown mode that disables all internal device circuitry except for the serial interface and POR circuits. While in the Shutdown mode, the internal temperature sensor is not active, so no temperature measurements will be made. Entering and exiting the Shutdown mode is controlled by the SD bit in the Configuration Register.

Entering the Shutdown mode can affect the ALERT pin depending on the Alarm Thermostat mode. If the device is configured to operate in the Interrupt mode, then the ALERT pin will go inactive when the device enters the Shutdown mode; however, the ALERT pin will not change states if the device is operating in the Comparator mode.

The fault count information will not change when the device enters or exits the Shutdown mode; therefore, the number of previous temperature faults recorded by the internal fault counter will be retained unless the device is power-cycled or reset. When exiting the Shutdown mode, the ALERT pin will go active if operating in Interrupt mode, a valid fault condition exists, and the T_{HIGH} and T_{LOW} event cycles are maintained (i.e. T_{HIGH} event before entering Shutdown mode followed by a T_{LOW} event when exiting Shutdown mode).

The device can be powered-down while in the Shutdown mode so that it will remain in the Shutdown mode after the subsequent Power-up operation. This is accomplished by setting the NVSD bit in the Nonvolatile Configuration Register to the Logic 1 state prior to power-down. Upon power-up or reset, the device will first copy the contents of the Nonvolatile Data Registers into the Volatile Data Registers, after which the device will perform a single temperature measurement and store the result in the Temperature Register. After this process is complete, the device will re-enter the Shutdown mode.

5.3.1 One-Shot Mode

The AT30TSE752A/754A/758A features a One-Shot Temperature mode that allows the device to perform a single temperature measurement while in the Shutdown mode. By keeping the device in the Shutdown mode and utilizing the One-Shot mode, the AT30TSE752A/754A/758A can remain in a lower power state and only go active to take temperature measurements on an as-needed basis. The internal fault counter will be updated when taking a temperature measurement using the One-Shot mode; therefore, a valid fault condition can be generated by the One-Shot temperature measurements. If operating in Comparator mode, then the fault condition will cause the ALERT pin to go either active or inactive depending on if the fault condition is a result of a T_{HIGH} or T_{LOW} event. If operating in Interrupt mode, the fault condition will cause the ALERT pin to pulse active for a short duration of time to indicate a T_{HIGH} or T_{LOW} event has occurred. The ALERT pin will then return to the inactive state.

The One-Shot mode is controlled using the OS bit in the Configuration Register (see Section 6.3.1, “OS Bit” on page 20).

6. Registers

The AT30TSE752A/754A/758A contains eight registers (a Pointer Register and seven data registers) that are used to control the operational mode and performance of the temperature sensor, store the user-defined high and low temperature limits, and store the digitized temperature measurements. All accesses to the device are performed using these eight registers. In order to read from and write to one of the device's seven data registers, the user must first select a desired data register by utilizing the Pointer Register.

The device incorporates both volatile and nonvolatile versions of the Configuration Register, the T_{LOW} Limit Register, and the T_{HIGH} Limit Register. Upon device power-up or reset, the AT30TSE752A/754A/758A will copy the contents of the Nonvolatile Data Registers into the Volatile Data Registers. Both the volatile and Nonvolatile Data Registers can be modified separately provided that the registers are not locked or locked down; however, all temperature sensor related operations, such as responses to high and low temperature conditions, are based on the settings stored in the volatile versions of the registers only. Therefore, if the Nonvolatile Data Registers are updated with new values, then the contents of the Nonvolatile Data Registers should be copied to the Volatile Data Registers (see Section 9.1, “Copy Nonvolatile Registers to Volatile Registers” on page 34)

Table 6-1. Registers

Register	Address	Read/ Write	Size	Power-on Default	Factory Default
Pointer Register	n/a	W	8-bit	00h	n/a
Temperature Register	00h	R	16-bit	0000h	n/a
Configuration Register	01h	R/W	16-bit	Copy of Nonvolatile Configuration Register	n/a
T_{LOW} Limit Register	02h	R/W	16-bit	Copy of Nonvolatile T_{LOW} Limit Register	n/a
T_{HIGH} Limit Register	03h	R/W	16-bit	Copy of Nonvolatile T_{HIGH} Limit Register	n/a
Nonvolatile Configuration Register	11h	R/W	16-bit	Last Programmed State	0000h
Nonvolatile T_{LOW} Limit Register	12h	R/W	16-bit	Last Programmed State	4B00h (75°C)
Nonvolatile T_{HIGH} Limit Register	13h	R/W	16-bit	Last Programmed State	5000h (80°C)

The Configuration Register, despite being 16-bits wide, is compatible to industry standard LM75-type temperature sensors that use an 8-bit wide register in that only the first 8-bits of the Configuration Register need to be written to or read from.

6.1 Pointer Register

The 8-bit Write-only Pointer Register is used to address and select which one of the device's seven data registers (Temperature Register, Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, or Nonvolatile T_{HIGH} Limit Register) will be read from or written to.

For Read operations from the AT30TSE752A/754A/758A, once the Pointer Register is set to point to a particular data register, it remains pointed to that same data register until the Pointer Register value is changed.

Example: If the user sets the Pointer Register to point to the Temperature Register, then all subsequent reads from the device will output data from the Temperature Register until the Pointer Register value is changed.

For Write operations to the AT30TSE752A/754A/758A, the Pointer Register value must be refreshed each time a Write to the device is to be performed, even if the same data register is going to be written to a second time in a row.

Example: If the Pointer Register is set to point to the Configuration Register, once the subsequent Write operation to the Configuration Register has completed, the user cannot write again into the Configuration Register without first setting the Pointer Register value again. As long as a Write operation is to be performed, the device will assume that the Pointer Register value is the first data byte received after the address byte.

Since only seven data registers are available for access, only the five LSBs (P4-P0) of the Pointer Register are used; the remaining three bits (P7-P5) of the Pointer Register should always be set to zero to allow for future migration paths to other temperature sensor devices that have more than seven data registers. In addition, the device incorporates additional commands that are decoded in lieu of the Pointer Register byte; therefore, if bits P7-P5 are not set as zero when setting the value of the Pointer Register byte, the device may interpret the data as one of the additional commands. Table 6-2 shows the bit assignments of the Pointer Register and the associated pointer addresses of the data registers available. Attempts to write any values other than those listed in Table 6-2 into the Pointer Register will be ignored by the device, and the contents of the Pointer Register will not be changed. The device will respond back to the Master with a NACK to indicate that the device received an invalid Pointer Register byte.

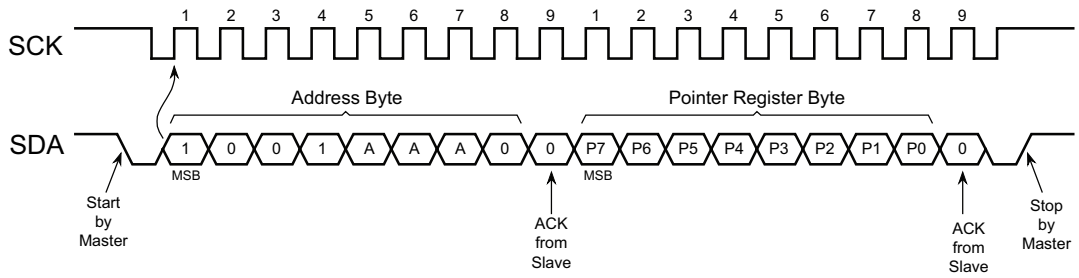
Table 6-2. Pointer Register and Address Assignments

Pointer Register Value								Associated Address	Register Selected
P7	P6	P5	P4	P3	P2	P1	P0		
0	0	0	0	0	0	0	0	00h	Temperature Register
0	0	0	0	0	0	0	1	01h	Configuration Register
0	0	0	0	0	0	1	0	02h	T_{LOW} Limit Register
0	0	0	0	0	0	1	1	03h	T_{HIGH} Limit Register
0	0	0	1	0	0	0	1	11h	Nonvolatile Configuration Register
0	0	0	1	0	0	1	0	12h	Nonvolatile T_{LOW} Limit Register
0	0	0	1	0	0	1	1	13h	Nonvolatile T_{HIGH} Limit Register

To set the value of the Pointer Register, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate data byte to the AT30TSE752A/754A/758A to set the value of the Pointer Register.

After device power-up or reset, the Pointer Register defaults to 00h which is the Temperature Register location; therefore, the Temperature Register can be read from immediately after device power-up or reset without having to set the Pointer Register. If the device is configured to power-up in the Shutdown mode, then the device will make a single temperature measurement immediately after power-up so that valid temperature data can be output from the Temperature Register.

Figure 6-1. Write Pointer Register



6.2 Temperature Register

The Temperature Register is a 16-bit Read-only Register that stores the digitized value of the most recent temperature measurement. The temperature data value is represented in the twos complement format, and, depending on the resolution selected, up to 12 bits of data will be available for output with the remaining LSBs being fixed in the Logic 0 state. The Temperature Register can be read at any time, and since temperature measurements are performed in the background, reading the Temperature Register does not affect any other operation that may be in progress.

The MSB (bit 15) of the Temperature Register contains the sign bit of the measured temperature value with a zero indicating a positive number and a one indicating a negative number. The remaining MSBs of the Temperature Register contain the temperature value in the twos complement format. Table 6-3 details the Temperature Register format for the different selectable resolutions, and Table 6-4 shows some examples for 12-bit resolution Temperature Register data values and the associated temperature readings.

Table 6-3. Temperature Register Format

Resolution	Upper Byte								Lower Byte							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0
11 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0
10 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0
9 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0	0

Note: TD = Temperature Data

Table 6-4. 12-bit Resolution Temperature Data/Values Examples

Temperature	Temperature Register Data	
	Binary Value	Hex Value
+125°C	0111 1101 0000 0000	7D00h
+100°C	0110 0100 0000 0000	6400h
+75°C	0100 1011 0000 0000	4B00h
+50.5°C	0011 0010 1000 0000	3280h
+25.25°C	0001 1001 0100 0000	1940h
+10.125°C	0000 1010 0010 0000	0A20h
+0.0625°C	0000 0000 0001 0000	0010h
0°C	0000 0000 0000 0000	0000h
-0.0625°C	1111 1111 1111 0000	FFF0h
-10.125°C	1111 0101 1110 0000	F5E0h
-25.25°C	1110 0110 1100 0000	E6C0h
-50.5°C	1100 1101 1000 0000	CD80h
-55°C	1100 1001 0000 0000	C900h

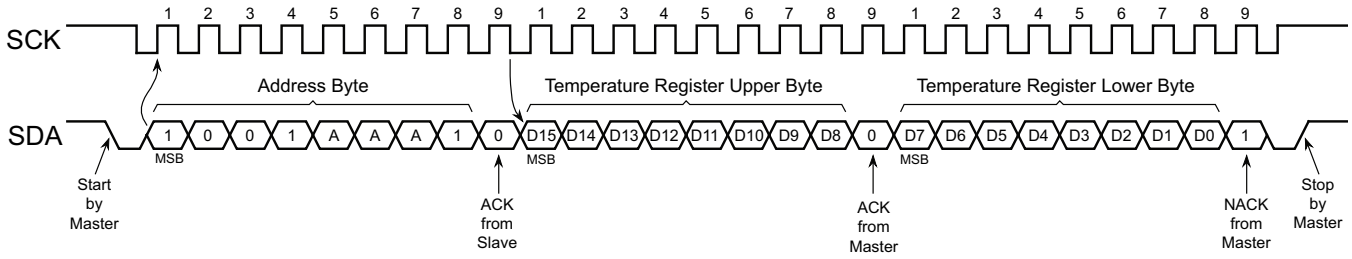
After each temperature measurement and digital conversion is complete, the new temperature data is loaded into the Temperature Register if the register is not currently being read. If a Read is in progress, then the previous temperature data will be output. Accessing the Temperature Register continuously without waiting the maximum conversion time (t_{CONV}) for the selected resolution may prevent the device from properly updating the Temperature Register with new temperature data.

In order to read the most recent temperature measurement data, the Pointer Register must be set or have been previously set to 00h. If the Pointer Register has already been set to 00h, the Temperature Register can be read by having the Master first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA1 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master can then read the upper byte of the Temperature Register. After the upper byte of the Temperature Register has been clocked out of the AT30TSE752A/754A/758A, the Master must send an ACK to indicate that it is ready for the lower byte of the temperature data. The AT30TSE752A/754A/758A will then clock out the lower byte of the Temperature Register, after which the Master must send a NACK to end the operation. When the AT30TSE752A/754A/758A receives the NACK, it will release the SDA line so that the Master can send a Stop or repeated Start condition. If the Master does not send a NACK but instead sends an ACK after the lower byte of the Temperature Register has been clocked out, then the device will repeat the sequence by outputting new temperature data starting with the upper byte of the Temperature Register.

If 8-bit temperature resolution is satisfactory, then the lower byte of the Temperature Register does not need to be read. In this case, the Master would send a NACK instead of an ACK after the upper byte of the Temperature Register has been clocked out of the AT30TSE752A/754A/758A. When the AT30TSE752A/754A/758A receives the NACK, the device will know that it should not send out the lower byte of the Temperature Register and will instead release the SDA line so the Master can send a Stop or repeated Start condition.

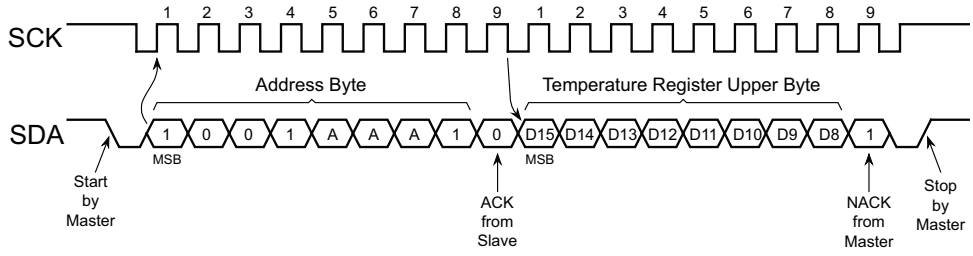
The Temperature Register defaults to 0000h after device power-up or reset; therefore, the system should wait the maximum conversion time (t_{CONV}) for the selected resolution before attempting to read valid temperature data. If the device is configured to power-up in the Shutdown mode, then the device will make a single temperature measurement immediately after power-up so that valid temperature data can be output from the Temperature Register after the maximum t_{CONV} time. Since the Temperature Register is a Read-only Register, any attempts to write to the register will be ignored, and the device will subsequently respond by sending a NACK back to the Master for any data bytes that are sent.

Figure 6-2. Read Temperature Register — 16 Bits



Note: Assumes the Pointer Register was previously set to point to the Temperature Register.

Figure 6-3. Read Temperature Register — 8 Bits



Note: Assumes the Pointer Register was previously set to point to the Temperature Register.

6.3 Configuration Register

The Configuration Register is used to control key operational modes and settings of the device such as the One-Shot mode, the temperature conversion resolution, the fault tolerance queue, the ALERT pin polarity, the Alarm Thermostat mode, and the Shutdown mode. The Configuration Register is a 16-bit wide Read/Write Register; however, only the first 8-bits of the register are actually used while the least-significant 8-bits are reserved for future use to provide an upward migration path to other temperature sensor devices that have enhanced features. Since only the most-significant 8-bits of the Configuration Register are used, the device is backwards compatible to industry standard LM75-type temperature sensors that use 8-bit wide registers.

After device power-up or reset, the contents of the most-significant byte (bits 15 through 8) of the Nonvolatile Configuration Register will always be automatically copied into the Configuration Register. Therefore, the Configuration Register settings will match the settings of the Nonvolatile Configuration Register prior to when the device was powered-down or reset. Since the Configuration Register value will always be copied from the Nonvolatile Configuration Register, the Configuration Register can be temporarily changed without affecting subsequent power-up/reset settings. If it is desired for the new Configuration Register settings to become the new power-up/reset settings, then the contents of the Configuration Register can be copied into the most-significant byte of the Nonvolatile Configuration Register by using the copy Volatile Registers to Nonvolatile Registers command (see Section 9.2, “Copy Volatile Registers to Nonvolatile Registers” on page 35). Please note that when using the copy Volatile Registers to Nonvolatile Registers command, the contents of the T_{HIGH} and T_{LOW} Limit Registers will also be copied into the nonvolatile T_{HIGH} and T_{LOW} Limit Registers.

Table 6-5. Configuration Register

Bit	Name		Type	Description	
15	OS	One-Shot Mode	R/W	0	Normal Operation (Default)
				1	Perform One-Shot Measurement (Valid in Shutdown Mode Only)
14:13	R1:R0	Conversion Resolution	R/W	00	9-bits (Default)
				01	10-bits
				10	11-bits
				11	12-bits
12:11	FT1:FT0	Fault Tolerance Queue	R/W	00	Alarm after 1 Fault (Default)
				01	Alarm after 2 Consecutive Faults
				10	Alarm after 4 Consecutive Faults
				11	Alarm after 6 Consecutive Faults
10	POL	ALERT Pin Polarity	R/W	0	ALERT Pin is Active Low (Default)
				1	ALERT Pin is Active High
9	CMP/INT	Alarm Thermostat Mode	R/W	0	Comparator Mode (Default)
				1	Interrupt Mode
8	SD	Shutdown Mode	R/W	0	Temperature Sensor Performing Active Measurements (Default)
				1	Temperature Sensor Disabled and Device In Shutdown Mode
7:1	*RFU*	*Reserved for Future Use*	R	0	Reserved for Future Use
0	NVRBSY	Nonvolatile Registers Busy	R	0	Nonvolatile Registers are ready for access.
				1	Nonvolatile Registers are busy and cannot be read from or written to.

To set the value of the Configuration Register, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 01h to select the Configuration Register. After the Pointer Register byte of 01h has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After receiving the ACK from the AT30TSE752A/754A/758A, the Master must then send the appropriate data byte to the AT30TSE752A/754A/758A to set the value of the Configuration Register. Only the first data byte sent to the AT30TSE752A/754A/758A will be recognized as valid data; any subsequent bytes received by the device will simply be ignored. If the Master does not send a complete byte of Configuration Register data prior to issuing a Stop or repeated Start condition, then the AT30TSE752A/754A/758A will ignore the data and the contents of the Configuration Register will be unchanged.

In addition to the Master not sending a complete byte of Configuration Register data, writing to the Configuration Register will be ignored and no operation will be performed if the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state) or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state); however, the device will still respond with an ACK to indicate that it received the proper data byte even though the contents of the Configuration Register will not be changed.

Updating the Configuration Register, whether actually changing the Fault Tolerance Queue setting or not, will clear the internal fault counter and reset the count back to zero.

6.3.1 OS Bit

The OS bit is used to enable the One-Shot Temperature Measurement mode. When a Logic 1 is written to the OS bit while the AT30TSE752A/754A/758A is in the Shutdown mode, the device will become active and perform a single temperature measurement and conversion. After the Temperature Register has been updated with the measured temperature data, the device will return to the low-power Shutdown mode and clear the OS bit.

Writing a one to the OS bit when the device is not in the Shutdown mode will have no effect. When reading the Configuration Register, the OS bit will always be read as a Logic 0.

6.3.2 R1:R0 Bits

The R1 and R0 bits are used to select the conversion resolution of the internal sigma-delta ADC. Four possible resolutions can be set to maximize for either higher resolution or faster conversion times. The R1 and R0 bits will be copied from the NVR1 and NVR0 in the Nonvolatile Configuration Register after device power-up or reset, allowing the device to retain the conversion resolution that was previously set by the Nonvolatile Configuration Register prior to power-down or reset.

Table 6-6. Conversion Resolution

R1	R0	Conversion Resolution		Conversion Time
0	0	9 bits	0.5°C	25ms
0	1	10 bits	0.25°C	50ms
1	0	11 bits	0.125°C	100ms
1	1	12 bits	0.0625°C	200ms

6.3.3 FT1:FT0 Bits

The FT1 and FT0 bits are used to set the fault tolerance queue value which defines how many consecutive faults must occur before the ALERT pin will be activated (see Section 5.2.1, “Fault Tolerance Limits” on page 11). The FT1 and FT0 bit settings provide four different fault values as detailed in Table 6-7. After the device powers up or resets, the FT1 and FT0 bits will be copied from the NVFT1 and NVFT0 in the Nonvolatile Configuration Register; therefore, the fault tolerance queue value will default to whatever value was previously stored in the Nonvolatile Configuration Register prior to Configuration Register power-down or reset.

Table 6-7. Fault Tolerance Queue

FT1	FT0	Consecutive Faults Required
0	0	1
0	1	2
1	0	4
1	1	6

6.3.4 POL Bit

The ALERT pin polarity is controlled by the POL bit. When the POL bit is in the Logic 0 state, the ALERT pin will be an active low output. To configure the ALERT pin as an active high output, the POL bit must be set to the Logic 1 state.

After the device powers up or resets, the POL bit will be copied from the NVPOL bit in the Nonvolatile Configuration Register; therefore, the polarity of the ALERT pin will default to the state defined by the Nonvolatile Configuration Register prior to power-down or reset.

6.3.5 CMP/INT Bit

The CMP/INT bit controls whether the device will operate in the Comparator mode or the Interrupt mode. Setting the CMP/INT bit to the Logic 0 state will put the device into the Comparator mode. Alternatively, when the CMP/INT bit is set to the Logic 1 state, then the device will operate in the Interrupt mode. The function of the ALERT pin changes based on the CMP/INT bit setting.

The CMP/INT bit will be copied from the NVCMP/INT bit in the Nonvolatile Configuration Register after the device powers up or resets. Since the CMP/INT bit is copied from the NVCMP/INT bit, the device will default to whatever mode was selected by the Nonvolatile Configuration Register prior to power-down or reset.

6.3.6 SD Bit

The SD bit is used to enable or disable the device's Shutdown mode. When the SD bit is in the Logic 0 state, the device will be in the normal operational mode and perform continuous temperature measurements and conversions. When the SD bit is set to the Logic 1 state, the device will finish the current temperature measurement and conversion and will store the result in the Temperature Register, after which the device will then enter the Shutdown mode.

Resetting the SD bit back to a Logic 0 will return the device to the normal operating mode.

After the device powers up or resets, the SD bit will be copied from the NVSD bit in the Nonvolatile Configuration Register; therefore, it is possible for the device to automatically enter the Shutdown mode after power-up or reset by setting the NVSD bit to the Logic 1 state prior to power-down or reset. See Section 5.3, “Shutdown Mode” on page 14 for more details.

6.3.7 NVRBSY

The Ready/Busy status of the Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register can be determined by reading the NVRBSY bit. When the NVRBSY bit is in the Logic 0 state, then the Nonvolatile Configuration and Limit Registers are available to be read from or written to. When the NVRBSY bit is in the Logic 1 state, the Nonvolatile Registers are busy and cannot be accessed for reading, writing, or copying. Attempting to read the Nonvolatile Registers while the registers are busy will result in erroneous data being output. Similarly, any attempts to write to one of the Nonvolatile Registers while the NVRBSY bit is in the Logic 1 state will result in the data being ignored. Both the copy Nonvolatile Registers to Volatile Registers and the copy Volatile Registers to Nonvolatile Registers commands will also be ignored when the NVRBSY bit is in the Logic 1 state. For more details and a complete list of commands that are and are not allowed while NVRBSY is in the Logic 1 state, see Section 8., “Operations Allowed During Nonvolatile Busy Status” on page 33.

Figure 6-4. Write to Configuration Register

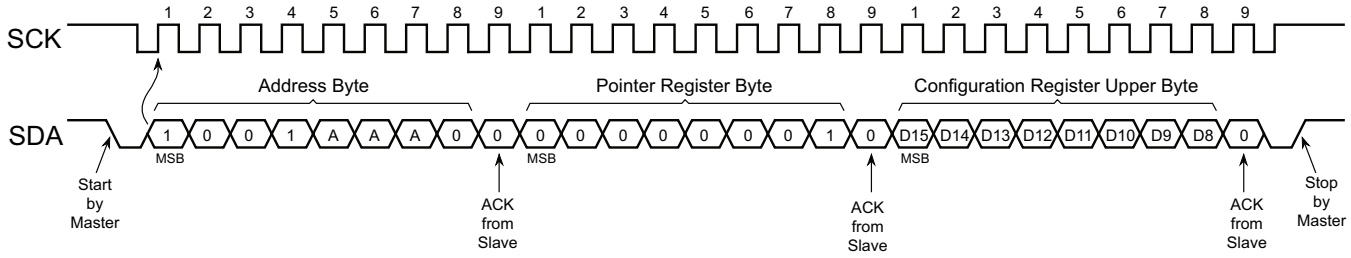
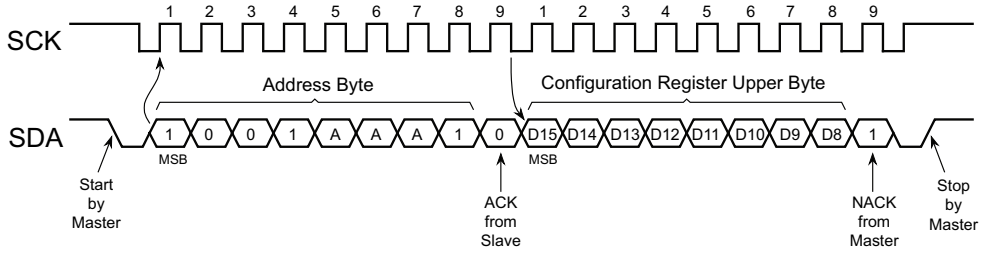


Figure 6-5. Read from Configuration Register



Note: Assumes the Pointer Register was previously set to point to the Configuration Register.

6.4 Nonvolatile Configuration Register

The Nonvolatile Configuration Register is a 16-bit wide Read/Write Register used to manage key power-up/reset device settings and operational modes including the locking of the AT30TSE752A/754A/758A's various registers. The Nonvolatile Configuration Register is used in conjunction with the Configuration Register to control how the device operates. All bits in the Nonvolatile Configuration Register will retain their state even after the device has been powered down or reset. On every power up or reset sequence, the contents of the most-significant byte (bits 15 through 8) of the Nonvolatile Configuration Register will be copied into the Configuration Register, after which all device operations and settings will then be controlled by the Configuration Register. By utilizing the Nonvolatile Configuration Register, the device can power-up or reset in a pre-defined, user-selected operating mode (e.g. Comparator mode, Shutdown mode, etc.) with pre-defined settings (e.g. 12-bit resolution, ALERT pin active high, etc.). Therefore, unlike standard LM75-type temperature sensors, there is no need to update the Configuration Register settings after every power-up or reset.

Since the Nonvolatile Configuration Register utilizes nonvolatile storage cells, care must be taken when updating the register to accommodate the aspects of an associated program time and finite program endurance limit. Power must not be removed from the device during the internally self-timed programming cycle of the register. If power is removed prior to the completion of the programming cycle, then the contents of the register cannot be guaranteed. In addition, the contents of the register may become corrupt if it is programmed more than the maximum allowed number of writes.

Table 6-8. Nonvolatile Configuration Register

Bit	Name		Type	Description	
15	*NU*	*Not Used*	*R*	0	*Not used*
14:13	NVR1:NVR0	Conversion Resolution	R/W	00	9-bits (Factory Default)
				01	10-bits
				10	11-bits
				11	12-bits
12:11	NVFT1:NVFT0	Fault Tolerance Queue	R/W	00	Alarm after 1 Fault (Factory Default)
				01	Alarm after 2 Consecutive Faults
				10	Alarm after 4 Consecutive Faults
				11	Alarm after 6 Consecutive Faults
10	NVPOL	ALERT Pin Polarity	R/W	0	ALERT Pin is Active Low (Factory Default)
				1	ALERT Pin is Active High
9	NVCMP/INT	Alarm Thermostat Mode	R/W	0	Comparator Mode (Factory Default)
				1	Interrupt Mode
8	NVSD	Shutdown Mode	R/W	0	Temperature Sensor Performing Active Measurements (Factory Default)
				1	Temperature Sensor Disabled and Device in Shutdown mode
7:3	*RFU*	*Reserved for Future Use*		0	*Reserved for Future Use*
2	RLCKDWN	Register Lockdown	R/W	0	All Configuration and Limit Registers are not locked down (Factory Default).
				1	All Configuration and Limit Registers are permanently locked down (ROM) and can never be modified again.
1	RLCK	Register Lock	R/W	0	All Configuration and limit registers are unlocked and can be modified (Factory Default).
				1	All Configuration and Limit Registers are locked and cannot be modified.
0	*RFU*	*Reserved for Future Use*	*R*	0	*Reserved for Future Use*

To set the value of the Nonvolatile Configuration Register, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 11h to select the Nonvolatile Configuration Register. After the Pointer Register byte of 11h has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After receiving the ACK from the AT30TSE752A/754A/758A, the Master must then send two data bytes to the AT30TSE752A/754A/758A to set the value of the Nonvolatile Configuration Register. Any subsequent bytes sent to the AT30TSE752A/754A/758A will simply be ignored by the device. If the Master does not send two complete bytes of Nonvolatile Configuration Register data prior to issuing a Stop or repeated Start condition, then the AT30TSE752A/754A/758A will ignore the data and the contents of the Nonvolatile Configuration Register will not be changed.

After the Master has issued a Stop or repeated Start condition, the AT30TSE752A/754A/758A will begin the internally self-timed program operation, and the contents of the Nonvolatile Configuration Register will be updated within a time of t_{PROG}. During this time, the NVRBSY bit in the Configuration Register will indicate that the device is busy. If the Master issues a repeated Start condition instead of a Stop condition, the AT30TSE752A/754A/758A will abort the operation and the contents of the Nonvolatile Configuration Register will not be changed.

In addition to the Master not sending two complete bytes of data, writing to the Nonvolatile Configuration Register will be ignored and no operation will be performed under the following conditions: the Nonvolatile Registers are already busy (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK, except in the case of the Nonvolatile Registers being busy, to indicate that it received the proper data bytes even though the program operation will not be performed. In the case of the Nonvolatile Registers being busy, the device will respond with an ACK to the address and pointer bytes but will then NACK when the data bytes are sent from the Master.

6.4.1 NVR1: NVR0 Bits

The nonvolatile NVR1 and NVR0 bits are used to select the power-up/reset default conversion resolution of the internal sigma-delta ADC. Four possible resolutions can be set to maximize for either higher resolution or faster conversion times. The NVR1 and NVR0 bits are set from the factory to default to the Logic 0 state to retain backwards compatibility to industry-standard LM75-type devices.

Table 6-9. Conversion Resolution

NVR1	NVR0	Conversion Resolution		Conversion Time
0	0	9 bits	0.5°C	25ms
0	1	10 bits	0.25°C	50ms
1	0	11 bits	0.125°C	100ms
1	1	12 bits	0.0625°C	200ms

6.4.2 NVFT1:NVFT0 Bits

The nonvolatile NVFT1 and NVFT0 bits are used to set the power-up/reset default Fault Tolerance Queue value which defines how many consecutive faults must occur before the ALERT pin will be activated (see Section 5.2.1, “Fault Tolerance Limits” on page 11). The NVFT1 and NVFT0 bit settings provide four different fault values as detailed in Table 6-10. Both the NVFT1 and NVFT0 bits are factory-set to default to the Logic 0 state.

Table 6-10. Fault Tolerance Queue

NVFT1	NVFT0	Consecutive Faults Required
0	0	1
0	1	2
1	0	4
1	1	6

6.4.3 NVPOL Bit

The nonvolatile NVPOL bit controls the power-up/reset default ALERT pin polarity. When the NVPOL bit is set to the Logic 0 state, the ALERT pin will be an active low output after the device powers up or resets. Conversely, when the NVPOL bit is set to the Logic 1 state, the ALERT pin will be an active high output. The NVPOL bit is set from the factory to default to the Logic 0 state.

6.4.4 NVCMP/INT Bit

The nonvolatile NVCMP/INT bit controls whether the device will operate in the Comparator mode or the Interrupt mode after a power-up or reset sequence. Setting the NVCMP/INT bit to the Logic 0 state (the factory default setting) will allow the device to power-up/reset in the Comparator mode. Alternatively, when the NVCMP/INT bit is set to the Logic 1 state, the device will power-up/reset in the Interrupt mode.

6.4.5 NVSD Bit

The nonvolatile NVSD bit is used to enable the device to power-up/reset in the Shutdown mode. When the NVSD bit is in the Logic 0 state, the device will power-up/reset in the normal operational mode and perform continuous temperature measurements and conversions. When the NVSD bit is set to the Logic 1 state, the device will automatically enter the Shutdown mode after a power-up or reset sequence (see Section 5.3, “Shutdown Mode” on page 14 for more details). The NVSD bit is factory-set to the Logic 0 state.

6.4.6 RLCKDWN

The one-time programmable RLCKDWN bit controls whether or not both the volatile and nonvolatile versions of the configuration and limit registers will be permanently locked down. Once the RLCKDWN bit is set to the Logic 1 state, the Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register will be locked down and can never be modified again. Since the RLCKDWN bit is one-time programmable, once the bit is set to the Logic 1 state, it cannot be reset again. The RLCKDWN bit takes priority over the RLCK bit (see Section 7., “Register Locking” on page 32 for more details) and is factory-set to the Logic 0 state.

6.4.7 RLCK

The nonvolatile RLCK bit controls the reversible locking of both the Volatile and Nonvolatile Configuration and Limit Registers. When the RLCK bit is set to the Logic 0 state, the Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register will be unlocked and can be modified. Alternatively, when the RLCK bit is set to the Logic 1 state, the Volatile and Nonvolatile Configuration and Limit Registers will be locked and cannot be modified. When the registers are locked, only the RLCK bit of the Nonvolatile Configuration Register can be altered and reset back to a Logic 0. Any attempts at changing other bits in the Nonvolatile Configuration Register will be ignored. The RLCK bit is set from the factory to default to the Logic 0 state. See Section 7., “Register Locking” on page 32 for more details.

Figure 6-6. Write to Nonvolatile Configuration Register

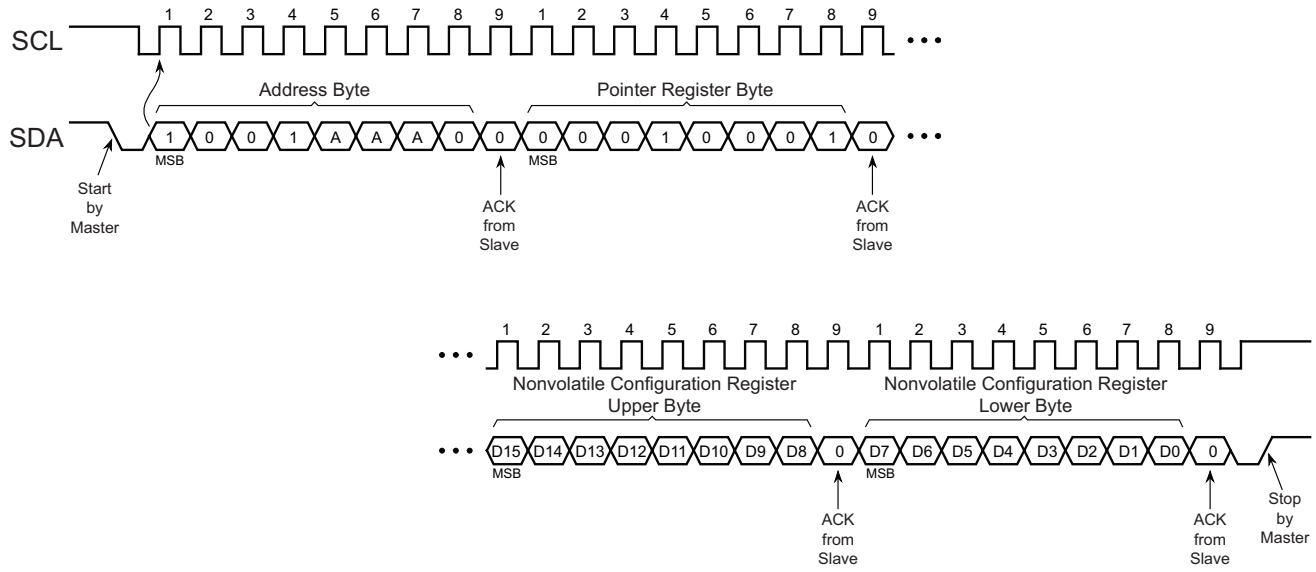
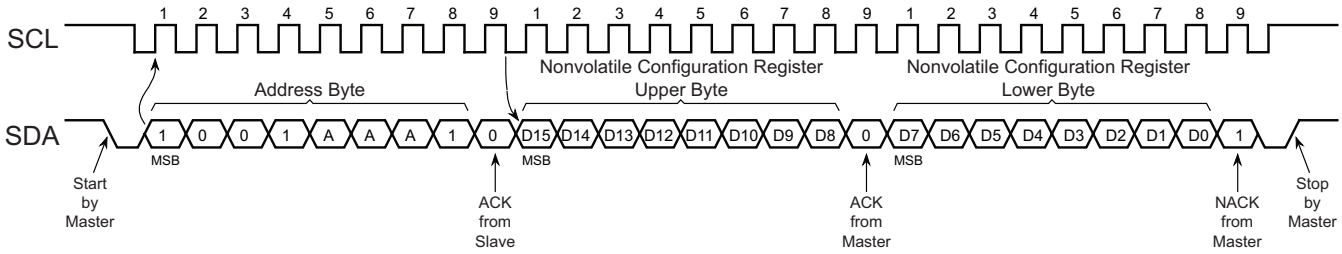


Figure 6-7. Read from Nonvolatile Configuration Register



Note: Assumes the Pointer Register was previously set to point to the Nonvolatile Configuration Register.

6.5 T_{LOW} and T_{HIGH} Limit Registers

The 16-bit T_{LOW} and T_{HIGH} Limit Registers store the user-programmable lower and upper temperature limits for the temperature alarm. Like the Temperature Register, the temperature data values of the T_{LOW} and T_{HIGH} Limit Registers are stored in the twos complement format with the MSB (bit 15) of the registers containing the sign bit (zero indicates a positive number and a one indicates a negative number).

As with the Temperature Register, the resolution selected by the R1 and R0 bits of the Configuration Register will determine how many bits of the T_{LOW} and T_{HIGH} Limit Registers will be used; therefore, when writing to the T_{LOW} and T_{HIGH} Limit Registers, up to 12 bits of data will be recognized by the device with the remaining LSBs being internally fixed to the Logic 0 state. Similarly, when reading from the registers, up to 12 bits of data will be output from the device with the remaining LSBs fixed in the Logic 0 state.

Table 6-11. T_{LOW} Limit Register and T_{HIGH} Limit Register Format

Resolution	Upper Byte								Lower Byte							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0
11 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0
10 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0
9 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0	0

Note: TD = Temperature Data

To set the value of either the T_{LOW} or T_{HIGH} Limit Register, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 02h to select the T_{LOW} Limit Register or 03h to select the T_{HIGH} Limit Register. After the Pointer Register byte has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After receiving the ACK from the AT30TSE752A/754A/758A, the Master must then send two data bytes to the AT30TSE752A/754A/758A to set the value of the T_{LOW} or T_{HIGH} Limit Register. Any subsequent bytes sent to the AT30TSE752A/754A/758A will simply be ignored by the device. If the Master does not send two complete bytes of data prior to issuing a Stop or repeated Start condition, then the AT30TSE752A/754A/758A will ignore the data and the contents of the register will not be changed.

In addition to the Master not sending two complete bytes of data, writing to the T_{LOW} or T_{HIGH} Limit Register will be ignored and no operation will be performed under the following conditions: the Nonvolatile Registers are busy because of a copy operation (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK, except in the case of the Nonvolatile Registers being busy, to indicate that it received the proper data bytes even though the contents of the T_{LOW} or T_{HIGH} Limit Register will not be changed. In the case of the Nonvolatile Registers being busy, the device will respond with an ACK to the address and pointer bytes but will then NACK when the data bytes are sent from the Master.

In order to read the T_{LOW} or T_{HIGH} Limit Register, the Pointer Register must be set or have been previously set to 02h to select the T_{LOW} Limit Register or 03h to select the T_{HIGH} Limit Register (if the previous operation was a Write to one of the registers, then the Pointer Register will already be set for that particular limit register). If the Pointer Register has already been set appropriately, the T_{LOW} or T_{HIGH} Limit Register can be read by having the Master first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA1 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master can then read the upper byte of the T_{LOW} or T_{HIGH} Limit Register. After the upper byte of the register has been clocked out of the AT30TSE752A/754A/758A, the Master must send an ACK to indicate that it is

ready for the lower byte of data. The AT30TSE752A/754A/758A will then clock out the lower byte of the register, after which the Master must send a NACK to end the operation. When the AT30TSE752A/754A/758A receives the NACK, it will release the SDA line so that the Master can send a Stop or repeated Start condition. If the Master does not send a NACK but instead sends an ACK after the lower byte of the register has been clocked out, then the device will repeat the sequence by outputting the data again starting with the upper byte of the register.

After the device powers up or resets, both the T_{LOW} and T_{HIGH} Limit Register values will be copied from the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers; therefore, the T_{LOW} and T_{HIGH} Limit Register values will default to whatever value was previously stored in the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers prior to power-down or reset. The value of the high temperature limit stored in the T_{HIGH} Limit Register must be greater than the value of the low temperature limit stored in the T_{LOW} Limit Register in order for the ALERT function to work properly; otherwise, the ALERT pin will output erroneous results and will falsely signal temperature alarms.

Figure 6-8. Write to T_{LOW} or T_{HIGH} Limit Register

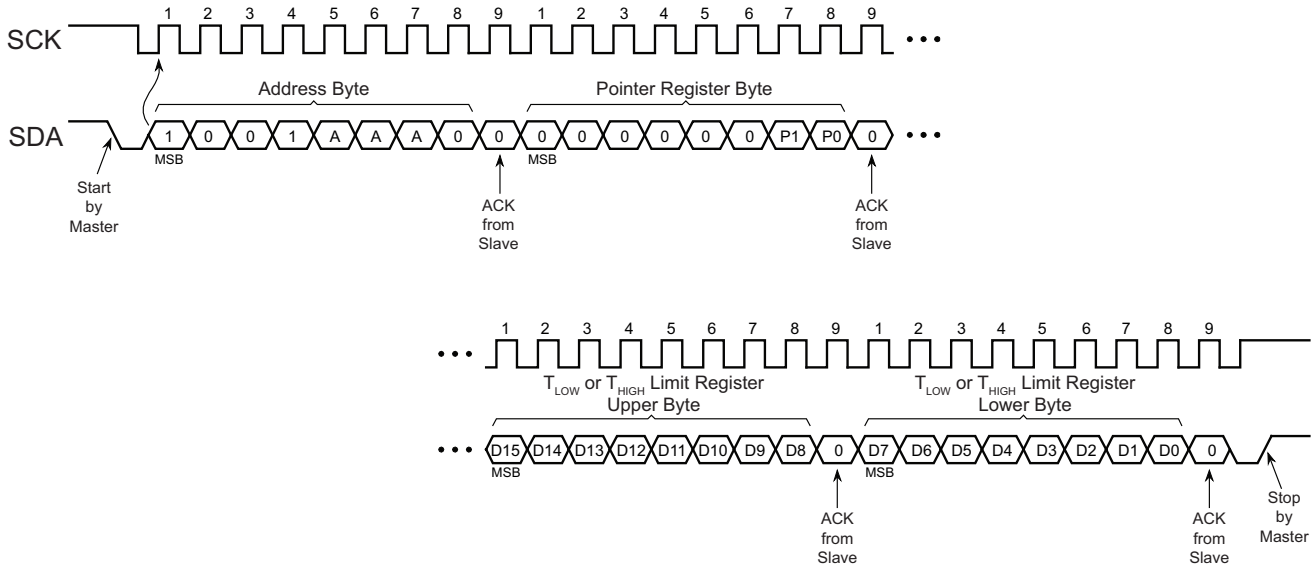
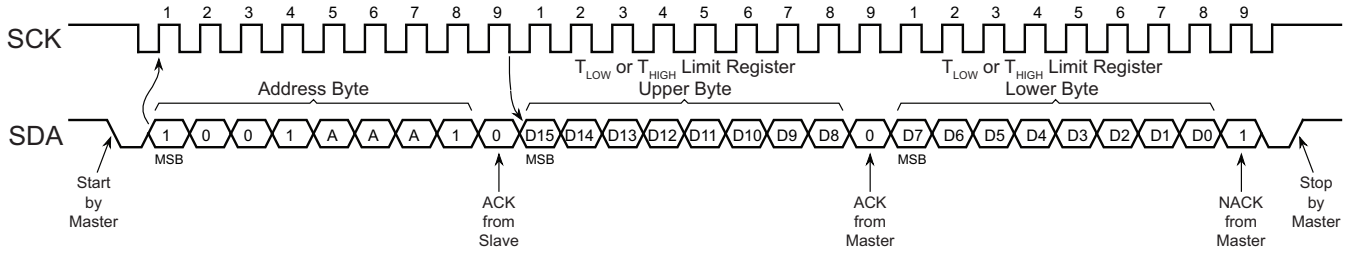


Figure 6-9. Read from T_{LOW} or T_{HIGH} Limit Register



Note: Assumes the Pointer Register was previously set to point to the T_{LOW} or T_{HIGH} Limit Register.

6.6 Nonvolatile T_{LOW} and T_{HIGH} Limit Registers

The 16-bit Nonvolatile T_{LOW} and T_{HIGH} Limit Registers store the power-up/reset default values for the volatile versions of the T_{LOW} and T_{HIGH} Limit Registers. Like their volatile counterparts, the temperature data values of the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers are stored in the twos complement format with the MSB (bit 15) of the registers containing the sign bit (zero indicates a positive number and a one indicates a negative number).

The values stored in both the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers will be retained even after the device has been powered down or reset. On every power-up or reset sequence, the contents of the Nonvolatile T_{LOW} Limit Register will be copied into the T_{LOW} Limit Register, and the contents of the Nonvolatile T_{HIGH} Limit Register will be copied into the T_{HIGH} Limit Register. All temperature limit comparisons for the temperature alarm will be done using the volatile versions of the T_{LOW} and T_{HIGH} Limit Registers. By utilizing the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers, the device can power-up or reset with pre-defined temperature limits specific to the particular application. Therefore, unlike standard LM75-type temperature sensors, there is no need to update the lower and upper temperature limit values after every power-up or reset.

Like the Nonvolatile Configuration Register, the Nonvolatile T_{LOW} and T_{HIGH} Limit Registers utilize nonvolatile storage cells, so the same care must be taken when updating the registers to accommodate for the associated program time and finite program endurance limit. Power must not be removed from the device during the internally self-timed programming cycle of the registers. If power is removed prior to the completion of the programming cycle, then the contents of the register being updated cannot be guaranteed. In addition, the contents of the register may become corrupt if it is programmed more than the maximum allowed number of writes.

As with the Temperature Register, the resolution selected by the R1 and R0 bits of the Configuration Register will determine how many bits of the T_{LOW} and T_{HIGH} Limit Registers will be used. Therefore, when writing to the T_{LOW} and T_{HIGH} Limit Registers, up to 12 bits of data will be recognized by the device with the remaining LSBs being internally fixed to the Logic 0 state. Similarly, when reading from the T_{LOW} and T_{HIGH} Limit Registers, up to 12 bits of data will be output from the device with the remaining LSBs fixed in the Logic 0 state.

Table 6-12. Nonvolatile T_{LOW} Limit Register and T_{HIGH} Limit Register Format

	Upper Byte								Lower Byte							
Resolution	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0
11 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0
10 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0
9 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0	0

Note: TD = Temperature Data

To set the value of either the Nonvolatile T_{LOW} or T_{HIGH} Limit Register, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 12h to select the Nonvolatile T_{LOW} Limit Register or 13h to select the Nonvolatile T_{HIGH} Limit Register. After the Pointer Register byte has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After receiving the ACK from the AT30TSE752A/754A/758A, the Master must then send two data bytes to the AT30TSE752A/754A/758A to set the value of the Nonvolatile T_{LOW} or T_{HIGH} Limit Register. Any subsequent bytes sent to the AT30TSE752A/754A/758A will simply be ignored by the device. If the Master does not send two complete bytes of data prior to issuing a Stop or repeated Start condition, then the AT30TSE752A/754A/758A will ignore the data and the contents of the register will not be changed.

After the Master has issued a Stop condition, the AT30TSE752A/754A/758A will begin the internally self-timed program operation, and the contents of the Nonvolatile T_{LOW} or T_{HIGH} Limit Register will be updated within a time of t_{PROG}. During

this time, the NVRBSY bit of the Configuration Register will indicate that the device is busy. If the Master issues a repeated Start condition instead of a Stop condition, the AT30TSE752A/754A/758A will abort the operation and the contents of the Nonvolatile T_{LOW} or T_{HIGH} Limit Register will not be changed.

In addition to the Master not sending two complete bytes of data, writing to the Nonvolatile T_{LOW} or T_{HIGH} Limit Register will be ignored and no operation will be performed under the following conditions: the Nonvolatile Registers are already busy (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK, except in the case of the Nonvolatile Registers being busy, to indicate that it received the proper data bytes even though the program operation will not be performed. In the case of the Nonvolatile Registers being busy, the device will respond with an ACK to the address and pointer bytes but will then NACK when the data bytes are sent from the Master.

In order to read the Nonvolatile T_{LOW} or T_{HIGH} Limit Register, the Pointer Register must be set or have been previously set to 12h to select the Nonvolatile T_{LOW} Limit Register or 13h to select the Nonvolatile T_{HIGH} Limit Register (if the previous operation was a Write to one of the registers, then the Pointer Register will already be set for that particular limit register). If the Pointer Register has already been set appropriately, the Nonvolatile T_{LOW} or T_{HIGH} Limit Register can be read by having the Master first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA1 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master can then read the upper byte of the Nonvolatile T_{LOW} or T_{HIGH} Limit Register. After the upper byte of the register has been clocked out of the AT30TSE752A/754A/758A, the Master must send an ACK to indicate that it is ready for the lower byte of data. The AT30TSE752A/754A/758A will then clock out the lower byte of the register, after which the Master must send a NACK to end the operation. When the AT30TSE752A/754A/758A receives the NACK, it will release the SDA line so that the Master can send a Stop or repeated Start condition. If the Master does not send a NACK but instead sends an ACK after the lower byte of the register has been clocked out, then invalid data will be output by the device.

The Nonvolatile T_{LOW} Limit Register is factory-set to default to 4B00h (+75°C) and the Nonvolatile T_{HIGH} Limit Register is set to default to 5000h (+80°C); therefore, both registers will need to be modified if these default temperature limits are not satisfactory for the application.

Figure 6-10. Write to Nonvolatile T_{LOW} or T_{HIGH} Limit Register

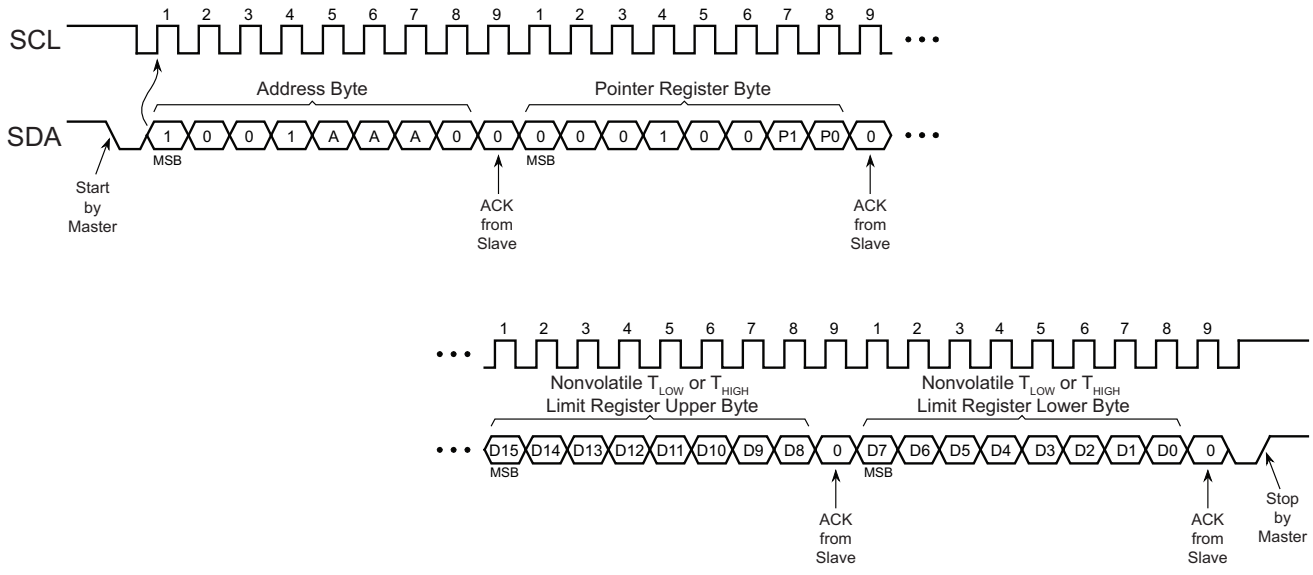
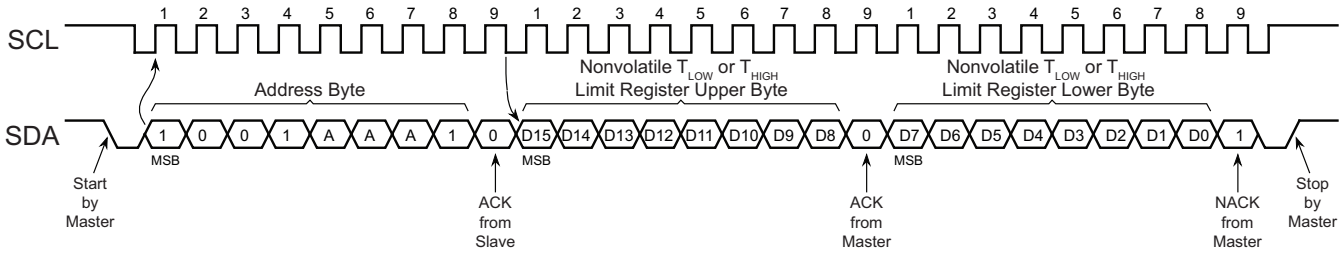


Figure 6-11. Read to Nonvolatile T_{LOW} or T_{HIGH} Limit Register



Note: Assumes the Pointer Register was previously set to point to the Nonvolatile T_{LOW} or T_{HIGH} Limit Register.

7. Register Locking

All Volatile and Nonvolatile Configuration and Limit Registers (the Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register) can be locked from data changes by utilizing the RLCK bit in the Nonvolatile Configuration Register. This provides the ability to lock the registers and protect them from inadvertent or erroneous data changes, giving system designers a more robust and secure temperature sensing solution compared to other industry devices. The RLCK bit can be reset so that the various registers can be modified if needed. Resetting of the RLCK bit is done by writing to the Nonvolatile Configuration Register and changing the RLCK bit back to a Logic 0 state. When the registers are locked, only the RLCK bit of the Nonvolatile Configuration Register can be altered, and any attempts at changing other bits in the Nonvolatile Configuration Register will be ignored.

In addition, the Volatile and Nonvolatile Configuration and Limit Registers can be permanently locked down by using the RLCKDWN bit in the Nonvolatile Configuration Register. When the RLCKDWN bit is set, the Volatile and Nonvolatile Configuration and Limit Registers will be permanently locked down so that they can never be modified again. Unlike the RLCK bit, the RLCKDWN bit is one-time programmable and cannot be reset. Therefore, the lockdown mechanism is not reversible. The RLCKDWN bit takes priority over the RLCK bit (see Table 7-1).

Having the ability to permanently lock down the Volatile and Nonvolatile Configuration and Limit Registers provides the ability to have a pre-defined, secure, and unchangeable temperature sensing solution for applications dealing with liability, risk, or safety concerns.

The register locking is not affected by power cycles or reset operations, including the General Call Reset; therefore, if a device is power cycled or reset with the registers in the locked or locked-down state, then the registers will remain locked or locked-down when normal device operation resumes.

Table 7-1. Register Locking

RLCKDWN	RLCK	Locking Status
0	0	Volatile and Nonvolatile Configuration and Limit Registers are unlocked and can be modified.
0	1	Volatile and Nonvolatile Configuration and Limit Registers are locked and cannot be modified except for the RLCK bit of the Nonvolatile Configuration Register which can be reset.
1	0	Volatile and Nonvolatile Configuration and Limit Registers are permanently locked down and can never be modified again.
1	1	Volatile and Nonvolatile Configuration and Limit Registers are permanently locked down and can never be modified again.

8. Operations Allowed During Nonvolatile Busy Status

While the AT30TSE752A/754A/758A is busy performing nonvolatile operations such as programming the Nonvolatile Configuration Register or the Serial EEPROM, certain other operations can still be executed. Table 8-1 details which commands are allowed or not allowed during a Nonvolatile Busy operation. For those commands that are not allowed during a Nonvolatile Busy operation, the device will respond with a NACK where it would normally respond with an ACK.

Example: If attempting to write to the Nonvolatile Configuration Register, the device would respond with an ACK after the device address byte and Pointer Register byte but then respond with a NACK instead of an ACK after the Master has sent the upper byte of configuration register data.

When attempting to read a register during a Nonvolatile Busy operation, the device will NACK instead of ACK after the AT30TSE752A/754A/758A device address byte has been received.

Table 8-1. Commands Allowed During Nonvolatile Busy Operations

Command	Allowed or Not Allowed
Write to Pointer Register	Allowed
Read Temperature Register	Allowed
Read Configuration Register	Allowed(1)
Write Configuration Register	Not Allowed
Read T_{LOW} or T_{HIGH} Limit Register	Allowed(1)
Write T_{LOW} or T_{HIGH} Limit Register	Not Allowed
Read or Write Nonvolatile Configuration Register	Not Allowed
Read or Write Nonvolatile T_{LOW} or T_{HIGH} Limit Register	Not Allowed
Copy Nonvolatile Registers to Volatile Registers	Not Allowed
Copy Volatile Registers to Nonvolatile Registers	Not Allowed
Read or Write to Serial EEPROM	Not Allowed
SMBus Alert Response Address (ARA)	Not Allowed
General Call (04h)	Not Allowed
General Call Reset (06h)	Not Allowed

Note: 1. Not allowed during Copy Nonvolatile Registers to Volatile Registers operation.

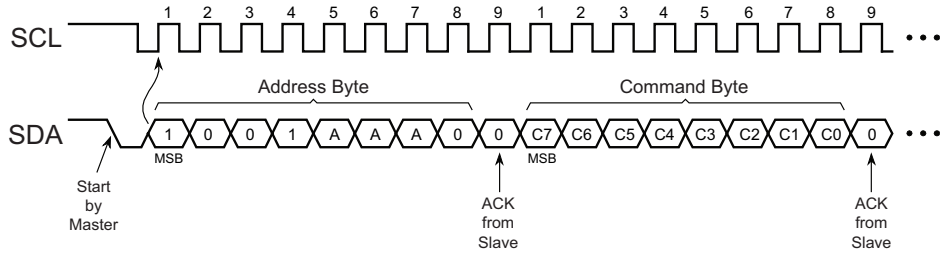
9. Other Commands

The AT30TSE752A/754A/758A incorporates additional commands for other device functions. The command opcode consists of a single byte of data that is sent from the Master to the AT30TSE752A/754A/758A in place of the Pointer Register byte; therefore, the device must first be addressed by the Master and then given the subsequent command opcode. Sending any of the command opcodes to the AT30TSE752A/754A/758A will not change the contents of the Pointer Register byte.

Table 9-1. Command Listing

Command	Opcode	
Copy Nonvolatile Registers to Volatile Registers	B8h	1011 1000
Copy Volatile Registers to Nonvolatile Registers	48h	0100 1000

Figure 9-1. Command Loading



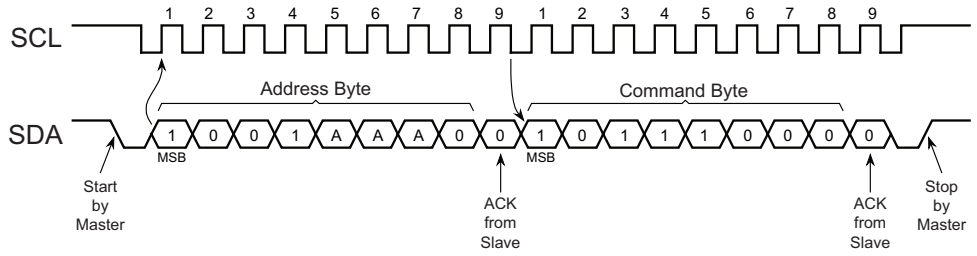
9.1 Copy Nonvolatile Registers to Volatile Registers

The Copy Nonvolatile Registers to Volatile Registers command allows the contents of the Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register to be copied into the Configuration Register, T_{LOW} Limit Register, and T_{HIGH} Limit Register. The copy process is automatically performed upon power-up or reset, but the Copy Nonvolatile Registers to Volatile Registers command provides the ability to re-copy the data registers if needed.

To copy the contents of the Nonvolatile Data Registers into the Volatile Data Registers, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the command byte of B8h for the Copy Nonvolatile Registers to Volatile Registers operation. After the command byte of B8h has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After the Master has subsequently issued a Stop or repeated Start condition, the AT30TSE752A/754A/758A will begin the internally self-timed copy operation. The copy process will take place in a maximum time of t_{COPYR} during which time the NVRBSY bit in the Configuration Register will indicate that the nonvolatile registers are busy. If the Master issues a repeated Start condition instead of a Stop condition, the AT30TSE752A/754A/758A will abort the copy operation and the contents of the Volatile Data Registers will not be changed.

The Copy Nonvolatile Registers to Volatile Registers command will be ignored and no operation will be performed under the following conditions: the Nonvolatile Registers are already busy (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK to indicate that it received the command byte even though the copy process will not be performed.

Figure 9-2. Copy Nonvolatile Registers to Volatile Registers



9.2 Copy Volatile Registers to Nonvolatile Registers

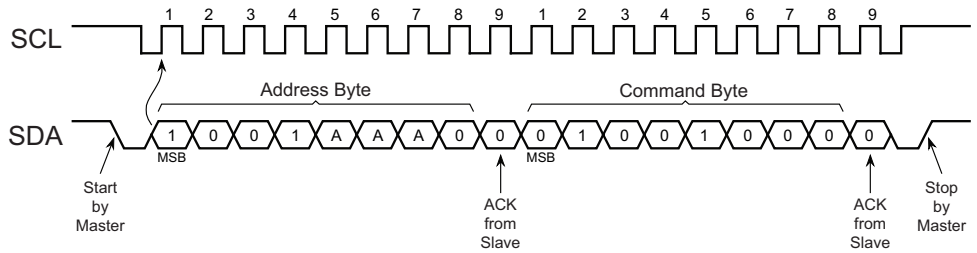
The Copy Volatile Registers to Nonvolatile Registers command allows the contents of the Configuration Register, T_{LOW} Limit Register, and T_{HIGH} Limit Register to be copied into the Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register. The Copy Volatile Registers to Nonvolatile Registers command can be used in the event that the Volatile Data Registers are modified and it is desired for that newly modified data to become the new power-up/reset defaults.

To copy the contents of the Volatile Data Registers into the Nonvolatile Data Registers, the Master must first initiate a Start condition followed by the AT30TSE752A/754A/758A device address byte (1001AAA0 where “AAA” corresponds to the hard-wired A_{2-0} address pins). After the AT30TSE752A/754A/758A has received the proper address byte, the device will send an ACK to the Master. The Master must then send the command byte of 48h for the Copy Volatile Registers to Nonvolatile Registers operation. After the command byte of 48h has been sent, the AT30TSE752A/754A/758A will send another ACK to the Master. After the Master has subsequently issued a Stop or repeated Start condition, the AT30TSE752A/754A/758A will begin the internally self-timed copy operation. The copy process will take place in a maximum time of t_{COPYW} during which time the NVRBSY bit in the Configuration Register will indicate that the nonvolatile registers are busy. If the Master issues a repeated Start condition instead of a Stop condition, the AT30TSE752A/754A/758A will abort the copy operation and the contents of the Nonvolatile Data Registers will not be changed.

The Copy Volatile Registers to Nonvolatile Registers command will be ignored and no operation will be performed under the following conditions: the nonvolatile registers are already busy (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the volatile and nonvolatile registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the volatile and nonvolatile registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state); however, the device will still respond with an ACK to indicate that it received the command byte even though the copy process will not be performed.

Care must be taken when copying the Volatile Data Registers to the Nonvolatile Data Registers in order to accommodate the associated program time and finite program endurance limit. Power must not be removed from the device during the internally self-timed copy/program cycle. If power is removed prior to the completion of the copy/program cycle, then the contents of the nonvolatile registers cannot be guaranteed. In addition, the contents of the nonvolatile registers may become corrupt if programmed more than the maximum allowed number of Writes.

Figure 9-3. Copy Volatile Registers to Nonvolatile Registers



10. Serial EEPROM

The AT30TSE752A/754A/758A contains an integrated 2Kb, 4Kb, or 8Kb Serial EEPROM that is a drop in functional replacement for a stand alone 2-wire Serial EEPROM device enabling the added benefit of saving board space and component cost. The Serial EEPROM can be used to permanently store system configuration, application specific, and or user preference data.

10.1 Memory Organization

The Serial EEPROM in the AT30TSE752A/754A/758A is internally organized into pages or rows of data bytes. The AT30TSE752A has 256 bytes and is internally organized with 16 pages of 16 bytes in each page. The AT30TSE754A has 512 bytes and is internally organized with 32 pages of 16 bytes in each page. The AT30TSE758A has 1024 bytes and is internally organized with 64 pages of 16 bytes in each page.

Table 10-1. AT30TSE752A/754A/758A Serial EEPROM Memory Organization

Atmel Device	Density	Bytes in each Page	Number of Pages in Array
AT30TSE752A	2Kb (256 bytes)	16	16
AT30TSE754A	4Kb (512 bytes)	16	32
AT30TSE758A	8Kb (1024 bytes)	16	64

10.2 Memory Addressing

Every Serial EEPROM byte location within the AT30TSE752A/754A/758A can be individually accessed for Write or Read operations. To access a byte location requires entering the desired byte address in the address field for a Write or Read operation. The address field size will vary depending on the Serial EEPROM density; the AT30TSE752A requires an 8-bit address field, AT30TSE754A requires a 9-bit address field and the AT30TSE758A requires a 10-bit address field. Table 10-2 shows the address byte and the relationship of the P0 and P1 memory page address bits and the device address bits (A2-A0). The P0 bit is the MSB of the required 9-bit address field for the AT30TSE754A and the P0 and P1 bits are the MSBs of the required 10-bit address field for the AT30TSE758A. The P0 and P1 bits along with the word address byte comprise the required 9-bit or 10-bit address field for the AT30TSE754A and AT30TSE758A, respectively, to enable every byte in the memory to be individually selected for a Write or Read operation.

The software device address bits (A2-A0) must match the corresponding hard-wired device address pins (A_{2-0}) for proper communication (ACK) to occur.

Example: The AT30TSE752A requires that all three device address bits (A2-A0) must match the corresponding hard-wired device address pins (A_{2-0}). The AT30TSE754A requires the device address bits (A2 and A1) must match the hard-wired device address pins (A_2 and A_1). The AT30TSE758A requires only the device address bit (A2) to match the hard-wired device address pin (A_2).

Table 10-2. Serial EEPROM Address Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Atmel Device	Device Type Identifier				Device Address			Read/Write
AT30TSE752A	1	0	1	0	A2	A1	A0	R/$\overline{W}$
AT30TSE754A	1	0	1	0	A2	A1	P0	R/$\overline{W}$
AT30TSE758A	1	0	1	0	A2	P1	P0	R/$\overline{W}$

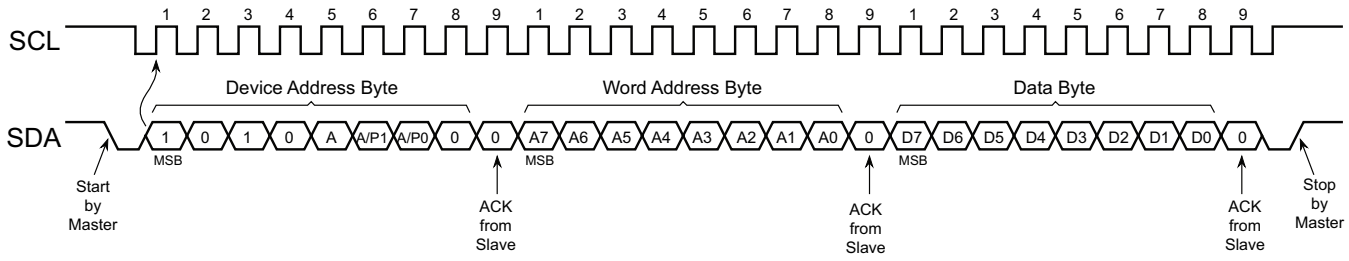
10.3 Write Operations

The Serial EEPROM within the AT30TSE752A/754A/758A supports single byte writes up to a full 16 bytes per page. The only difference between a Byte Write and a Page Write protocol sequence is the amount of data bytes loaded. Regardless of whether a Byte Write or Page Write operation is performed, it will take the same amount of time to write the data to the addressed memory location(s). The internal write cycle will complete in the minimum t_{WR} specification.

10.3.1 Byte Write

Following the Start condition from the Master, the device type identifier (1010), the device address bits and the R/$\overline{W}$, which is Logic 0 state, are placed onto the bus by the Master. This indicates to the addressed device that the Master will follow by transmitting a byte with the word address. The AT30TSE752A/754A/758A will respond with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location in the memory to be written. After receiving an ACK by the AT30TSE752A/754A/758A, the Master will transmit the data byte to be written into the addressed memory location. The AT30TSE752A/754A/758A responds with an ACK and then the Master generates a Stop condition. The Stop condition initiates the internal write cycle and, during this time, the AT30TSE752A/754A/758A will not respond (NACK) to any valid protocol until the write cycle is complete. The internal write cycle will complete in the minimum t_{WR} specification.

Figure 10-1. Byte Write to Serial EEPROM

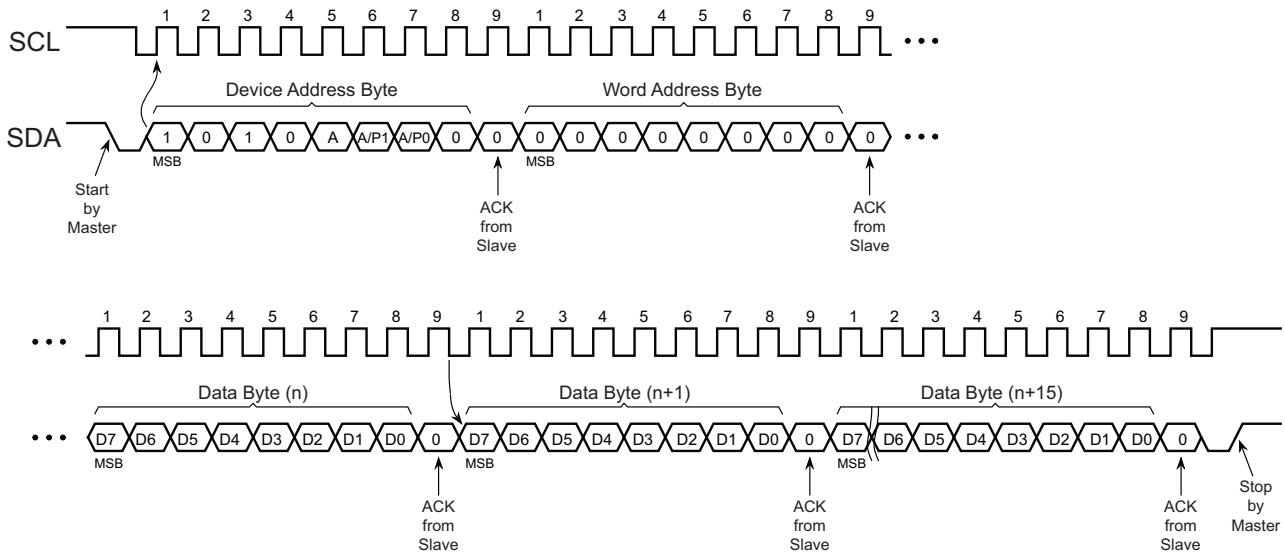


10.3.2 Page Write

The device address byte, word address byte, and the first data byte are transmitted to the AT30TSE752A/754A/758A in the same way as in the Byte Write protocol sequence. But instead of generating a Stop condition, the Master transmits up to 16 data bytes to the AT30TSE752A/754A/758A, which are temporarily stored into an internal page buffer and will be written into memory once the Master has generated the Stop condition. Upon receipt of each data byte, the four lower order word address bits are internally incremented by one since the page size is 16 bytes. If the Master should transmit more than 16 data bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be replaced. As with the Byte Write operation, once the Stop condition is generated by the Master, then the device's internal write cycle will begin. The internal write cycle will complete in the minimum t_{WR} specification. A very important point to understand is that Page Write operations are limited to writing data bytes within a single physical page regardless of the number of bytes actually being written.

Example: If a Page Write operation attempts to write across a physical page boundary, then the data will simply rollover to the beginning of the same page and replace any existing data bytes previously loaded in the page buffer.

Figure 10-2. Page Write to Serial EEPROM



10.3.3 Acknowledge Polling

Since the AT30TSE752A/754A/758A will NACK during a write cycle because it is busy writing data, this can be used to determine when the write cycle is complete and therefore could be used to maximize bus throughput. Once the Stop condition for a write sequence has been issued from the Master, the AT30TSE752A/754A/758A initiates the internally self-timed write cycle and ACK polling can then be immediately started by the Master. This involves the Master transmitting a Start condition followed the device address byte. If the AT30TSE752A/754A/758A is still busy with the write cycle, NACK will be returned by the device. If the write cycle is complete, the device will ACK indicating the write cycle is complete and the Master can then proceed with the next Read or Write operation.

10.4 Read Operations

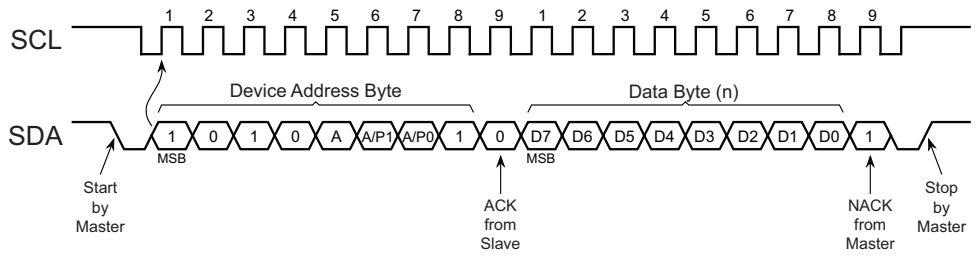
Read operations are initiated in the same way as Write operations, with the exception that the R/$\overline{W}$ is set to a Logic 1 state. There are three basic types of Read operations:

- Current Address Read
- Random Read
- Sequential Read

10.4.1 Current Address Read

The AT30TSE752A/754A/758A contains an internal address counter that maintains the address of the last byte address accessed during the last Read or Write operation incremented by one. The address stays valid between operations as long as the power to the device is maintained. The address rollover during a Read operation is from the last byte of the last memory page to the first byte of the first page. Upon receipt of the device address byte with the R/$\overline{W}$ bit set to a Logic 1 state, the AT30TSE752A/754A/758A will ACK and transmit the 8-bit data byte. The Master will respond with a NACK followed by a Stop condition to end the transmission. It is recommended to not rely on the Current Address Read operation because the only way to guarantee the correct Read Address is to use the Random Read Protocol that loads the specific starting byte address location of the data to be read. For more details about the Random Read Protocol, see Section 10.4.2, Random Read.

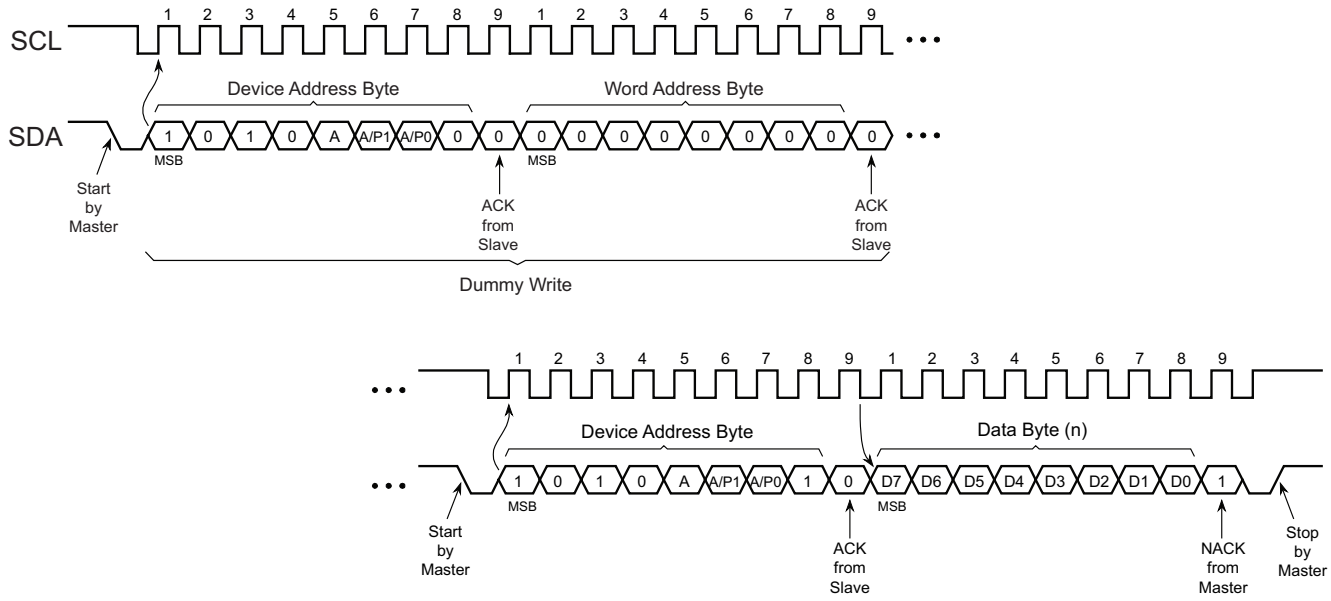
Figure 10-3. Current Address Read from Serial EEPROM



10.4.2 Random Read

Random Read operations allow the Master to access any memory location in a random manner and requires a “dummy write” sequence to preload the byte address of the data byte to be read. To perform this type of Read operation, the data byte address must first be set. This is accomplished by sending the device address byte and the word address byte to the AT30TSE752A/754A/758A as part of a Write operation or “dummy write” sequence. Once the word address byte is sent, the Master generates a Start condition following the ACK. This terminates the Write operation but not before the AT30TSE752A/754A/758A’s internal address pointer is set. This is the reason it is called a “dummy write” sequence as its only purpose is to preload the starting byte address to be read from. The Master then issues the device address byte again, but with the R/$\overline{W}$ bit set to a logic “1” state. The AT30TSE752A/754A/758A will ACK and transmit the data byte. The Master will NACK and generate a Stop condition and the AT30TSE752A/754A/758A will discontinue the transmission.

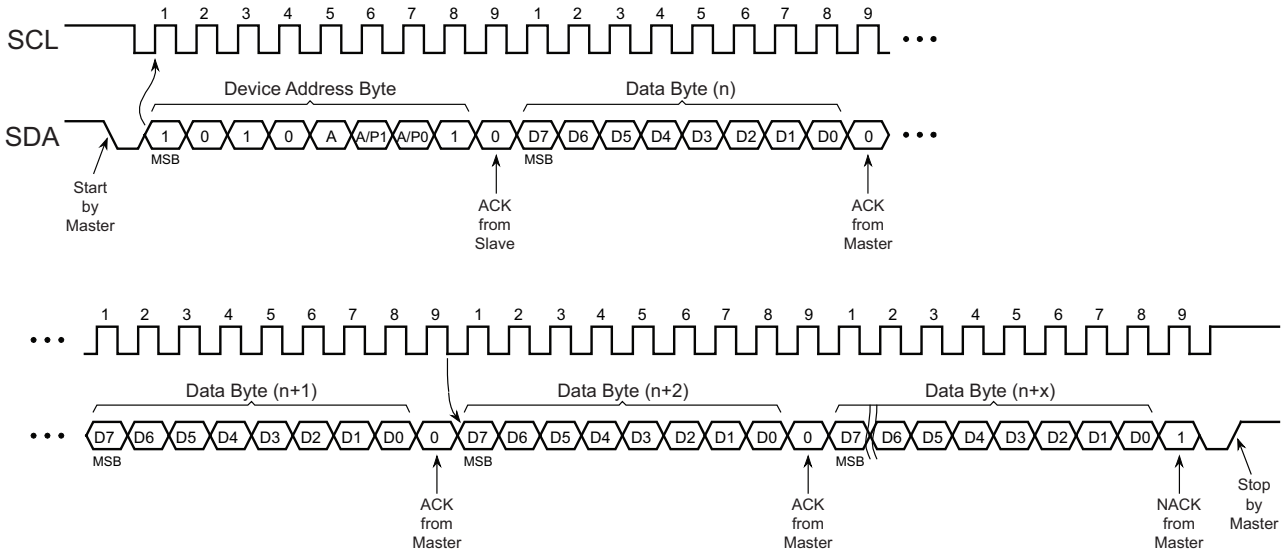
Figure 10-4. Random Read from Serial EEPROM



10.4.3 Sequential Read

Sequential Read operations are initiated in the same way as a Random Read, except that after the AT30TSE752A/754A/758A transmits the first data byte, the Master issues a ACK instead of a NACK and Stop condition in a Random Read operation. This directs the AT30TSE752A/754A/758A to increment the internal address pointer by one and transmit the next sequentially addressed data byte. The AT30TSE752A/754A/758A will repeat and continue transmitting sequential data bytes until the Master wants to terminate the Read operation by issuing a NACK and Stop condition.

Figure 10-5. Sequential Read from Serial EEPROM



10.5 Software Write Protect

The AT30TSE752A/754A/758A features a Reversible Software Write Protect (RSWP) mode that once enabled, disables the Serial EEPROM write circuitry and therefore, protects the contents of the entire memory array against any intentional or unintentional Write operations. The RSWP feature is invoked by sending the “Set RSWP” protocol sequence to the AT30TSE752A/754A/758A that is similar to a normal memory Write command sequence as shown in Table 10-3 and Figure 10-6. The Master can set the memory array to Full Write Protection status by issuing a Start condition followed by 01100010 (62h) and the AT30TSE752A/754A/758A will respond with an ACK. Next, the Master sends the word address byte and the AT30TSE752A/754A/758A will respond with an ACK. Then the Master sends the data byte and the AT30TSE752A/754A/758A will respond with an ACK. The word address and data bytes are don't care values. In addition, during the protocol sequence, the A_2 and A_1 device address pins must be set to ground and the A_0 device address pin set to V_{HV}.

The Software Write Protection can be reversed to no protect status by the Master sending the “Clear RSWP” protocol sequence as shown in Table 10-3 and Figure 10-7. This requires the Master to send a Start condition followed by 01100110 (66h), Word Address Byte, Data Byte, and a Stop condition with an ACK response from the AT30TSE752A/754A/758A after each byte transferred. The word address and data bytes are don't care values. In addition, during the protocol sequence, the A_2 device address pin must be set to ground, A_1 device address pin set to V_{CC} and the A_0 device address pin set to V_{HV}.

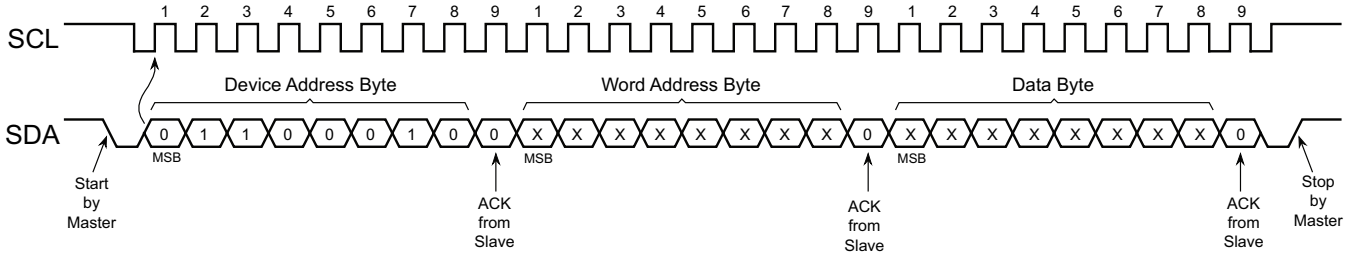
The Write Protection status can be checked to see if the memory array is in full protection or not by sending a Start condition followed by 01100011 (63h), if the AT30TSE752A/754A/758A responds with a NACK, this indicates the memory array is in full write protect. Likewise, if the AT30TSE752A/754A/758A responds with an ACK, this indicates the memory array is not protected.

Table 10-3. Software Write Protection for Serial EEPROM

Command	Device Address Pin			RSWP Write							R/$\overline{W}$
	A2	A1	A0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set RSWP	GND	GND	V_{HV}	0	1	1	0	0	0	1	0
Clear RSWP	GND	V_{CC}	V_{HV}	0	1	1	0	0	1	1	0

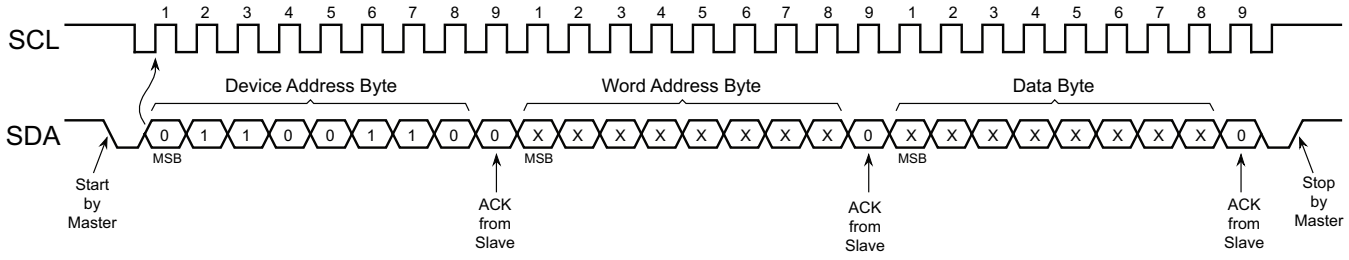
Note: V_{HV} = A_0 Pin High Voltage. See Section 12.3, “DC Characteristics” on page 45 for more information.

Figure 10-6. Set Reversible Software Write Protect



Notes: 1. Apply GND at A_2 and A_1 pins and V_{HV} at A_0 pin.
2. X = Don't care

Figure 10-7. Clear Reversible Software Write Protect



Notes: 1. Apply GND at A2 and V_{CC} at A_1 pin and V_{HV} at A_0 pin.
2. X = Don't care

11. SMBus Features and I²C General Call

11.1 SMBus Alert

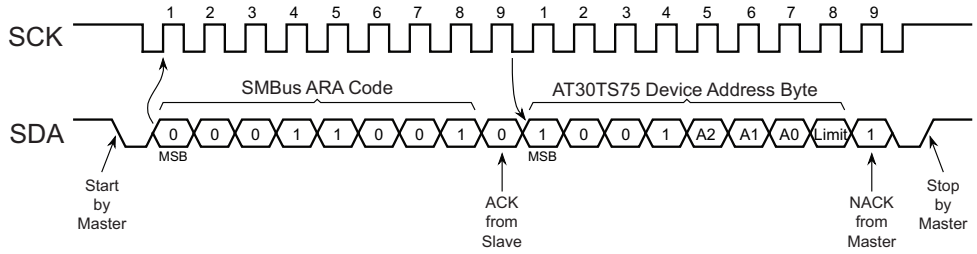
The AT30TSE752A/754A/758A utilizes the ALERT pin to support the SMBus Alert function when the Alarm Thermostat mode is set to the Interrupt mode (the CMP/INT bit of the Configuration Register is set to one) and the ALERT pin polarity is set to active low (the POL bit of the Configuration Register is set to zero). The AT30TSE752A/754A/758A is a slave-only device, and normally, slave devices on the SMBus cannot signal to the Master that they want to communicate; however, the AT30TSE752A/754A/758A uses the SMBus Alert function (the ALERT pin) to signal to the Master that it wants to communicate.

Several SMBus ALERT pins from different slave devices can be connected to a common SMBus Alert input on the Master. When the SMBus Alert input on the Master is pulled low by one of the slave devices, the Master can perform a specialized Read operation from the slave devices to determine which device sent the SMBus Alert signal.

The specialized Read operation is known as an SMBus Alert Response Address (ARA) and requires that the Master first initiate a Start condition followed by the SMBus ARA code of 00011001. The slave device that generated the SMBus Alert signal will respond to the Master with an ACK. After sending the ACK, the slave device will then output its own device address (1001AAA for the AT30TSE752A/754A/758A where “AAA” corresponds to the hard-wired A_{2-0} address pins) on the bus. Since the device address is seven bits long, the remaining eighth bit (the LSB) is used as an indicator to notify the Master which temperature limit caused the alarm (the LSB will be a Logic 1 if the T_{HIGH} limit was met or exceeded, and the LSB will be a Logic 0 if the T_{LOW} limit was exceeded).

The SMBus ARA can activate several slave devices at the same time; therefore, if more than one slave responds, standard SMBus arbitration rules apply and the device with the lowest address wins the arbitration. The device winning the arbitration will clear its SMBus Alert output after it has responded to the SMBus ARA and provided its device address. All other devices with higher addresses do not generate an ACK and continue to hold their SMBus Alert outputs low until cleared. The Master will continue to issue SMBus ARA sequences until all slave devices that generated an SMBus Alert signal have responded and cleared their SMBus Alert outputs.

Figure 11-1. SMBus Alert

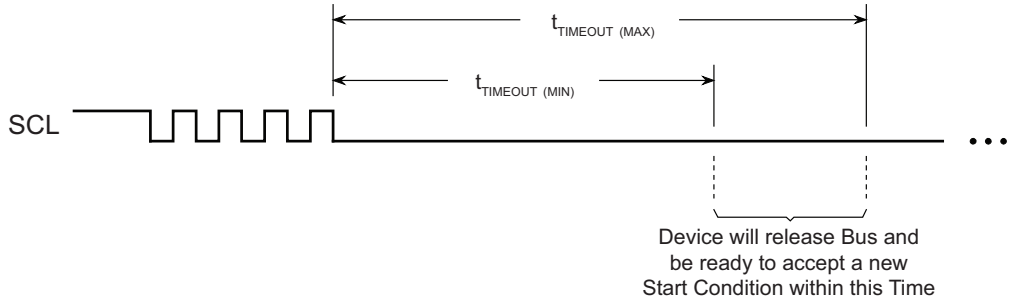


Note: The “Limit” bit (the LSB) of the device address byte will be one or zero depending on if the T_{HIGH} or T_{LOW} limit was exceeded.

11.2 SMBus Timeout

The AT30TSE752A/754A/758A supports the SMBus Timeout feature in which the AT30TSE752A/754A/758A will reset its serial interface and release the SMBus (stop driving the bus and let SDA float high) if the SCL pin is held low for more than the minimum $t_{TIMEOUT}$ specification. The AT30TSE752A/754A/758A will be ready to accept a new Start condition before $t_{TIMEOUT}$ maximum has elapsed.

Figure 11-2. SMBus Timeout



11.3 General Call

The AT30TSE752A/754A/758A will respond to an I^2C General Call address (0000000) from the Master only if the eighth bit (the LSB) of the General Call address byte is zero. If the General Call address byte is 00000000, then the device will send an ACK to the Master and await a command byte from the Master.

If the Master sends a command byte of 04h, then the AT30TSE752A/754A/758A will re-latch the status of its address pins in case the system has assigned a new address to the device. If the Master sends a command byte of 06h (General Call Reset), then the AT30TSE752A/754A/758A will re-latch the status of its address pins and perform a reset sequence. The reset sequence will cause the contents of the Nonvolatile Data Registers to be copied into the Volatile Data Registers, and the device will be busy for a maximum time of t_{POR} during the reset and copying operation.

12. Electrical Specifications

12.1 Absolute Maximum Ratings*

Temperature under Bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Supply voltage with respect to ground	-0.5V to +7.0V
ALERT Pin	-0.5V to V_{CC} + 0.3V
All input voltages with respect to ground	-0.5V to V_{CC} + 0.5V
All other output voltages with respect to ground	-0.5V to V_{CC} + 0.5V

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

Pull-up voltages applied to the ALERT pin that exceed the “Absolute Maximum Ratings” may forward bias to the ESD protection circuitry. Doing so may result in improper device function and may corrupt temperature measurements.

12.2 DC and AC Operating Range

		AT30TSE752A/754A/758A
Operating Temperature (Case)	Industrial High Temperature	-55°C to +125°C(1)(2)
V_{CC} Power Supply		1.7V to 5.5V

Notes: 1. Device operation is guaranteed from -40°C to +125°C.
2. Device operation is not guaranteed at -55°C but ensured by characterization.

12.3 DC Characteristics

Symbol	Parameter	V_{CC} Range	Condition	Min	Typ[1]	Max	Units
I_{CC1}	Active Current, Bus Inactive	1.7V ≤ V_{CC} ≤ 2.0V	Active Temperature Conversions		60	75	µA
		2.7V ≤ V_{CC} ≤ 3.6V			65	95	
		4.5V ≤ V_{CC} ≤ 5.5V			75	100	
I_{CC2}	Active Current, Bus Active	1.7V ≤ V_{CC} ≤ 2.0V	Active Temperature Conversions, f_{SCL} = 400kHz		120	160	µA
		2.7V ≤ V_{CC} ≤ 3.6V			150	225	
		4.5V ≤ V_{CC} ≤ 5.5V			225	325	
I_{CC3}	Active Current, Nonvolatile Register or EEPROM Read	1.7V ≤ V_{CC} ≤ 2.0V	Active Temperature Conversions, f_{SCL} = 400kHz		0.15	0.20	mA
		2.7V ≤ V_{CC} ≤ 3.6V			0.23	0.35	
		4.5V ≤ V_{CC} ≤ 5.5V			0.48	0.63	
I_{CC4}	Active Current, Nonvolatile Register Copy or EEPROM Write	1.7V ≤ V_{CC} ≤ 2.0V	Active Temperature Conversions, f_{SCL} = 400kHz		0.70	1.20	mA
		2.7V ≤ V_{CC} ≤ 3.6V			1.80	2.60	
		4.5V ≤ V_{CC} ≤ 5.5V			2.40	3.20	
I_{SD1}	Shutdown Mode Current, Bus Inactive	1.7V ≤ V_{CC} ≤ 2.0V			0.40	2.50	µA
		2.7V ≤ V_{CC} ≤ 3.6V			0.60	3.50	
		4.5V ≤ V_{CC} ≤ 5.5V			1.20	5.50	
I_{SD2}	Shutdown Mode Current, Bus Active	1.7V ≤ V_{CC} ≤ 2.0V	f_{SCL} = 400kHz		110	140	µA
		2.7V ≤ V_{CC} ≤ 3.6V			130	180	
		4.5V ≤ V_{CC} ≤ 5.5V			180	270	
I_{LI}	Input Leakage Current		V_{IN} = CMOS levels			±1	µA
I_{LO}	Output Leakage Current		V_{OUT} = CMOS levels			±1	µA
V_{IL}	Input Low Voltage					0.3 x V_{CC}	V
V_{IH}	Input High Voltage			0.7 x V_{CC}			V
V_{HV}	A_0 Pin High Voltage, Reversible Write Protection			7		10	V
V_{OL1}	Output Low Voltage		I_{OL} = 3mA			0.4	V
V_{OL2}	Output Low Voltage, ALERT Pin		I_{OL} = 4mA			0.4	V
V_{OH}	Output High Voltage		I_{OH} = -100µA	V_{CC} - 0.2			V

Note: 1. Typical values characterized at T_A = +25°C at V_{CC} = 1.8V, 3.0V, and 5.0V unless otherwise noted.

12.4 Temperature Sensor Accuracy and Conversion Characteristics

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
T_{ACC}	Sensor Accuracy	T_A = 0°C to +85°C		±0.5	±1.0	°C
		T_A = -25°C to +105°C		±1.0	±2.0	
		T_A = -40°C to +125°C		±2.0	±3.0	
		T_A = -55°C to +125°C[2]		±3.0		
T_{RES}	Conversion Resolution	Selectable 9 to 12 bits	0.5 (9 bits)		0.0625 (12 bits)	°C
t_{CONV}	Conversion Time	9-bit Resolution		25	37.5	ms
		10-bit Resolution		50	75	
		11-bit Resolution		100	150	
		12-bit Resolution		200	300	

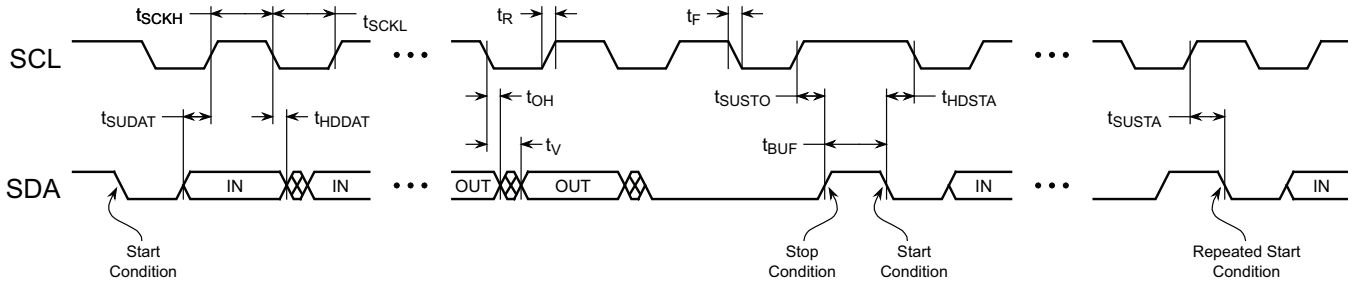
Notes: 1. Typical values characterized at V_{CC} = 3.3V, T_A = +25°C unless otherwise noted.
2. Sensor accuracy characterized to this range but not tested or guaranteed.

12.5 AC Characteristics

Symbol	Parameter	Fast Mode Plus		Units
		Min	Max	
f_{SCL}	Serial Clock Frequency	1[1]	1000	kHz
t_{SCLH}	Clock High Time	260		ns
t_{SCLL}	Clock Low Time	500		ns
t_R	Clock/Data Input Rise Time		120	ns
t_F	Clock/Data Input Fall Time		120	ns
t_{SUDAT}	Data In Setup Time	50		ns
t_{HDDAT}	Data In Hold Time	0		ns
t_V	Output Valid Time		350	ns
t_{OH}	Output Hold Time	0		ns
t_{BUF}	Bus Free Time Between Stop and Start Condition	500		ns
t_{SUSTA}	Repeated Start Condition Setup Time (SCL High to SDA Low)	50		ns
t_{HDSTA}	Start Condition Hold Time (SDA Low to SCL Low)	50		ns
t_{SUSTO}	Stop Condition Setup Time (SCL High to SDA High)	50		ns
t_{NS}	Noise Suppression Input Filter Time		50	ns
$t_{TIMEOUT}$	SMBus Timeout Time	25	75	ms
C_{LOAD}	Capacitive Load for SCL and SDA Lines		400	pF

Note: 1. Minimum clock frequency must be at least 1kHz to avoid activating the SMBus Timeout feature.

Figure 12-1. SMBus/I²C Timing Diagram



12.6 Nonvolatile Register and Serial EEPROM Characteristics

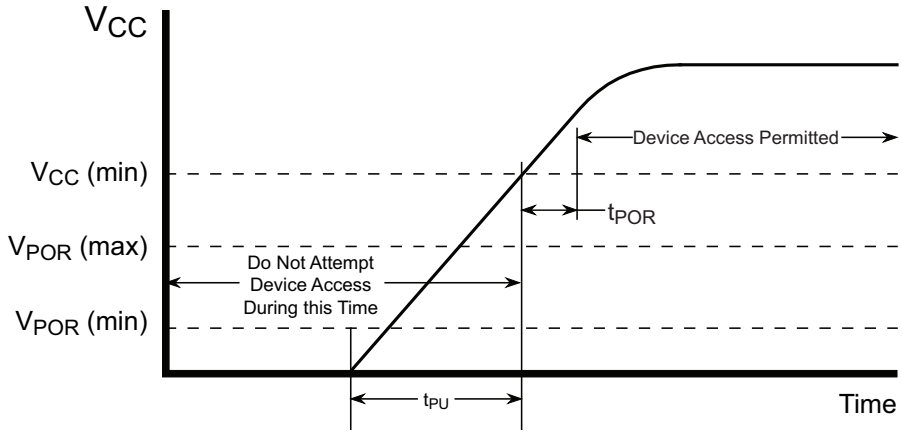
Symbol	Parameter	Min	Typ(1)	Max	Units
t_{PROG}	Nonvolatile Register Program Time		1.0	5.0	ms
t_{WR}	Serial EEPROM Write Cycle Time		3.0	5.0	ms
t_{COPYW}	Volatile to Nonvolatile Register Copy Time		1.0	5.0	ms
t_{COPYR}	Nonvolatile to Volatile Register Copy Time		100	200	µs
N_{ENDUR}	Nonvolatile Register Program/Copy Endurance	50,000	100,000		Cycles
S_{ENDUR}	Serial EEPROM Write Endurance	1,000,000			Cycles

Note: 1. Typical values characterized at V_{CC} = 3.3V, T_A = +25°C unless otherwise noted.

12.7 Power-Up Conditions

Symbol	Parameter	Min	Max	Units
t_{POR}	Power-On Reset Time		1	ms
V_{POR}	Power-On Reset Voltage Range		1.6	V

Figure 12-2. Power-Up Timing

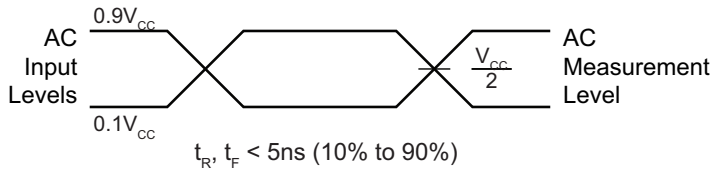


12.8 Pin Capacitance

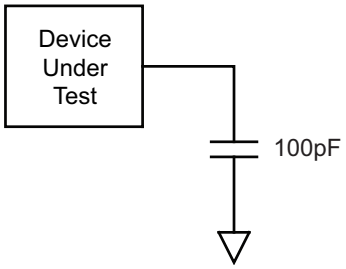
Symbol	Parameter	Min	Max	Units
$C_{I/O}$[1]	Input/Output Capacitance (SDA and ALERT pins)	$V_{I/O}$ = 0V	8	pF
C_{IN}[1]	Input Capacitance (A_{2-0} and SCL pins)	V_{IN}= 0V	6	pF

Note: 1. Not 100% tested (value guaranteed by design and characterization).

12.9 Input Test Waveforms and Measurement Levels

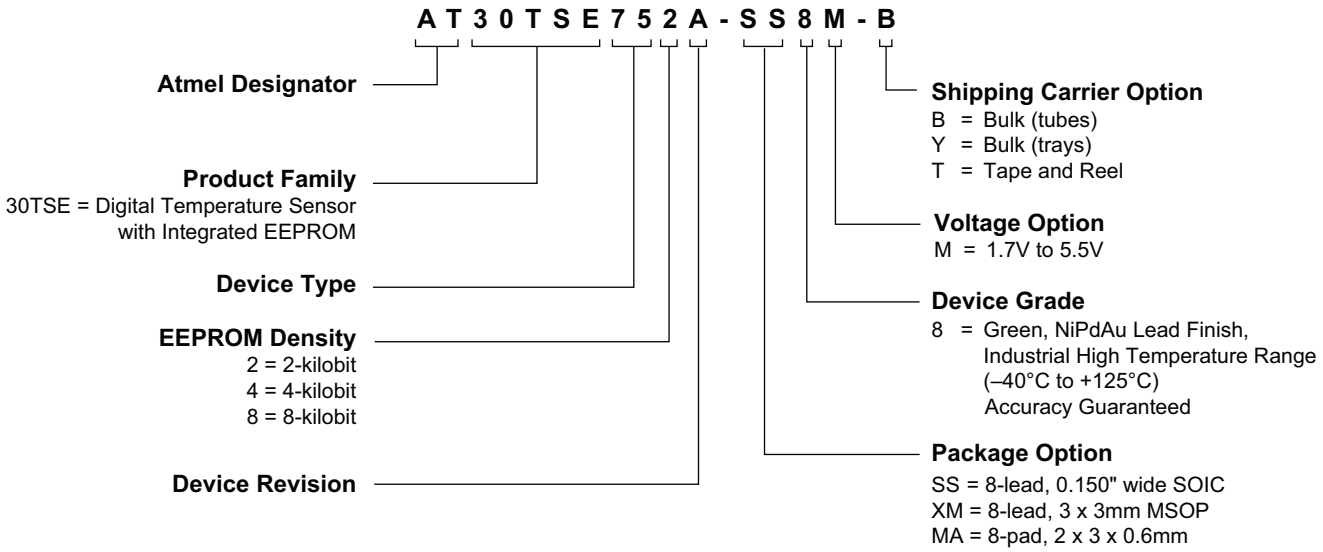


12.10 Output Test Load



13. Ordering Information

13.1 Atmel Ordering Code Detail



13.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

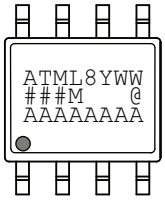
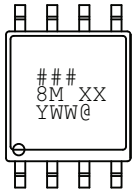
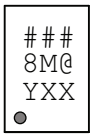
Atmel Ordering Code	Package	Lead (Pad) Finish	Operating Voltage	Max. Freq. (kHz)	Operation Range
AT30TSE752A-SS8M-B	8S1	NiPdAu	1.7V to 5.5V	1000	Industrial High Temperature (-55°C to +125°C)
AT30TSE752A-SS8M-T					
AT30TSE752A-XM8M-B	8XM				
AT30TSE752A-XM8M-T					
AT30TSE752A-MA8M-T	8MA2				
AT30TSE754A-SS8M-B	8S1	NiPdAu	1.7V to 5.5V	1000	Industrial High Temperature (-55°C to +125°C)
AT30TSE754A-SS8M-T					
AT30TSE754A-XM8M-B	8XM				
AT30TSE754A-XM8M-T					
AT30TSE754A-MA8M-T	8MA2				
AT30TSE758A-SS8M-B	8S1	NiPdAu	1.7V to 5.5V	1000	Industrial High Temperature (-55°C to +125°C)
AT30TSE758A-SS8M-T					
AT30TSE758A-XM8M-B	8XM				
AT30TSE758A-XM8M-T					
AT30TSE758A-MA8M-T	8MA2				

Note: The shipping carrier option code is not marked on the devices.

Package Type	
8S1	8-lead, 0.15” wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8XM	8-lead, 3.00 x 3.00mm, Plastic Miniature Small Outline (MSOP)
8MA2	8-pad, 2.00 x 3.00 x 0.60mm, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead (UDFN)

14. Part Marking Detail

AT30TSE752A, AT30TSE754A & AT30TSE758A: Package Marking Information

8-lead SOIC	8-lead MSOP	8-lead UDFN
		2.0 x 3.0 mm Body 

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

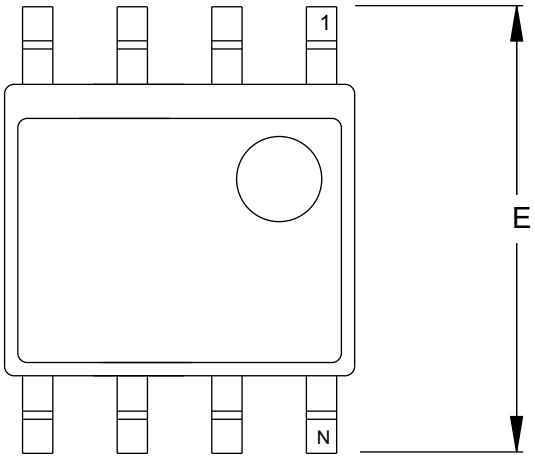
Catalog Number Truncation			
AT30TSE752A		Truncation Code ###: T5A	
AT30TSE754A		Truncation Code ###: T6A	
AT30TSE758A		Truncation Code ###: T7A	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
3: 2013 7: 2017	A: January	02: Week 2	M: 1.7V min
4: 2014 8: 2018	B: February	04: Week 4	
5: 2015 9: 2019	...	...	
6: 2016 0: 2020	L: December	52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		8: Industrial (C) (-40°C to 125°C)/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

1/18/13

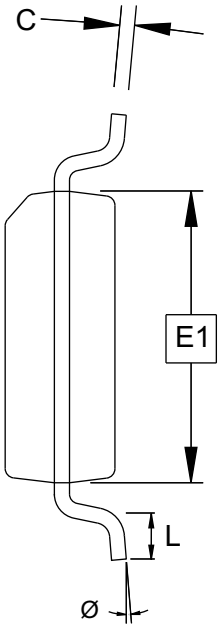
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **AT30TSE75xASM**, AT30TSE752A, AT30TSE754A & AT30TSE758A Package Marking Information	**DRAWING NO.** 30TSE75xASM	**REV.** A

15. Packaging Information

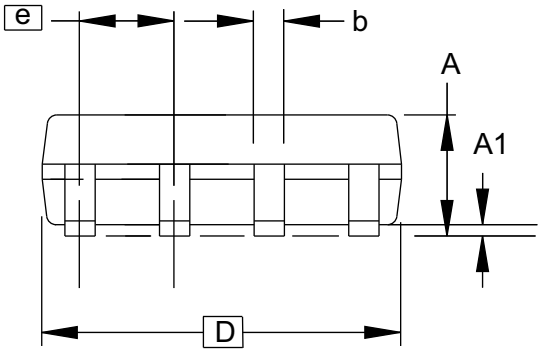
15.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

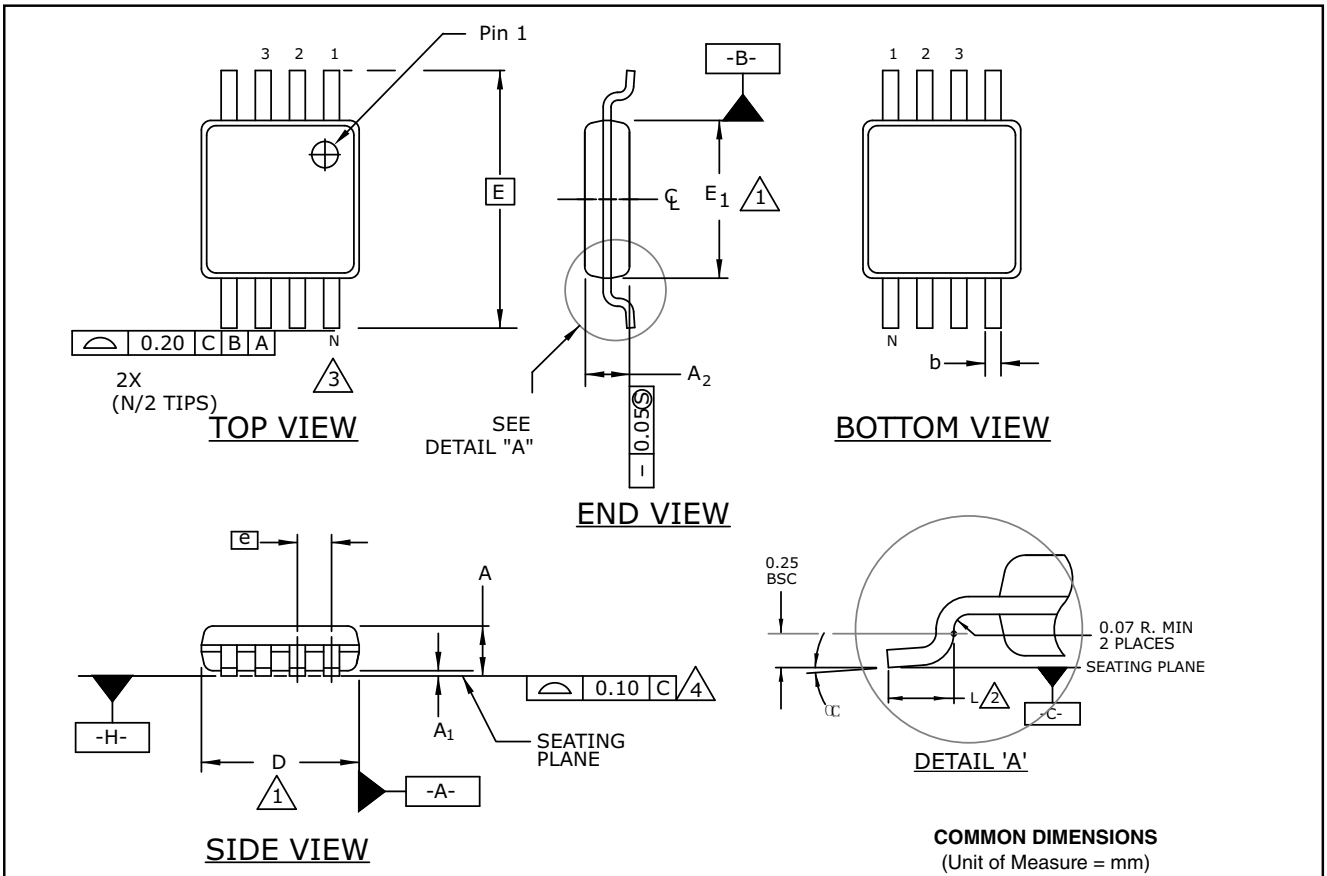
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

15.2 8XM — 8-lead MSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.22	-	0.38	
D	2.90	3.00	3.10	1
E		4.90 BSC		
E_1	2.90	3.00	3.10	1
e		0.65 BSC		
L	0.40	0.55	0.80	2
∝	0°	4°	8°	

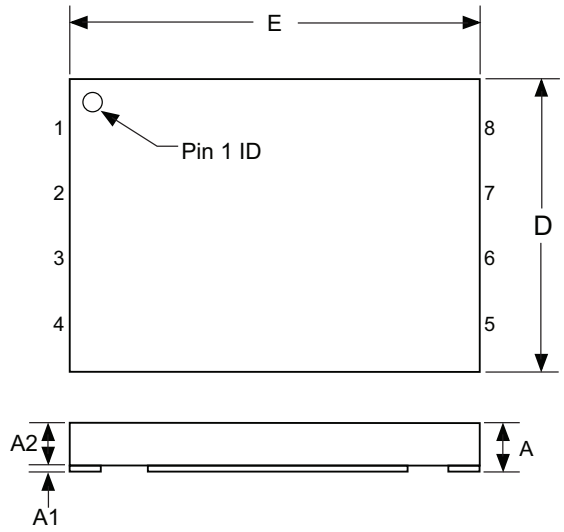
NOTES:

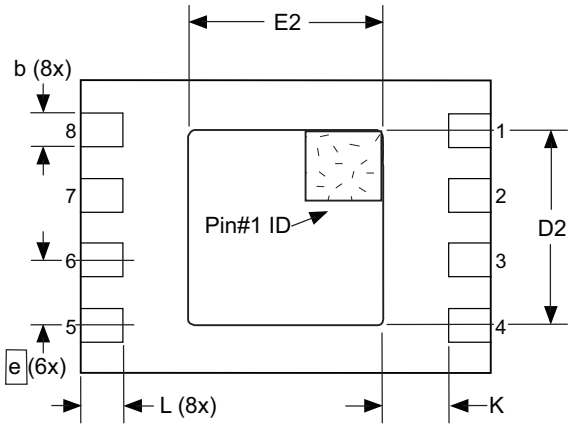
1. DIMENSIONS "D" & "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT DATUM PLANE -H-, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
2. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
3. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.10mm AT SEATING PLANE.
5. DATUMS -A- AND -B- TO BE DETERMINED BY DATUM PLANE -H- .

3/1/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **8XM,** 8-lead, 3.0x3.0mm Body, Plastic Thin Shrink Small Outline Package (TSSOP/MSOP)	GPC TZD	DRAWING NO. 8XM	REV. A

15.3 8MA2 — 8-pad UDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	1.90	2.00	2.10	
E	2.90	3.00	3.10	
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	–	–	0.55	
C	0.152 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
b	0.18	0.25	0.30	3
K	0.20	–	–	

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

9/6/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** C

16. Errata

16.1 No Errata

17. Revision History

Doc. Rev.	Date	Comments
8854E	04/2014	Update the DC Characteristics table, Power-Up Conditions Condition table, and T_{ACC} Sensor Accuracy parameter condition.
8854D	09/2013	Update the Absolute Maximum Ratings. Update the Address Byte table.
8854C	07/2013	Update from preliminary to complete/release status.
8854B	05/2013	Update disclaimer page. Update Tables 12-3 and 12-7. Update 8MA2 package drawing.
8854A	02/2013	Initial document release.





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