STL25DN10F7

Dual N-channel 100 V, 0.068 Ω typ., 5 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 double island package

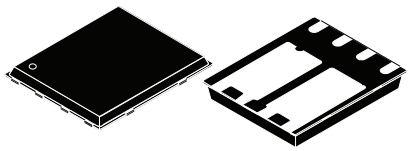
Datasheet — preliminary data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STL25DN10F7	100 V	< 0.08 Ω	5 A (1)

1. The value is rated according $R_{thj-pcb}$.

- N-channel enhancement mode
- Low gate charge
- 100% avalanche rated
- 175 °C junction temperature



PowerFLAT™ 5x6 double island

Applications

- Switching applications
- Automotive

Description

This device utilizes the 7th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Figure 1. Internal schematic diagram

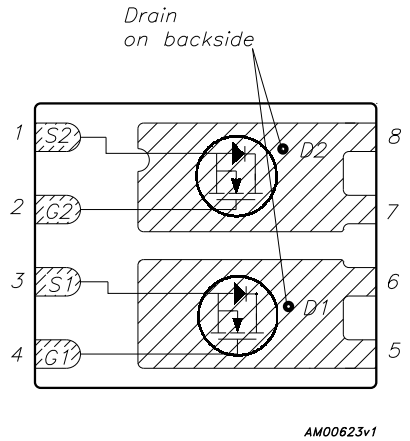


Table 1. Device summary

Order code	Marking	Package	Packaging
STL25DN10F7	25DN10F7	PowerFLAT™ 5x6 double island	Tape and reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	20	A
I_D (1)	Drain current (continuous) at T_C= 100 °C	15	A
I_D (2)	Drain current (continuous) at T_{pcb}= 25 °C	5	A
I_D (2)	Drain current (continuous) at T_{pcb}= 100 °C	3.7	A
I_{DM} (2)(3)	Drain current (pulsed)	20	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	60	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4	W
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 175	°C

1. The value is rated according R_{thj-c}
2. The value is rated according $R_{thj-pcb}$
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	32	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by maximum junction temperature)	TBD	A
E_{AS}	Single pulse avalanche energy (T_J = 25 °C, I_D = I_{AR}, V_{DD} = 14 V)	TBD	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V V_{DS} = 100 V, T_C= 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 2.5 A		0.068	0.08	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	400 110 5	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=50 V, I_D = 5 A V_{GS} =10 V *(see Figure 3)*	-	6 TBD TBD	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=50 V, I_D= 2.5 A, R_G=4.7 Ω, V_{GS}= 10 V *(see Figure 2)*	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		20	A
V_{SD}(2)	Forward on voltage	I_{SD}= 5 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 5 A, di/dt = 100 A/µs, V_{DD}= 80 V, T_j=150 °C *(see Figure 7)*	-	TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

3 Test circuits

Figure 2. Switching times test circuit for resistive load

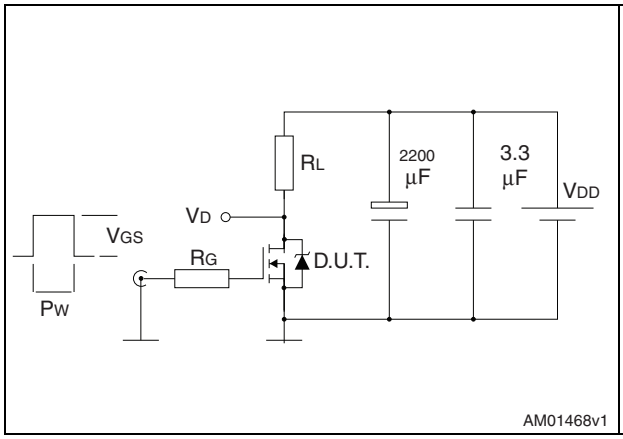


Figure 3. Gate charge test circuit

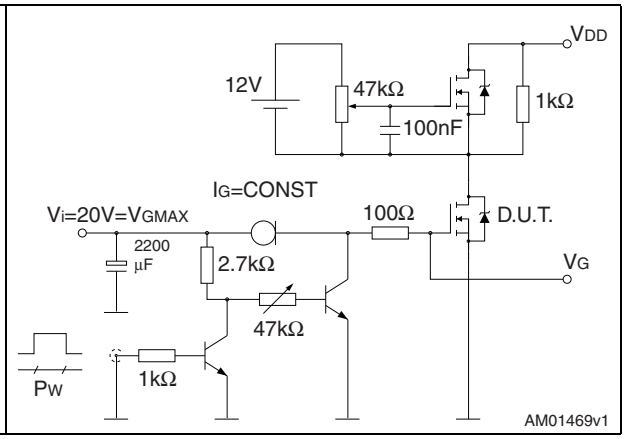


Figure 4. Test circuit for inductive load switching and diode recovery times

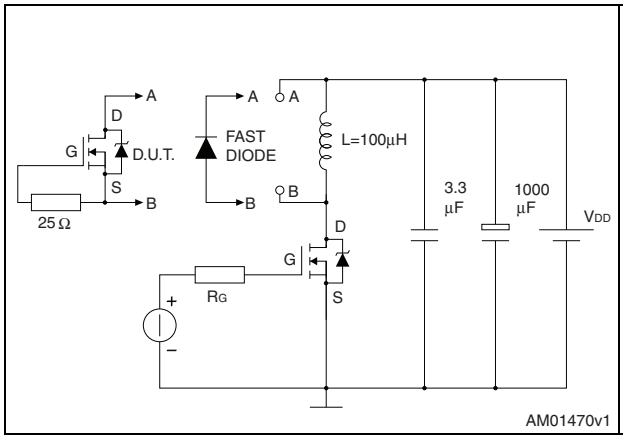


Figure 5. Unclamped inductive load test circuit

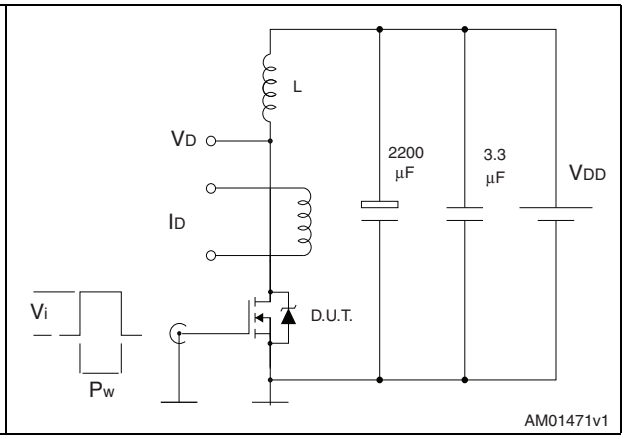


Figure 6. Unclamped inductive waveform

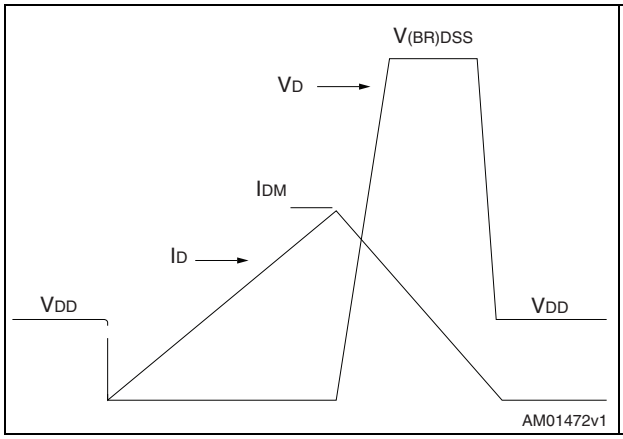
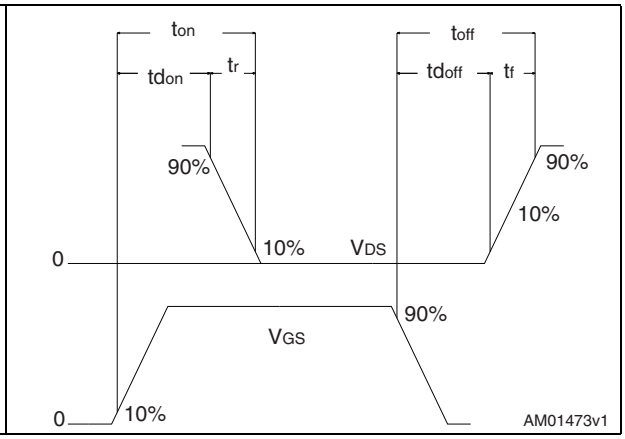


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. PowerFLAT™ 5x6 double island mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 8. PowerFLAT™ 5x6 double island drawing (dimensions are in mm)

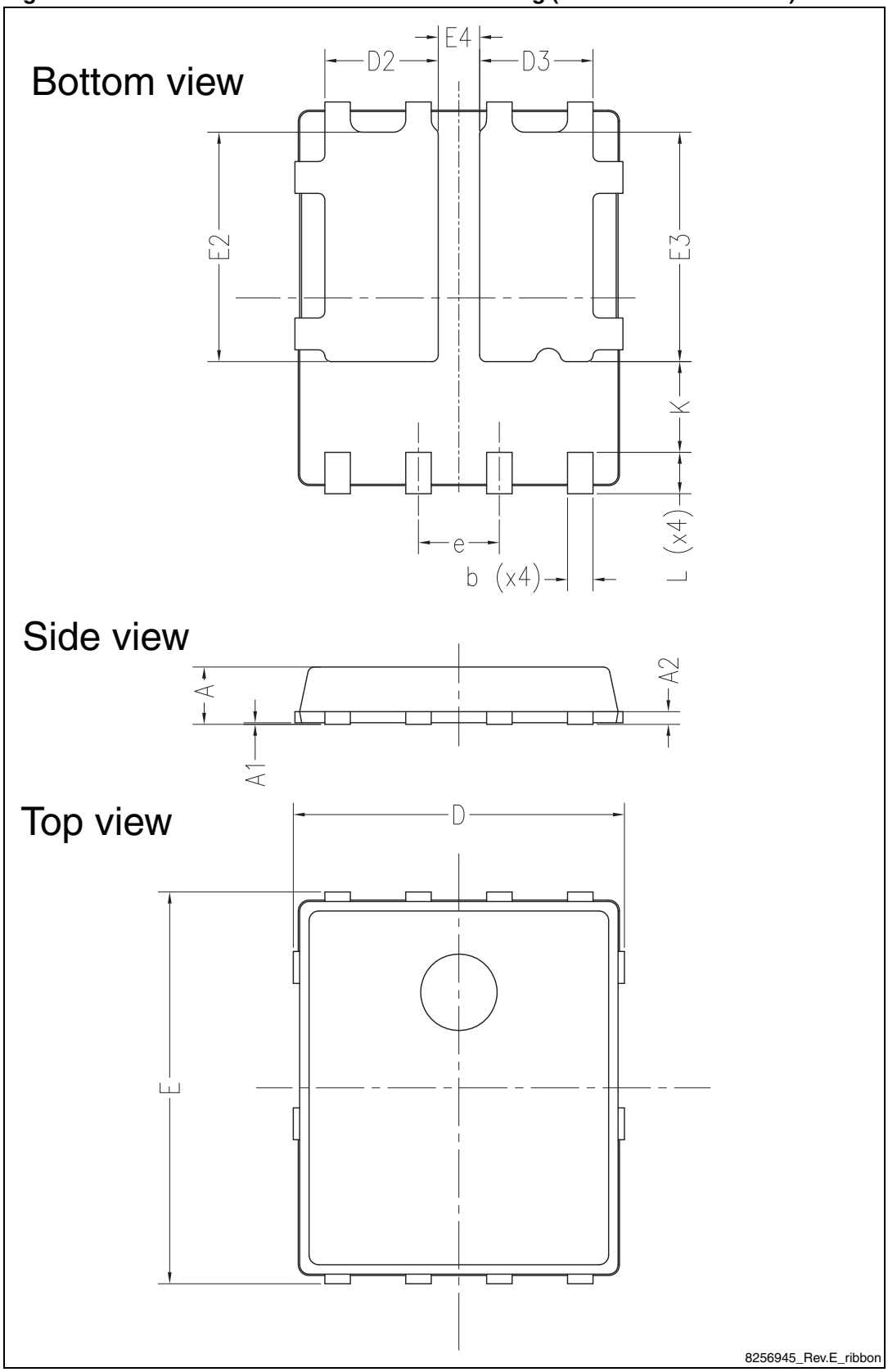
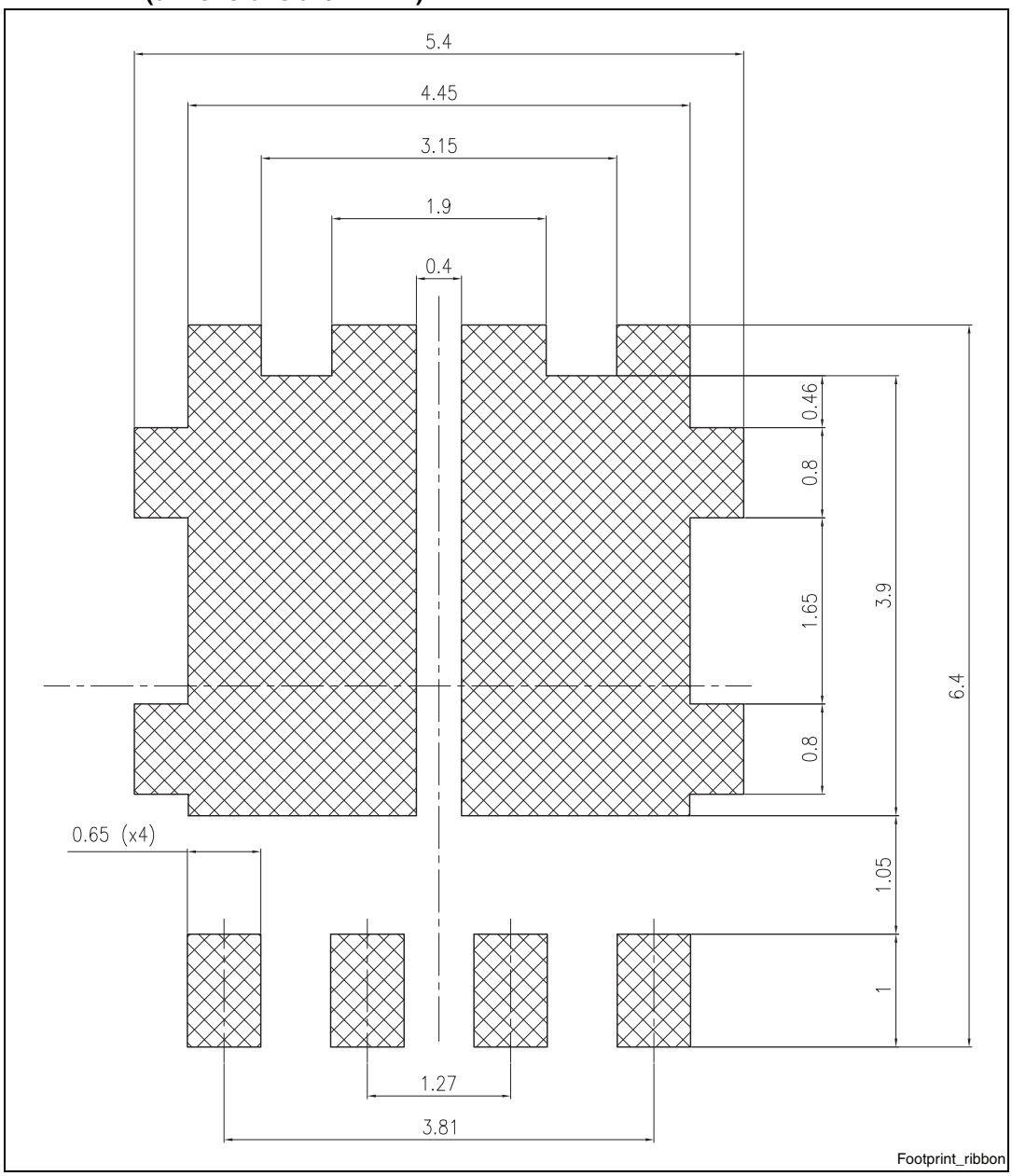


Figure 9. PowerFLAT™ 5x6 double island drawing recommended footprint (dimensions are in mm)



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Jan-2013	1	First release

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