STH170N8F7-2, STP170N8F7

N-channel 80 V, 0.0029 Ω typ., 120 A, STripFET™ VII DeepGATE Power MOSFET in H²PAK-2 and TO-220 packages

Datasheet — target specification

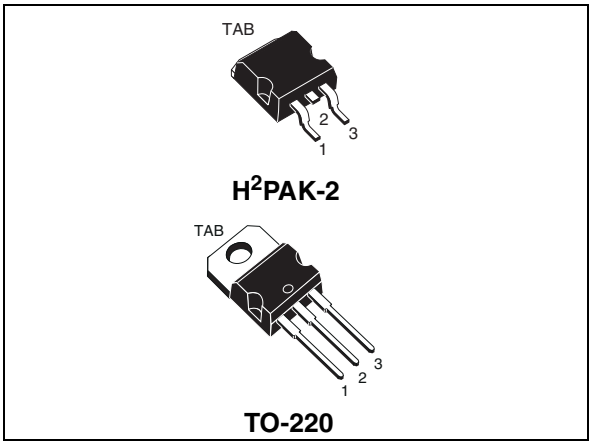
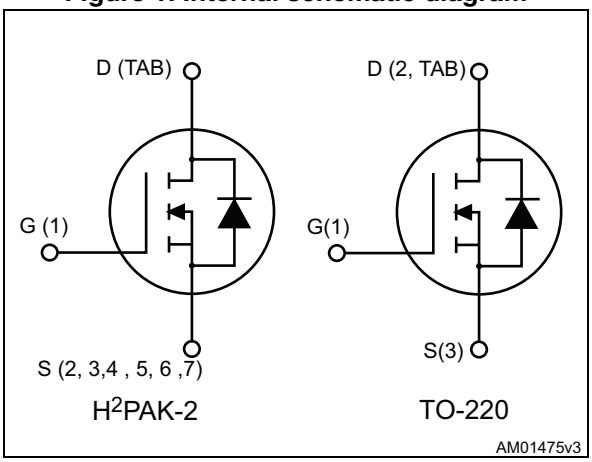


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH170N8F7-2	80 V	0.0036 Ω	120 A	200 W
STP170N8F7	80 V	0.0041 Ω	120 A	200 W

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the 7th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STH170N8F7-2	170N8F7	H²PAK-2	Tape and reel
STP170N8F7		TO-220	Tube

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D(1)	Drain current (continuous)	120	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM}(1)	Drain current (pulsed)	480	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	200	W
E_{AS}(1)	Single pulse avalanche energy	1.16	J
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Limited by package and rated according to R_{thj-c}.

Table 3. Thermal resistance

Symbol	Parameter	Value		Unit
		H^2PAK-2	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.75		°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb	35		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.		62.5	°C/W

1. When mounted on FR-4 board of 1 $inch^2$, 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	80			V
I_{DS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 80 V V_{DS} = 80 V; T_C=125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	For H^2PAK-2: V_{GS}= 10 V, I_D= 60 A		0.0029	0.0036	Ω
		For TO-220: V_{GS}= 10 V, I_D= 60 A		0.0034	0.0041	

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =50 V, f=1 MHz, V_{GS}=0	-	8350	-	pF
C_{oss}	Output capacitance		-	1500	-	pF
C_{rss}	Reverse transfer capacitance		-	45	-	pF
Q_g	Total gate charge	V_{DD}=40 V, I_D = 120 A V_{GS} =10 V *Figure 19*	-	120	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 40 V, I_D= 60 A, R_G= 4.7 Ω, V_{GS}= 10 V *Figure 18*	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM}(1)	Source-drain current (pulsed)		-		480	A
V_{SD}(2)	Forward on voltage	I_{SD} = 120 A, V_{GS}=0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD}= 64 V, T_j=150 °C	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.

3 Electrical characteristics (curves)

Figure 2. Safe operating area for H²PAK-2

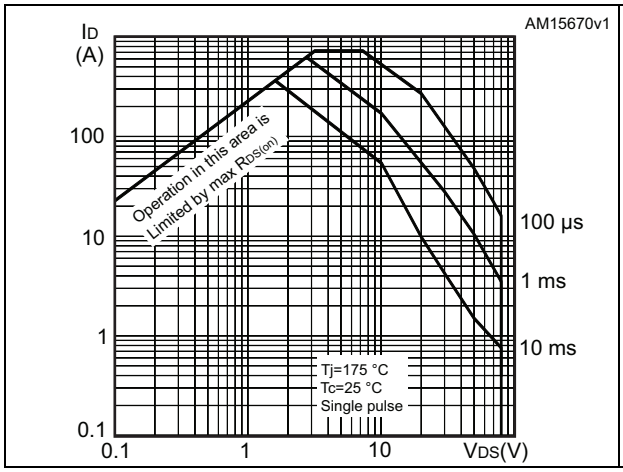


Figure 3. Safe operating area for TO-220

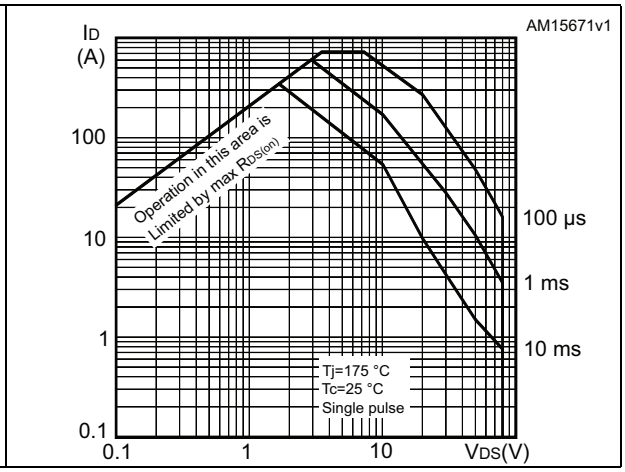


Figure 4. Thermal impedance

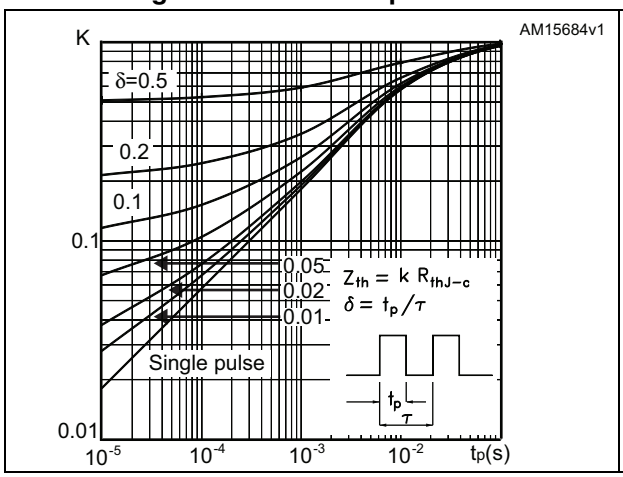


Figure 5. Gate charge vs gate-source voltage

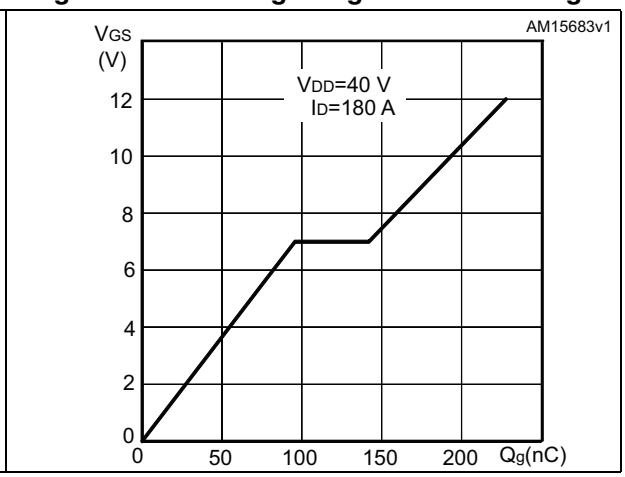


Figure 6. Output characteristics for TO-220

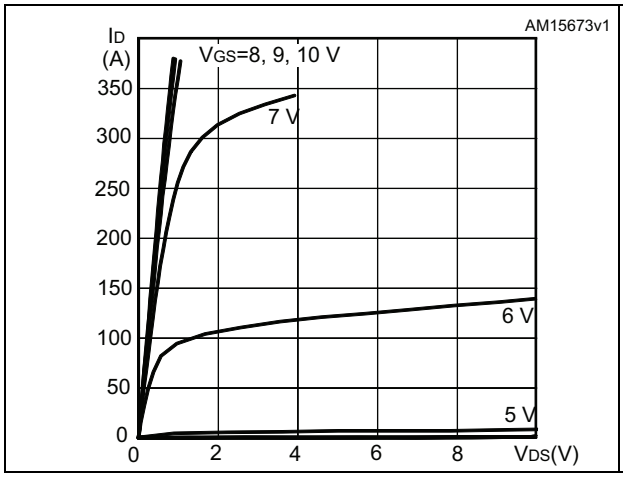


Figure 7. Transfer characteristics for TO-220

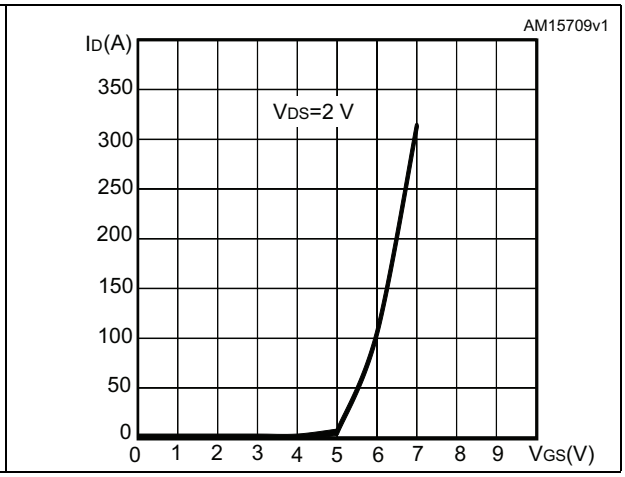


Figure 8. Output characteristics for H²PAK-2

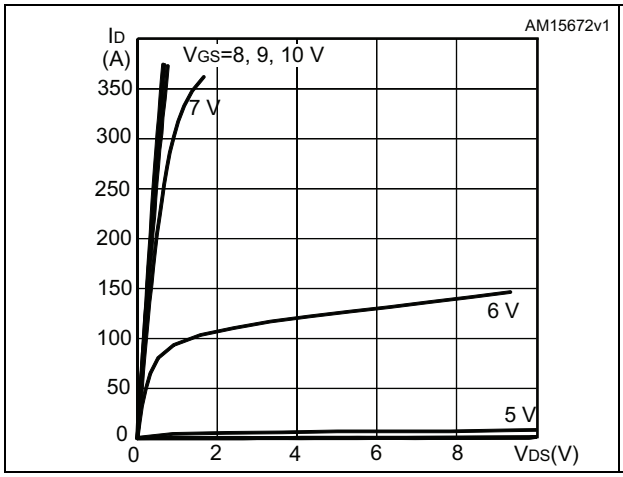


Figure 9. Transfer characteristics for H²PAK-2

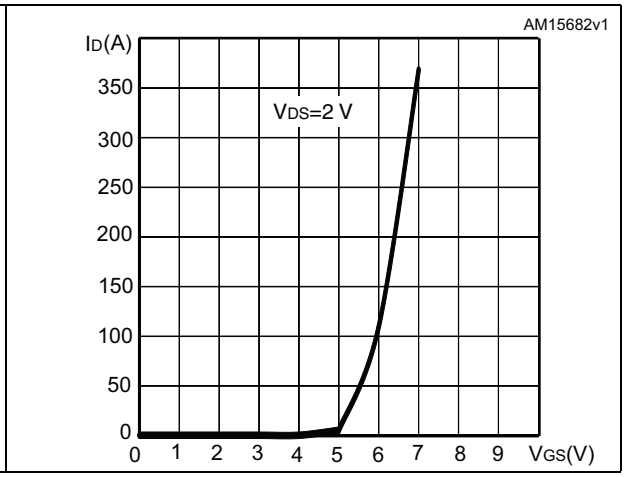


Figure 10. Normalized B_{VDSS} vs temperature

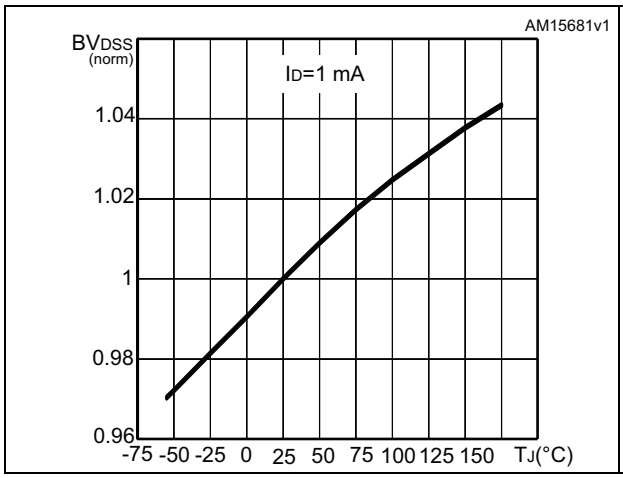


Figure 11. Static drain-source on-resistance for H²PAK-2

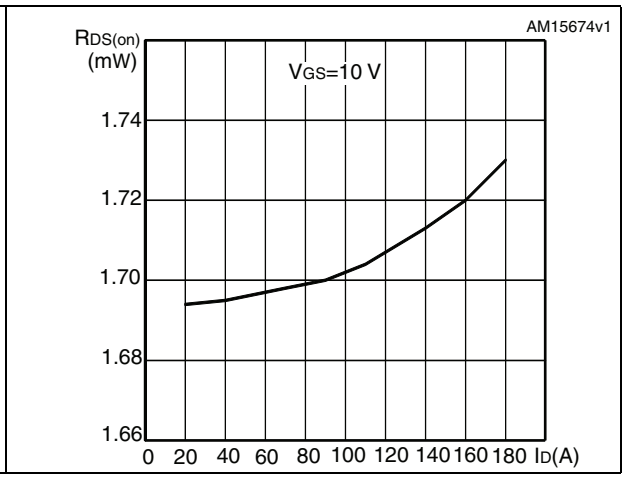


Figure 12. Static drain-source on-resistance for TO-220

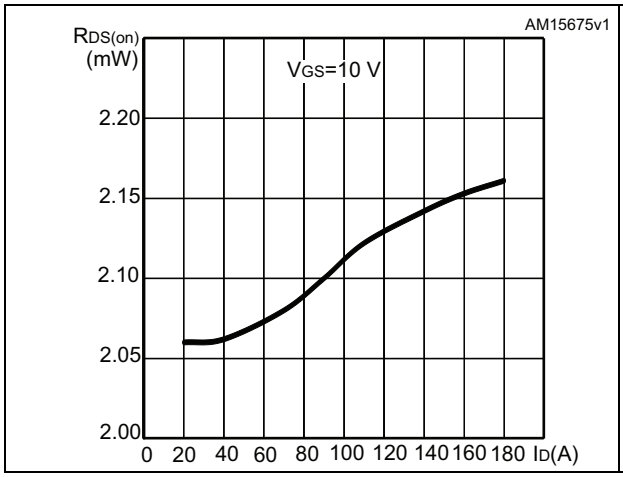


Figure 13. Capacitance variations

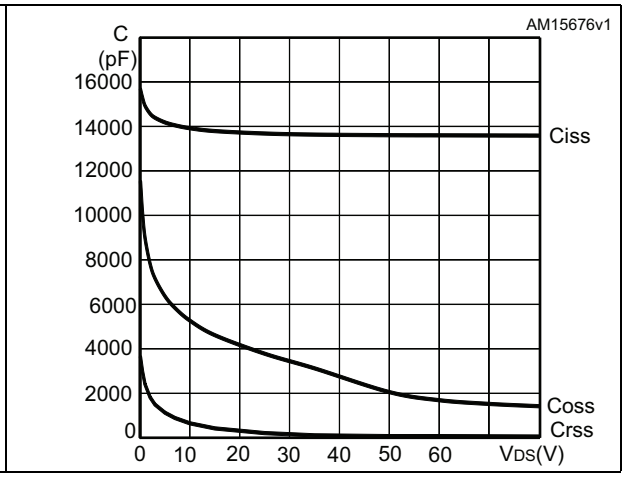


Figure 14. Source-drain diode forward characteristics

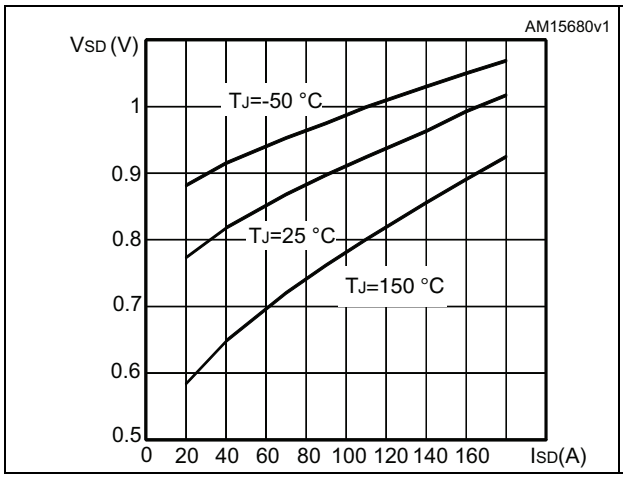


Figure 15. Normalized gate threshold voltage vs temperature

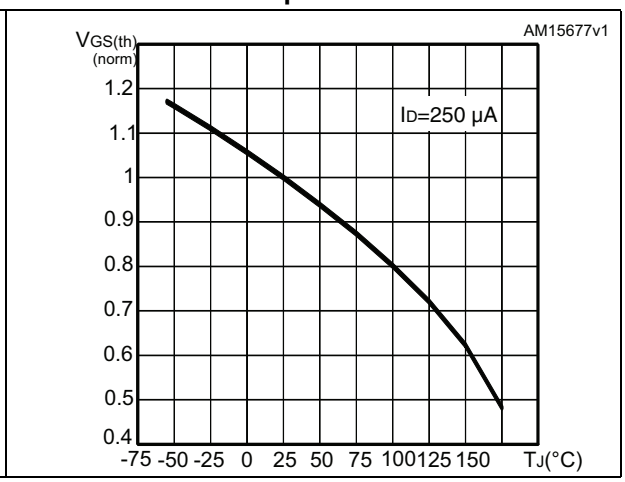


Figure 16. Normalized on-resistance vs temperature for H^2PAK-2

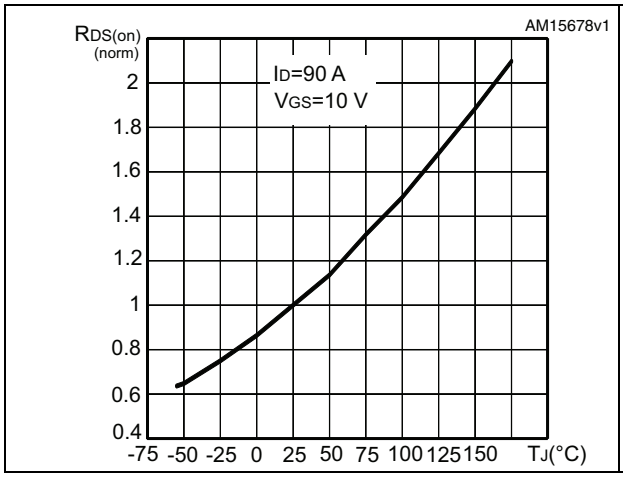
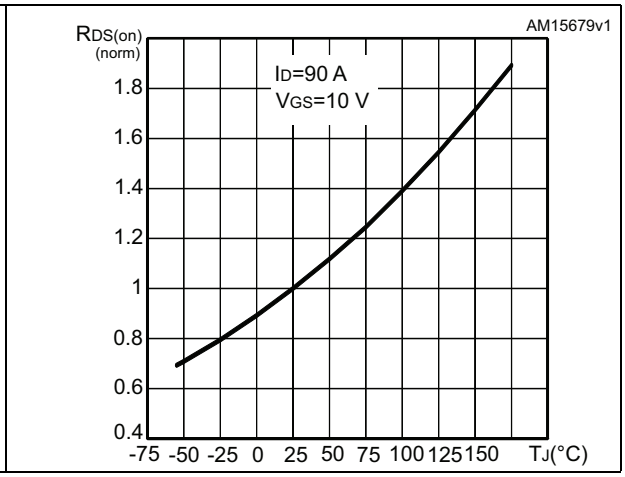


Figure 17. Normalized on-resistance vs temperature for TO-220



4 Test circuits

Figure 18. Switching times test circuit for resistive load

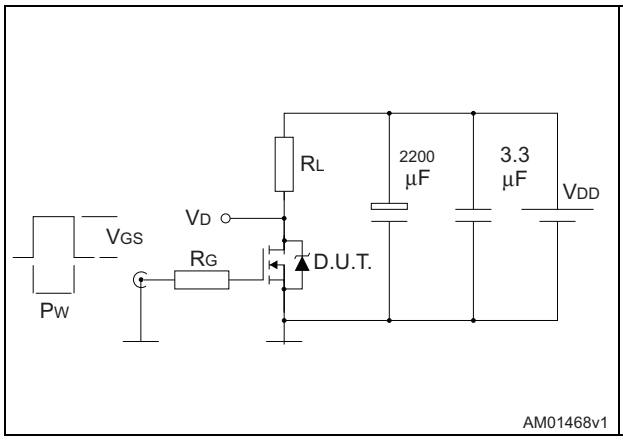


Figure 19. Gate charge test circuit

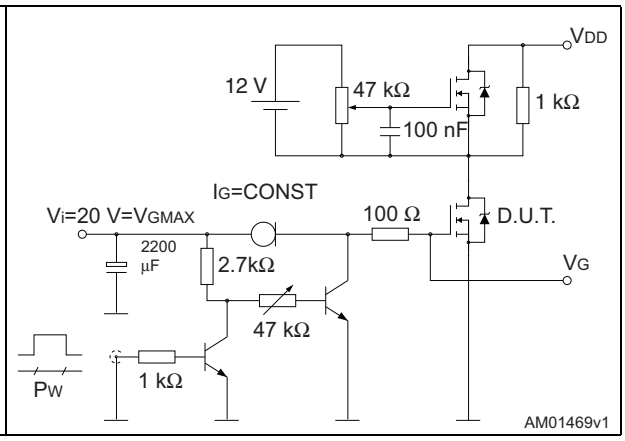


Figure 20. Test circuit for inductive load switching and diode recovery times

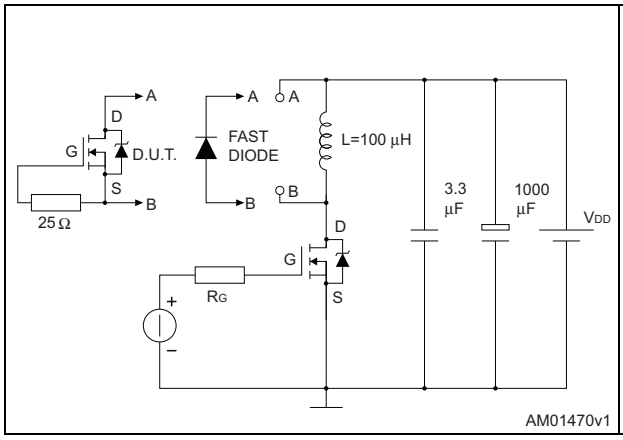


Figure 21. Unclamped inductive load test circuit

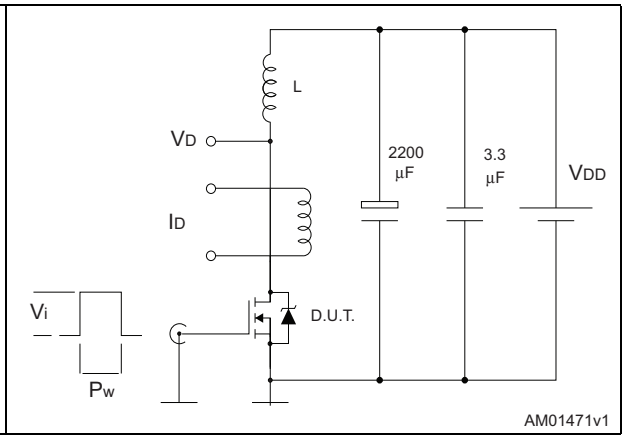


Figure 22. Unclamped inductive waveform

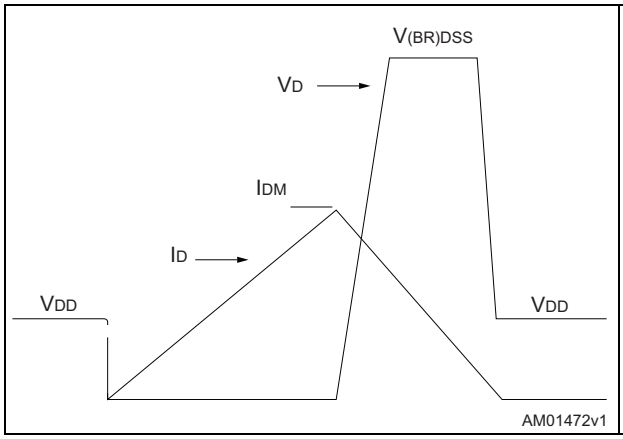
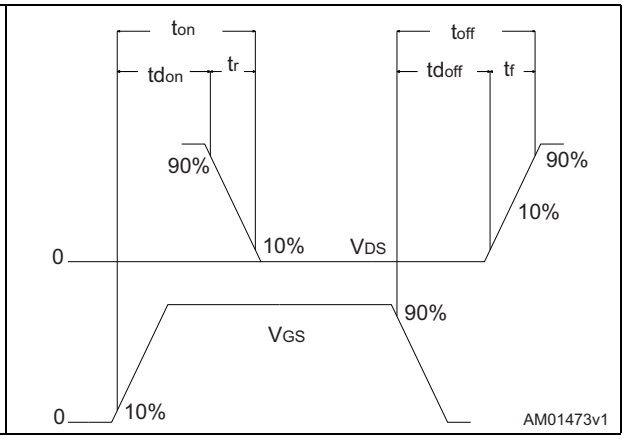


Figure 23. Switching time waveform



5 Package mechanical data

Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 24. H²PAK-2 drawing

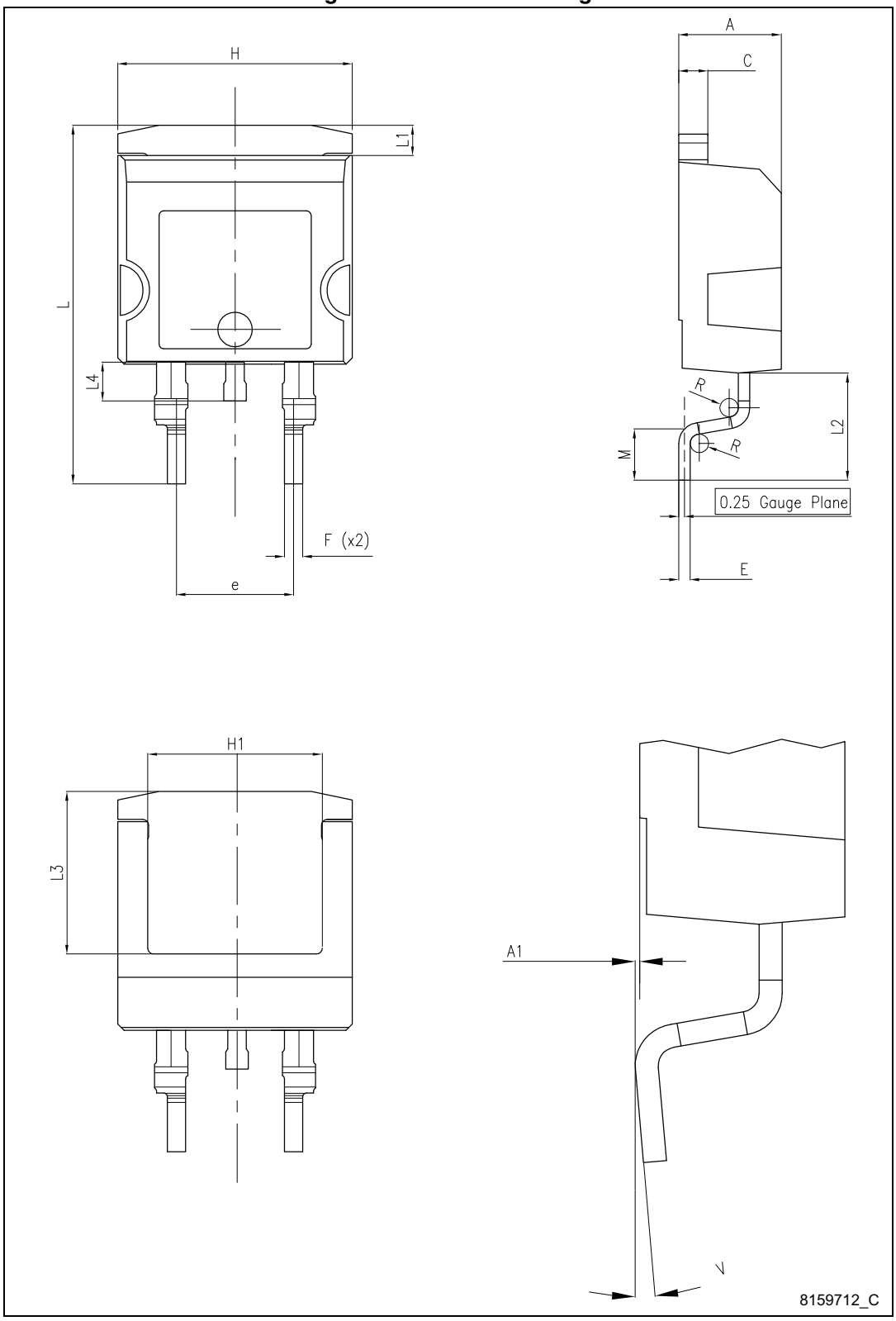


Figure 25. H²PAK-2 recommended footprint (in mm)

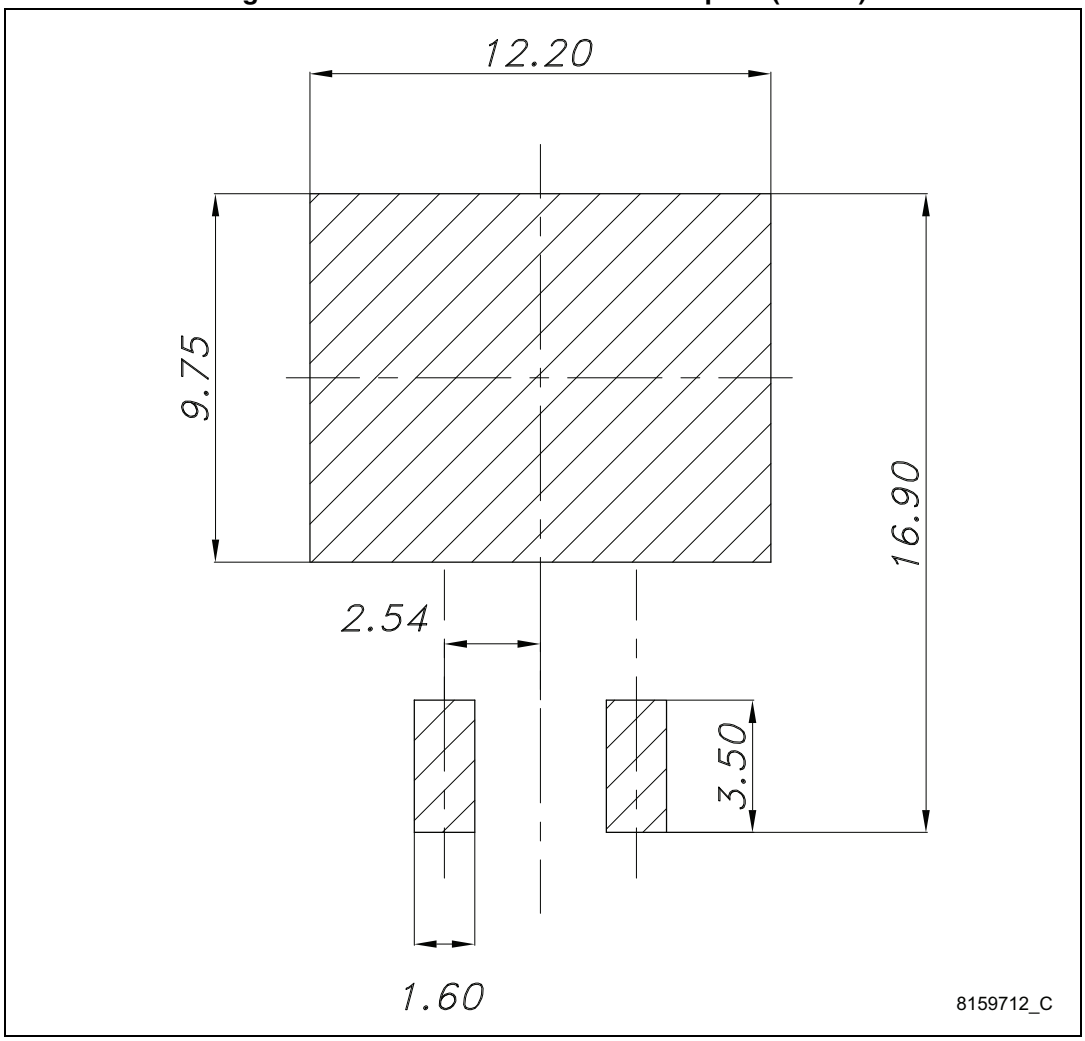
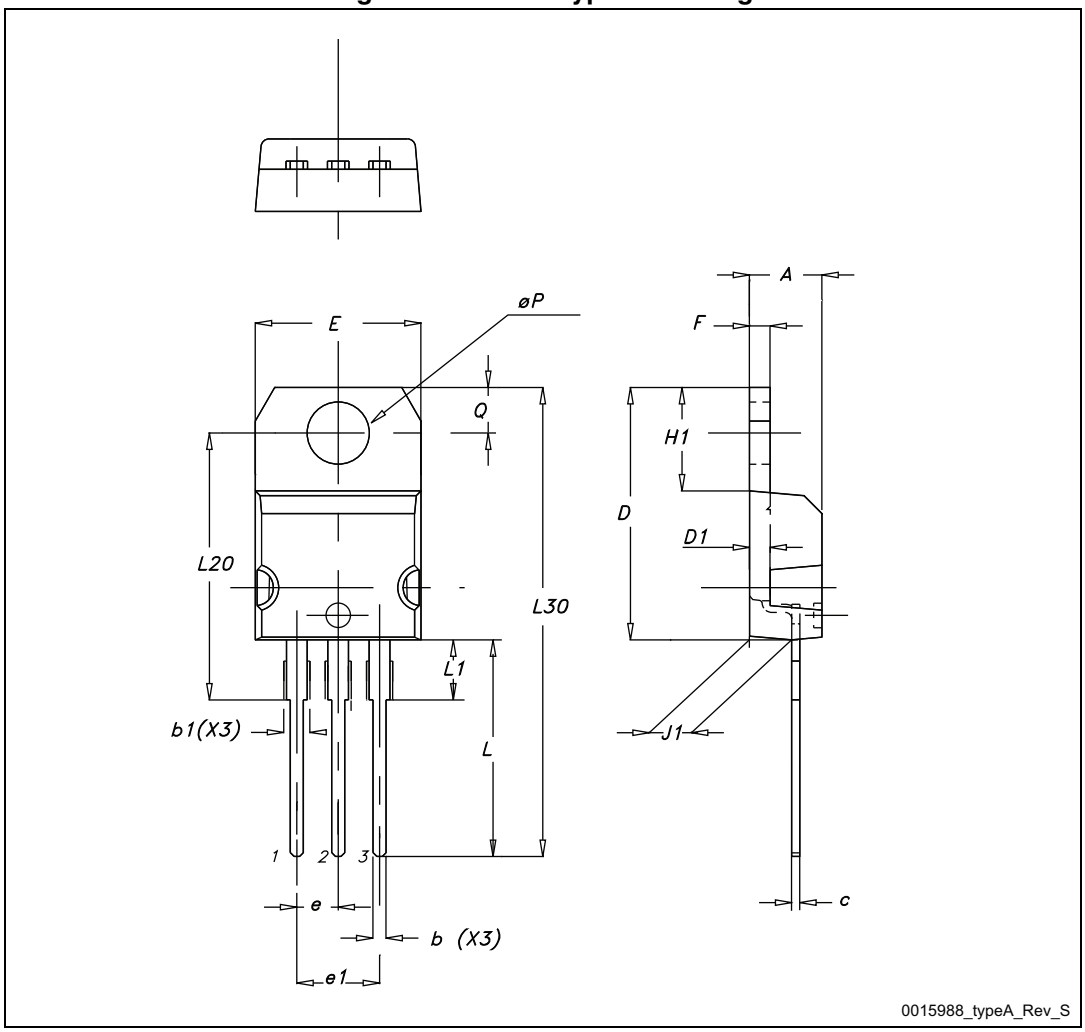


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing



6 Packaging information

Table 10. H²PAK-2 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape

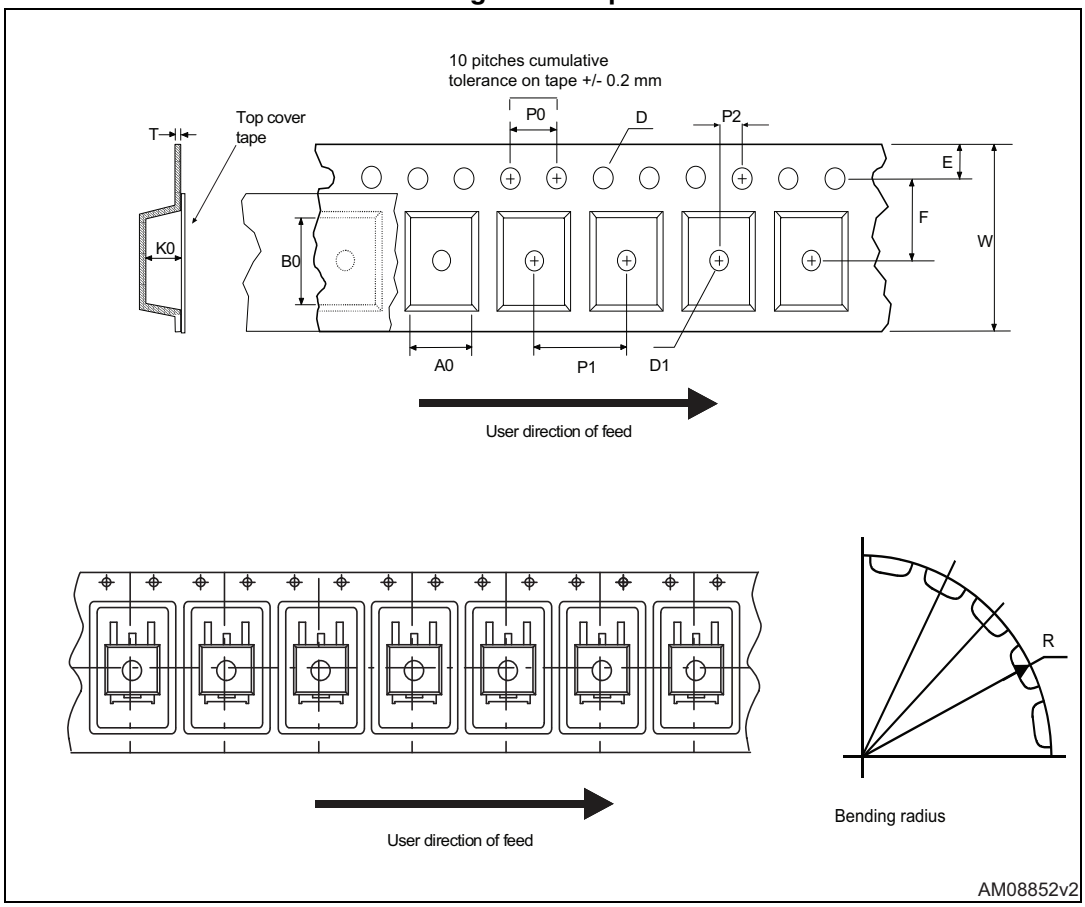
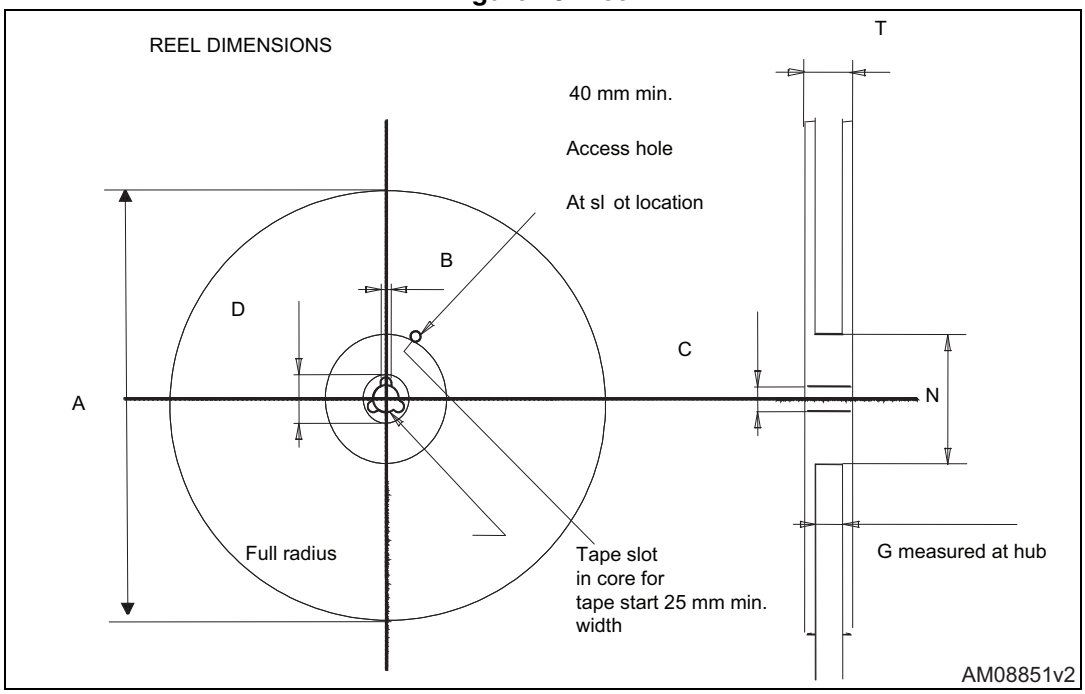


Figure 28. Reel



7 Revision history

Table 11. Document revision history

Date	Revision	Changes
16-Apr-2013	1	First release.

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