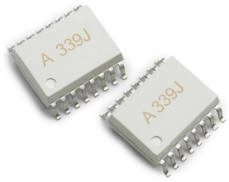
ACPL-339J

Dual-Output Gate Drive Optocoupler Interface with Integrated (V_{CE}) DESAT Detection, FAULT and UVLO Status Feedback

Data Sheet

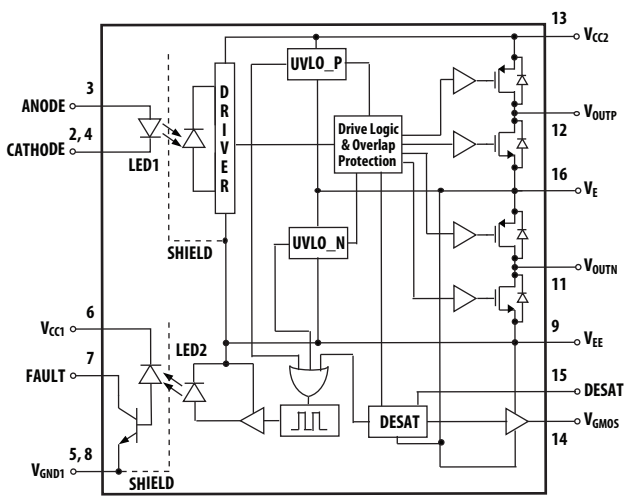


Description

The ACPL-339J is an advanced 1.0 A dual-output, easy-to-use, intelligent IGBT and Power MOSFET gate drive optocoupler interface. Uniquely designed to support MOSFET buffer of various current ratings, the ACPL-339J makes it easier for system engineers to support different system power ratings using one hardware platform by interchanging the MOSFET buffers and power IGBT/MOSFET switches. These changes can be made without redesigning the critical circuit isolation and short-circuit protection. This concept maximizes gate drive design scalability for motor control and power conversion applications ranging from low to high power ratings.

The ACPL-339J contains a AlGaAs LED. The LED is optically coupled to an integrated circuit with two power output stages with active timing control to prevent cross conduction at external MOSFET buffer. It is also integrated with features such as V_{CE} detection, under voltage lockout (UVLO), "soft" IGBT turn-off, and isolated open collector fault feedback to provide maximum design flexibility and circuit protection. The ACPL-339J has an insulation voltage of V_{IORM} = 1414 V_{peak} in IEC/EN/DIN EN 60747-5-5.

Functional Diagram



Features

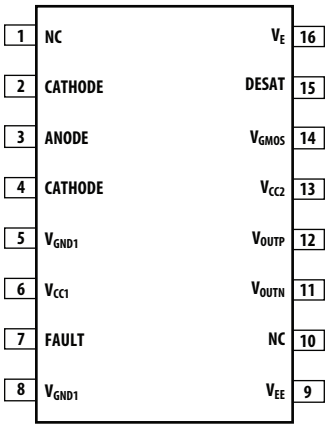
- Dual output drive for external NMOS and PMOS buffer
- 1.0 A minimum peak output current
- Active timing control to prevent cross conduction in MOSFET buffer
- IGBT desaturation detection
- Isolated DESAT and UVLO fault feedback
- Configurable "Soft" shutdown during fault
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis for positive and negative power supply
- 300 ns maximum propagation delay over temperature range.
- 6.0 mA to 10.0 mA Low LED input current
- 25 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Wide Operating V_{CC} Range: 15 to 30 Volts
- Industrial temperature range: -40° C to 105° C
- SO-16 package
- Safety Approval Pending
  - UL Recognized 5000 V_{RMS} for 1 min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1414 V_{peak}

Applications

- IGBT/Power MOSFET gate drive Interface
- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial Inverters
- Switching power supplies

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pin Description



Pin	Symbol	Description
1	NC	No connection
2	CATHODE	Cathode
3	ANODE	Anode
4	CATHODE	Cathode
5	V_{GND1}	Input ground
6	V_{CC1}	Positive input supply voltage. (3.3 V ± 5%, 5 V± 5%)
7	FAULT	Fault output. FAULT changes from logic low to high output: a) after T_{BLANK} (set by C_{BLANK} and the internal current source of 250 μA), once the voltage on the DESAT pin exceeding an internal reference voltage of 8 V (reference to V_E) b) UVLO condition
8	V_{GND1}	Input ground
9	V_{EE}	Output supply voltage.
10	NC	No connection
11	V_{OUTN}	Low side voltage output
12	V_{OUTP}	High side voltage output
13	V_{CC2}	Positive output supply voltage
14	V_{GMOS}	V_{GMOS} will switch from V_{EE} to V_E after DESAT is activated
15	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 8 V while the IGBT is on, FAULT and V_{GMOS} outputs are changed from logic low to high state.
16	V_E	Common (IGBT emitter) output supply voltage.

Ordering Information

ACPL-339J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

	Option					
Part number	RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-339J	-000E	SO-16	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

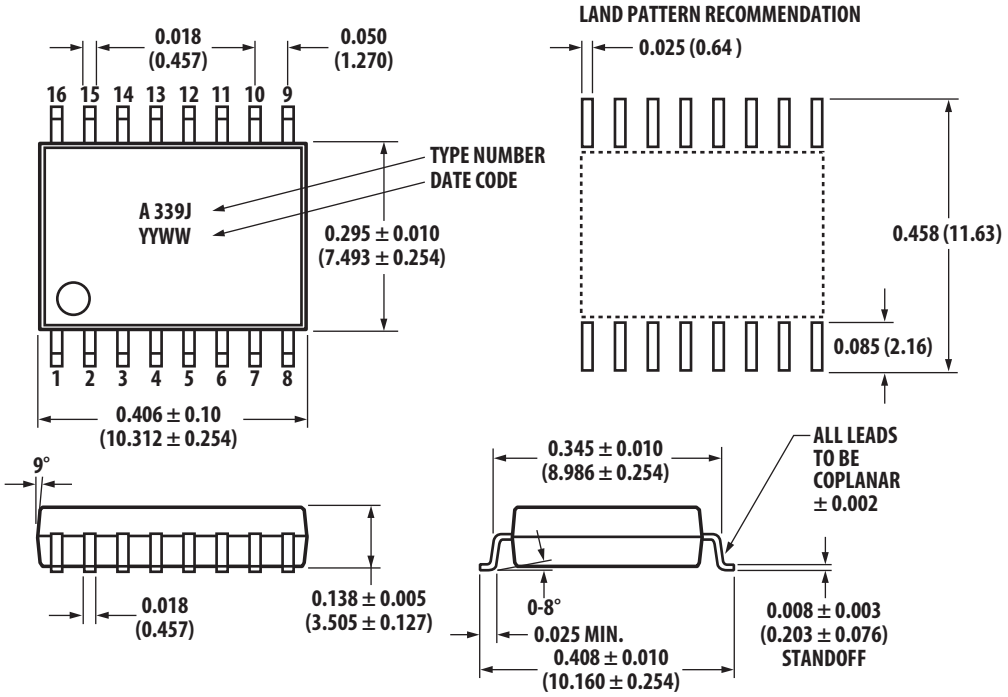
Example 1:

ACPL-339J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-339J 16-Lead Surface Mount Package



Dimensions in inches (millimeters)

Notes: Initial and continued variation in the color of the ACPL-339J's white mold compound is normal and does note affect device performance or reliability.

Floating Lead Protrusion is 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-339J is pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5

Maximum working insulation voltage V_{IORM} = 1414 V_{PEAK}

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 50000 V_{RMS}. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – IV	
for rated mains voltage ≤ 1000 V_{rms}		I – III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a** V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	400	mA
Output Power	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	W

* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

** Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-339J	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (< 1 μs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		5.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		5.5	A	2
Positive Input Supply Voltage	V_{CC1}	0	7	V	
FAULT Output Current	I_{FAULT}		8	mA	
FAULT Pin Voltage	V_{FAULT}	-0.5	V_{CC1}	V	
Total Output Supply Voltage	$(V_{CC2} – V_{EE})$	0	35	V	
Negative Output Supply Voltage	$(V_E – V_{EE})$	0	17	V	
Positive Output Supply Voltage	$(V_{CC2} – V_E)$	0	$35 – (V_E – V_{EE})$	V	
High Side Output Voltage	$V_{OUTP(PEAK)}$	$V_E – 0.5$	$V_{CC2} + 0.5$	V	
Low Side Output Voltage	$V_{OUTN(PEAK)}$	$V_{EE} – 0.5$	$V_E + 0.5$	V	
DESAT Voltage	V_{DESAT}	$V_E – 0.5$	$V_{CC2} + 0.5$	V	
V_{GMOS} Voltage	V_{GMOS}	$V_{EE} – 0.5$	$V_E + 0.5$	V	
Output IC Power Dissipation	P_O		600	mW	3
Input LED Power Dissipation	P_I		150	mW	4

Notes:
1. Derate linearly above 70° C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 μs
3. Derate linearly above 95° C free-air temperature at a rate of 20 mW/°C.
4. Derate linearly above 95° C free-air temperature at a rate of 4 mW/°C. The maximum LED junction temperature should not exceed 125° C.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	-40	105	°C	
Positive input supply voltage	V_{CC1}	3.3	5.5	V	
Total Output Supply Voltage	$(V_{CC2} – V_{EE})$	21	30	V	
Negative Output Supply Voltage	$(V_E – V_{EE})$	6	15	V	
Positive Output Supply Voltage	$(V_{CC2} – V_E)$	15	$30 – (V_E – V_{EE})$	V	
Input Current (ON)	$I_{F(ON)}$	6	10	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	

Table 5. Electrical Specifications (DC)

Unless otherwise noted, all typical values at T_A = 25° C, V_{CC1} = 3.3 V or 5 V, $V_{CC2} - V_E$ = 15 V, $V_E - V_{EE}$ = 8 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V_{OUTP} High Level Output Current	I_{OUTPH}	-1			A	$V_{CC2} - V_{OUTP} \leq 15$ V	3	1
V_{OUTP} Low Level Output Current	I_{OUTPL}	1			A	$V_{OUTP} - V_E \leq 15$ V	4	1
V_{OUTN} High Level Output Current	I_{OUTNH}	-1			A	$V_E - V_{OUTN} \leq 8$ V	3	1
V_{OUTN} Low Level Output Current	I_{OUTNL}	1			A	V_{OUTN} - $V_{EE} \leq 8$ V	4	1
V_{OUTP} High Level Output R_{DSON}	R_{OUTPH}		3.5	7	Ω	I_{OUTP} = -1 A, V_F = 0 V	3, 5	1
V_{OUTP} Low Level Output R_{DSON}	R_{OUTPL}		1.5	4	Ω	I_{OUTP} = 1 A, I_F = 8 mA	4, 6	1
V_{OUTN} High Level Output R_{DSON}	R_{OUTNH}		3.5	7	Ω	I_{OUTN} = -1 A, V_F = 0 V	3, 5	1
V_{OUTN} Low Level Output R_{DSON}	R_{OUTNL}		1.5	4	Ω	I_{OUTN} = 1 A, I_F = 8 mA	4, 6	1
V_{OUTP} High Level Output Voltage	V_{OUTPH}	V_{CC2} – 0.60	V_{CC2} – 0.30		V	I_{OUTP} = -100 mA, V_F = 0 V	1	2, 4, 5
V_{OUTP} Low Level Output Voltage	V_{OUTPL}		V_E + 0.14	V_E + 0.50	V	I_{OUTP} = 100 mA, I_F = 8 mA	2	
V_{OUTN} High Level Output Voltage	V_{OUTNH}	V_E – 0.60	V_E – 0.30		V	I_{OUTN} = -100 mA, V_F = 0 V	1	3, 4, 5
V_{OUTN} Low Level Output Voltage	V_{OUTNL}		V_{EE} + 0.12	V_{EE} + 0.60	V	I_{OUTN} = 100 mA, I_F = 8 mA	2	
V_{GMOS} High Level Output Current	I_{OUTGH}	-80			mA	$V_E - V_{GMOS} \leq 8$ V, I_F = 8 mA, DESAT = Open		
V_{GMOS} Low Level Output Current	I_{OUTGL}	80			mA	$V_{GMOS} - V_{EE} \leq 8$ V, V_F = 0 V, DESAT = Open		
V_{GMOS} High Level Output R_{DSON}	R_{OUTGH}		22	30	Ω	I_{OUTG} = -80 mA, I_F = 8 mA	7	
V_{GMOS} Low Level Output R_{DSON}	R_{OUTGL}		6	10	Ω	I_{OUTN} = 80 mA, V_F = 0 V, DESAT = Open	8	
V_{GMOS} High Level Output Voltage	V_{OUTGH}		V_E		V	I_{OUTG} = 0 mA, I_F = 8 mA, DESAT = Open		
V_{GMOS} Low Level Output Voltage	V_{OUTGL}		V_{EE}		V	I_{OUTN} = 0 mA, V_F = 0 V, DESAT = Open		
High Level Output Supply Current (V_{CC2})	I_{CC2H}		8.5	12	mA	V_F = 0 V, No Load	9, 10	
Low Level Output Supply Current (V_{CC2})	I_{CC2L}		8.5	12	mA	I_F = 8 mA, No Load,	9, 10	
High Level Output Supply Current (V_{EE})	I_{EEH}		8	11	mA	V_F = 0 V, No Load	11, 12	
Low Level Output Supply Current (V_{EE})	I_{EEL}		8	11	mA	I_F = 8 mA, No Load	11, 12	
Threshold Input Current Low to High	I_{FLH}		1.3	5	mA	No Load, $V_{OUTP} - V_E < 5$ V, $V_{OUTN} - V_{EE} < 1$ V	13, 14	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V	No Load, $V_{OUTP} - V_E > 5$ V, $V_{OUTN} - V_{EE} > 1$ V		

Table 5. Electrical Specifications (DC) (continued)

Unless otherwise noted, all typical values at T_A = 25° C, V_{CC1} = 3.3 V or 5 V, $V_{CC2} - V_E$ = 15 V, $V_E - V_{EE}$ = 8 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 8 mA		
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C	I_F = 8 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 mA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO_P Threshold, V_{CC2}-V_E	V_{UVLOP+}	12	13	14	V	I_F = 8 mA, $V_{OUTP} - V_E$ < 5 V	31	2, 5, 6
	V_{UVLOP-}	11	12	13	V	I_F = 8 mA, $V_{OUTP} - V_E$ > 5 V	31	3, 5, 7
UVLO_P Hysteresis, V_{CC2}-V_E	V_{UVLOP+} - V_{UVLOP-}		1		V			
UVLO_N Threshold, V_E-V_{EE}	V_{UVLON+}	4.8	5.4	6	V	I_F = 8 mA, $V_{OUTN} - V_{EE}$ < 1 V	31	2, 5, 8
	V_{UVLON-}	4.7	5	5.7	V	I_F = 8 mA, $V_{OUTN} - V_{EE}$ > 1 V	31	3, 5, 9
UVLO_N Hysteresis, V_E-V_{EE}	V_{UVLON+} - V_{UVLON-}		0.3		V			
DESAT Threshold	V_{DESAT}	7.5	8	9	V	$V_{CC2} - V_E > V_{UVLOP-}$ and $V_E - V_{EE} > V_{UVLON-}$	15	5
Blanking Capacitor Charging Current	I_{CHG}	0.15	0.25	0.36	mA	V_{DESAT} = 2 V	16	5, 10
DESAT Low Voltage when Blanking Capacitor Discharge	V_{DSCHG}		1.1	3	V	I_{DSCHG} = 10 mA		5, 10
FAULT Logic Low Output Voltage	V_{FAULTL}		0.10	0.25	V	V_{DESAT} = 0 V, R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 5 V or 3.3 V		
FAULT Logic High Output Voltage	V_{FAULTH}		V_{CC1}		V	DESAT = Open, R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 5 V or 3.3 V		
FAULT Logic Low Output Current	I_{FAULTL}		0.25		mA	V_{FAULT} = 0.15 V, V_{CC1} = 5 V or 3.3 V		
FAULT Logic High Output Current	I_{FAULTH}		0.2	1	µA	$V_{FAULT} = V_{CC1}$ = 5 V or 3.3 V		

Notes:
1. Output is sourced at -1.0 A / 1.0 A with a maximum pulse width = 10 µs.
2. 15 V is the recommended minimum operating positive supply voltage ($V_{CC2} - V_E$) to ensure adequate margin in excess of the maximum V_{UVLOP+} threshold of 13.5 V. For High Level Output Voltage testing, V_{OUTP} is measured with a 50 µs pulse load current. When driving capacitive loads, V_{OUTP} will approach V_{CC} as I_{OUTPH} approaches zero units.
3. 6.6 V is the recommended minimum operating positive supply voltage ($V_E - V_{EE}$) to ensure adequate margin in excess of the maximum V_{UVLON+} threshold of 5.6 V. For High Level Output Voltage testing, V_{OUTN} is measured with a 50 µs pulse load current. When driving capacitive loads, V_{OUTN} will approach V_E as I_{OUTNH} approaches zero units.
4. Maximum pulse width = 1.0 ms.
5. Once V_{OUTP} is allowed to go low ($V_{CC2} - V_E > V_{UVLOP+}$) and V_{OUTN} is allowed to go high ($V_E - V_{EE} > V_{UVLON+}$), the DESAT detection feature of the ACPL-339J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once $V_{CC2} - V_E > V_{UVLOP+}$ and $V_E - V_{EE} > V_{UVLON+}$, DESAT will remain functional until $V_{CC2} - V_E < V_{UVLOP-}$ or $V_E - V_{EE} < V_{UVLON-}$,. Thus, the DESAT detection and UVLO features of the ACPL-339J work in conjunction to ensure constant IGBT protection.
6. This is the "increasing" (i.e. turn-on or "positive going" direction) of $V_{CC2} - V_E$.
7. This is the "decreasing" (i.e. turn-off or "negative going" direction) of $V_{CC2} - V_E$.
8. This is the "increasing" (i.e. turn-on or "positive going" direction) of $V_{EE} - V_E$.
9. This is the "decreasing" (i.e. turn-ff or "negative going" direction) of $V_{EE} - V_E$.
10. See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.

Table 6. Switching Specifications (AC)

Unless otherwise noted, all typical values at T_A = 25° C, V_{CC1} = 3.3 V or 5 V, and $V_{CC2} - V_E$ = 15 V, $V_E - V_{EE}$ = 8 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	100	180	300	ns	$C_P = C_N$ = 4 nF, f = 20 kHz, Duty Cycle = 50%, I_F = 6 mA to 10 mA	17, 18, 30	1
Propagation Delay Time to Low Output Level	t_{PHL}	100	150	300	ns		17, 18, 30	1
Pulse Width Distortion	PWD	150	25	150	ns			2
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PLH} - t_{PHL}$)	-200		200	ns		36, 37	3
Propagation Delay Skew	t_{PSK}			170	ns			7
LED OFF to 90% of V_{OUTP}	t_{DP}	50	150	250	ns		17,18, 30	
LED ON to 10% of V_{OUTN}	t_{DN}	50	125	250	ns		17,18, 30	
Non-overlap Time Low to High	t_{NLH}		30		ns		25, 30	
Non-overlap Time High to Low	t_{NHL}		20		ns		25, 30	
10% to 90% Rise Time on V_{OUTP}	t_{PR}		40		ns	$C_P = C_N$ = 4 nF, f = 20 kHz, Duty Cycle = 50%, I_F = 8 mA	30	
90% to 10% Fall Time on V_{OUTP}	t_{PF}		40		ns		30	
10% to 90% Rise Time on V_{OUTN}	t_{NR}		40		ns		30	
90% to 10% Fall Time on V_{OUTN}	t_{NF}		30		ns		30	
Delay time from DESAT threshold to 50% of High V_{GMOS}	t_1		250	500	ns	$C_P = C_N$ = 4 nF, C_G = 1 nF, f = 250 Hz, Duty Cycle = 50%, I_F = 8 mA	19, 22, 28, 29	
Delay time from DESAT threshold to 50% of High V_{OUTP}	t_2		250	500	ns		19, 28, 29	
Delay time from DESAT threshold to 50% of High FAULT	t_3		8.5	11	µs	R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 3.3 V or 5 V, f = 250 Hz, Duty Cycle = 50%, I_F = 8 mA	20, 28, 29	
Delay from 50% of V_{GMOS} to 50% of V_{OUTN}	t_4		11		ns	$C_P = C_N$ = 4 nF, C_G = 1 nF, f = 250 Hz, Duty Cycle = 50%, I_F = 8 mA	21, 23, 28, 29	
Mute time	t_{MUTE}	0.75	1	1.5	ms	f = 700 Hz, Duty Cycle = 50%, I_F = 8 mA	24, 28, 29	4
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	35		kV/µs	T_A = 25° C, V_{CM} = 1500 V, V_{CC1} = 5 V, C_F = 1 nF, R_F = 10 kΩ, I_F = 8 mA with split resistors		5
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	35		kV/µs	T_A = 25° C, V_{CM} = 1500 V, V_{CC1} = 5 V, C_F = 1 nF, R_F = 10 kΩ, V_F = 0 V		6

Notes:

1. This load condition approximates the gate load of a 60V/5A MOSFET
2. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
3. The difference between t_{PHL} and t_{PLH} between any two ACPL-339J parts under the same test conditions.
4. Auto Reset: This is the minimum amount of time when V_{OUTP} will be asserted high, V_{OUTN} asserted low, V_{GMOS} asserted high and FAULT asserted high, after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
5. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_{OUTP} - V_E$ > 12 V, $V_{OUTN} - V_{EE}$ > 5 V or FAULT > 2 V). A 1 nF and a 10 kΩ pull-up resistor is needed in fault detection mode.
6. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_{OUTP} - V_E$ < 1.0 V, $V_{OUTN} - V_{EE}$ < 1.0 V or FAULT < 0.8 V).
7. t_{PSK} is equal to the worst-case difference in t_{PHL} or t_{PLH} that will be seen between units under the same test condition.

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{rms}	RH < 50%, t = 1 min., T_A = 25° C		1, 2
Input-Output Resistance	R_{I-O}		> 10^9		W	V_{I-O} = 500 V		2
Input-Output Capacitance	C_{I-O}		1.3		pF	freq =1 MHz		

Notes
1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.
2. Device considered a two-terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.

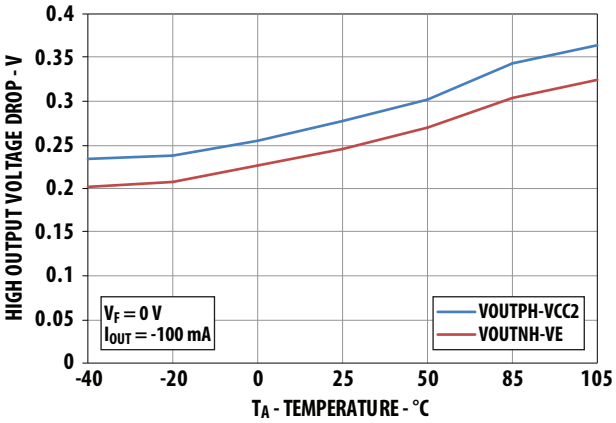


Figure 1. V_{OUTPH}/V_{OUTNH} vs. temperature

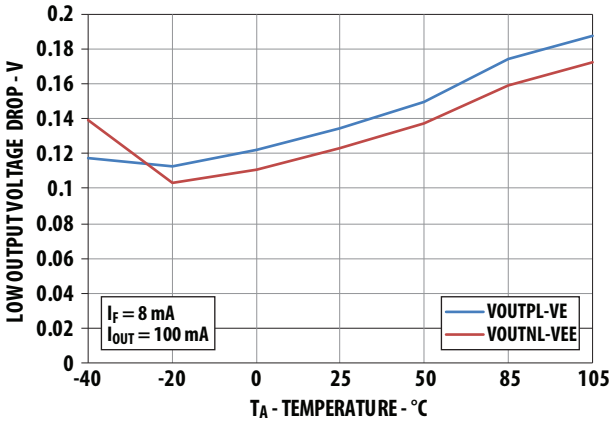


Figure 2. V_{OUTPL}/V_{OUTNL} vs. temperature

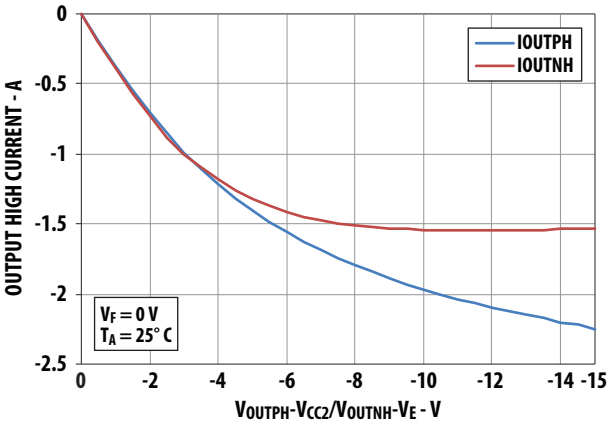


Figure 3. I_{OUTPH}/I_{OUTNH} vs.V_{OUTPH}/V_{OUTNH}

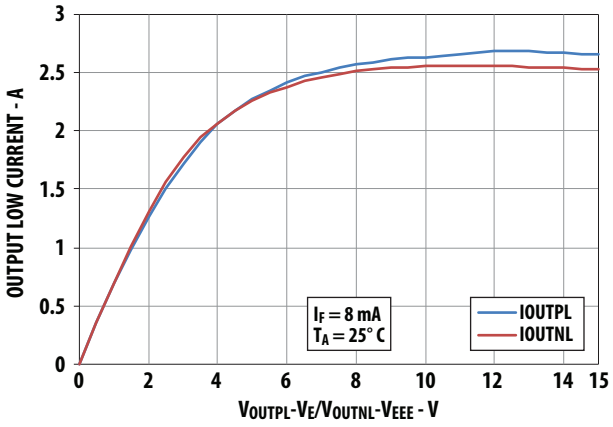


Figure 4. I_{OUTPL}/I_{OUTNL} vs.V_{OUTPL}/V_{OUTNL}

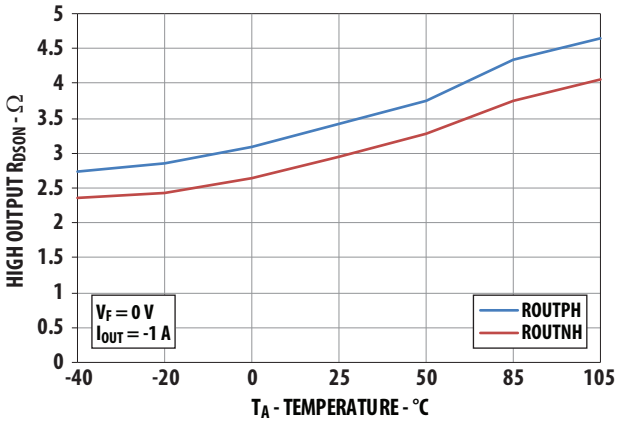


Figure 5. R_{OUTPH}/R_{OUTNH} vs. temperature

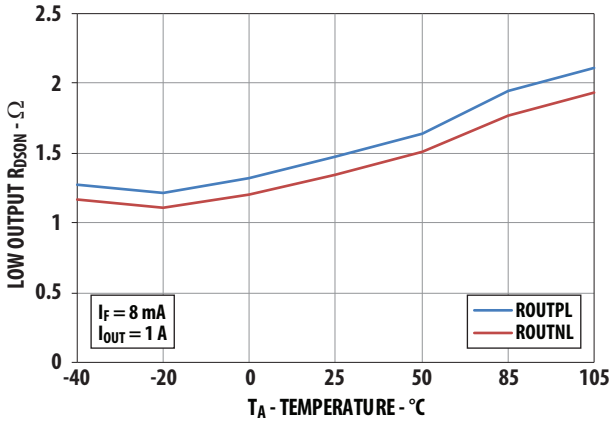


Figure 6. R_{OUTPL}/R_{OUTNL} vs. temperature

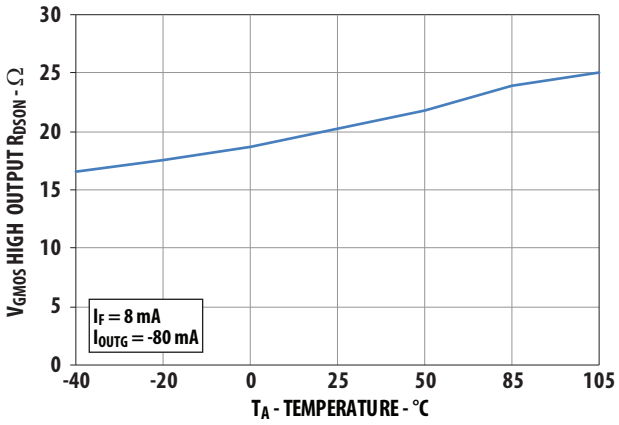


Figure 7. R_{OUTGH} vs. temperature

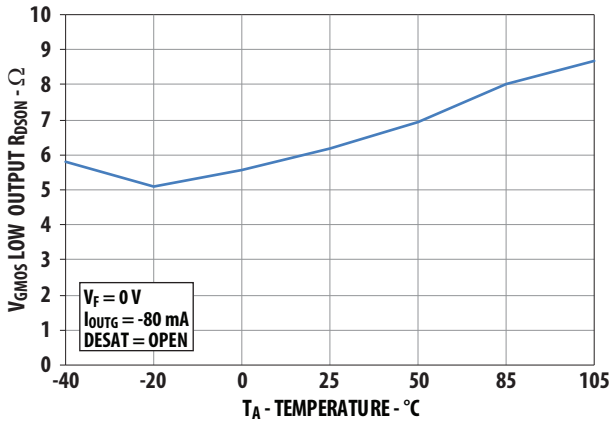


Figure 8. R_{OUTGL} vs. temperature

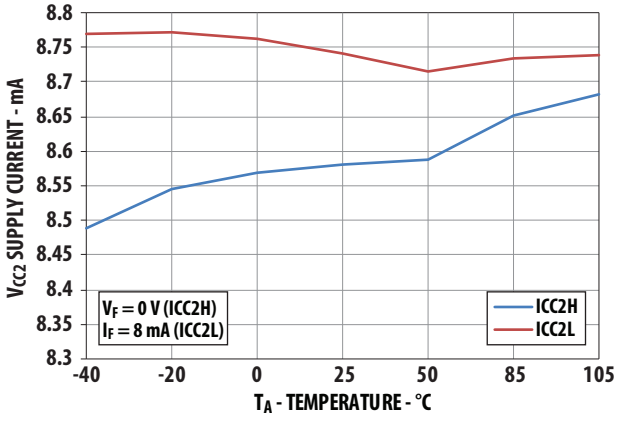


Figure 9. I_{CC2} vs. temperature

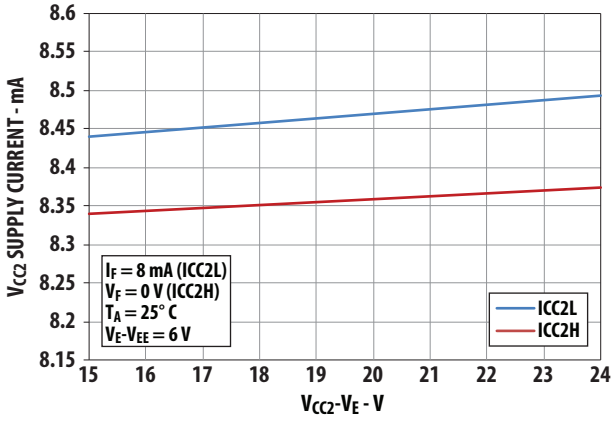


Figure 10. I_{CC2} vs. V_{CC2}

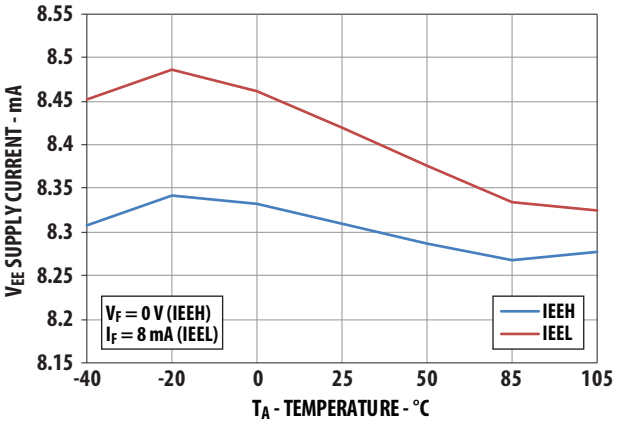


Figure 11. I_{EE} vs. temperature

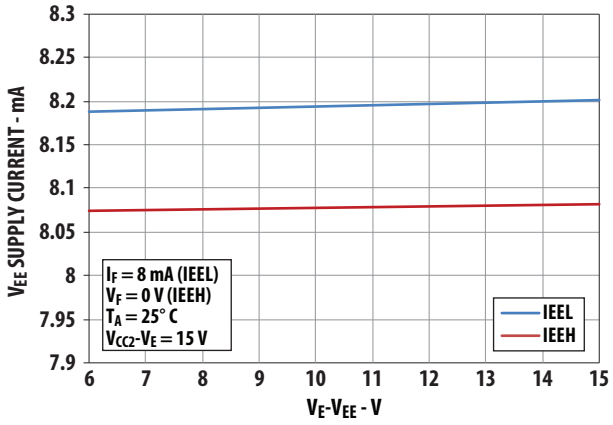


Figure 12. I_{EE} vs. V_{EE}

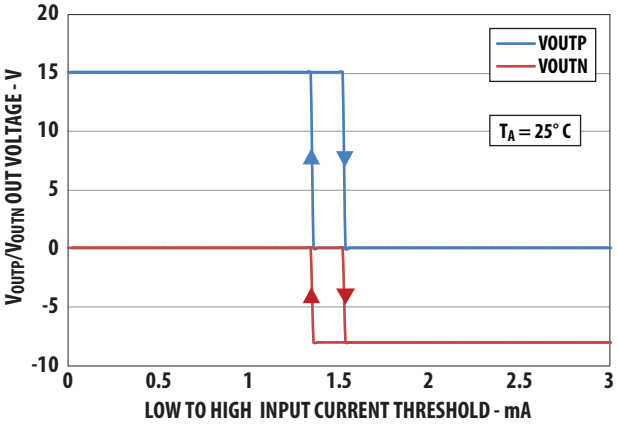


Figure 13. V_{OUTPH}/V_{OUTNH} vs. I_{FLH}

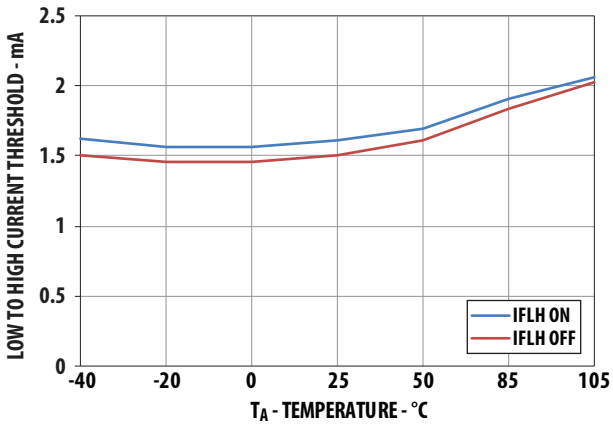


Figure 14. I_{FLH} vs. temperature

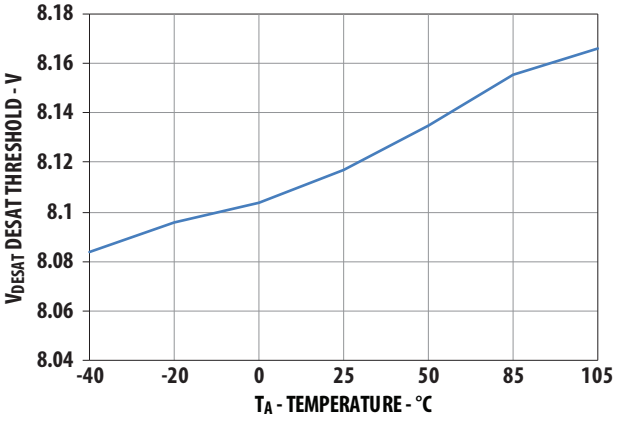


Figure 15. V_{DESAT} vs. temperature

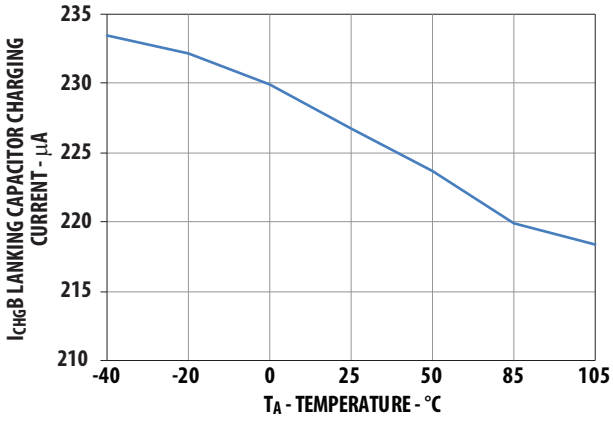


Figure 16. I_{CHG} vs. temperature

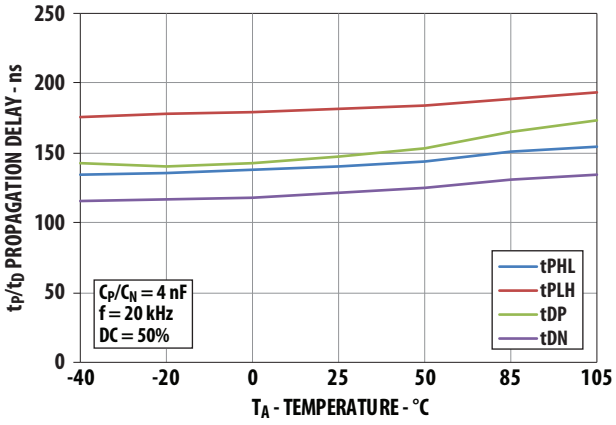


Figure 17. t_P /t_D vs. temperature

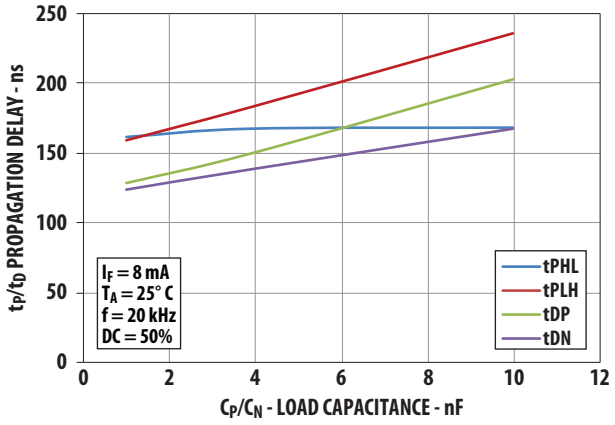


Figure 18. t_P /t_D vs. C_P/C_N

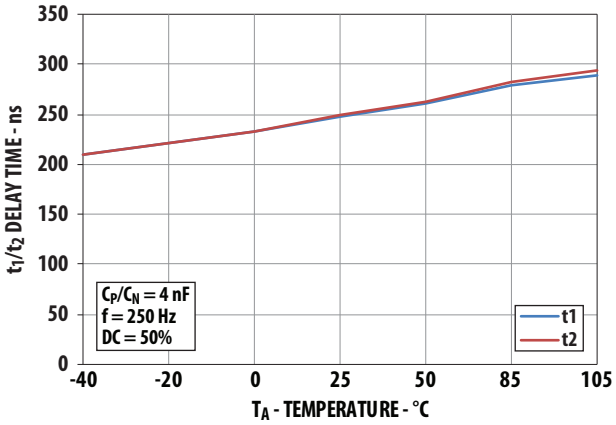


Figure 19. t_1 /t_2 vs. temperature

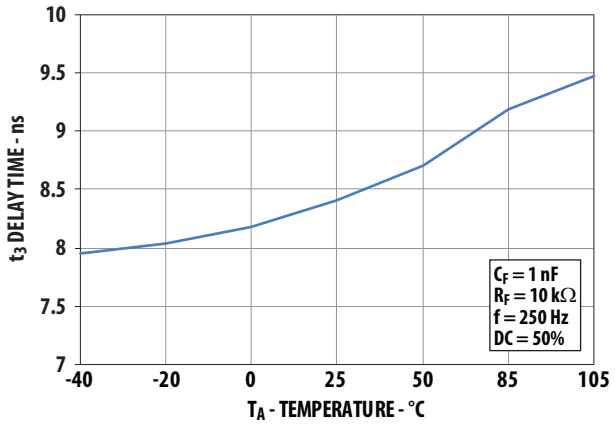


Figure 20. t_3 vs. temperature

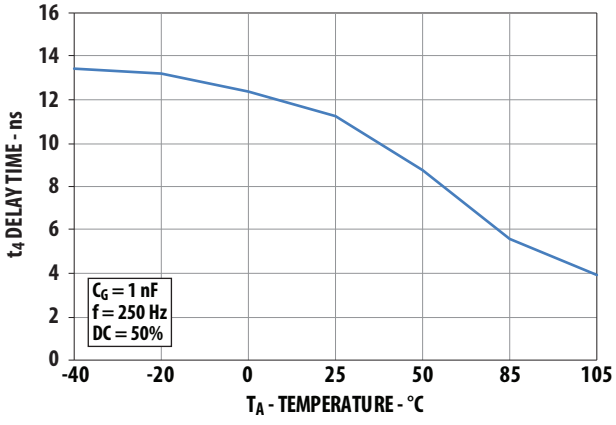


Figure 21. t_4 vs. temperature

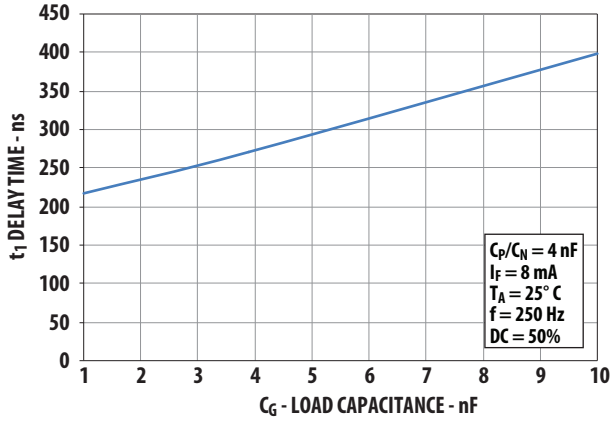


Figure 22. t_1 vs. C_G

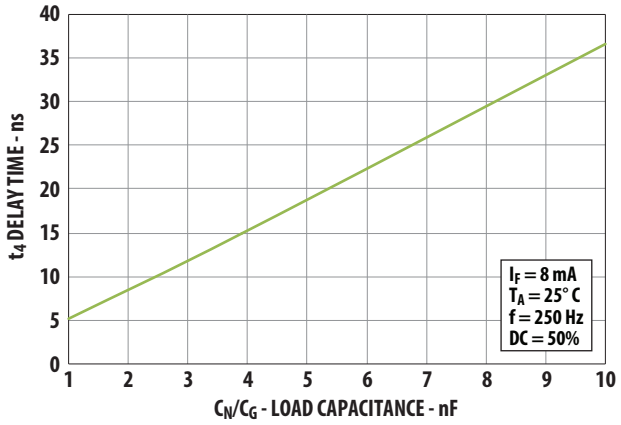


Figure 23. t_4 vs. C_N /C_G

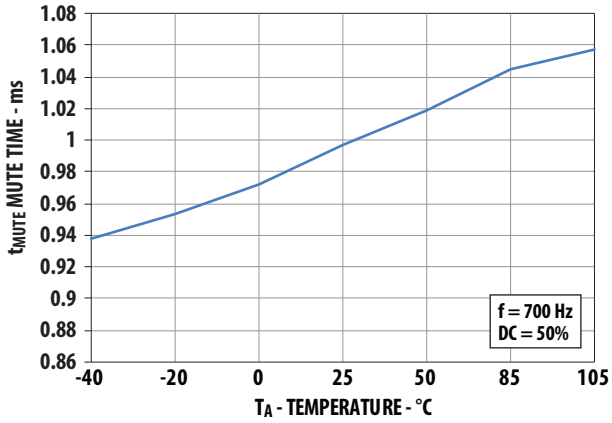


Figure 24. t_{MUTE} vs. temperature

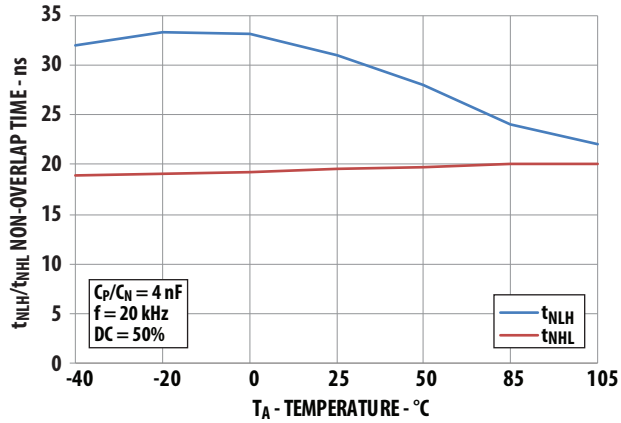


Figure 25. t_{NLH}/t_{NHL} vs. temperature

Applications Information

Product Overview Description

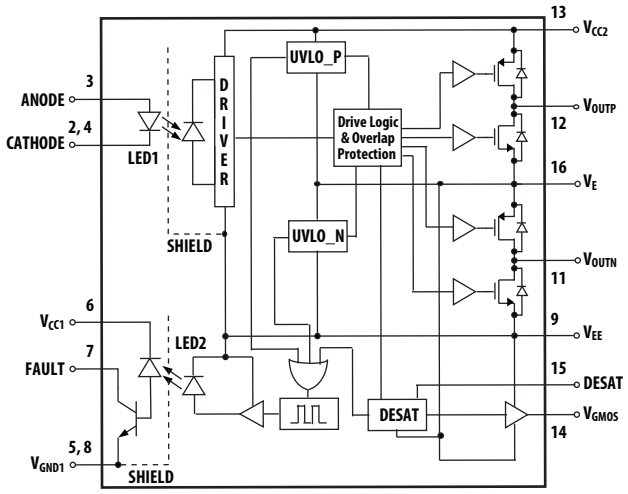
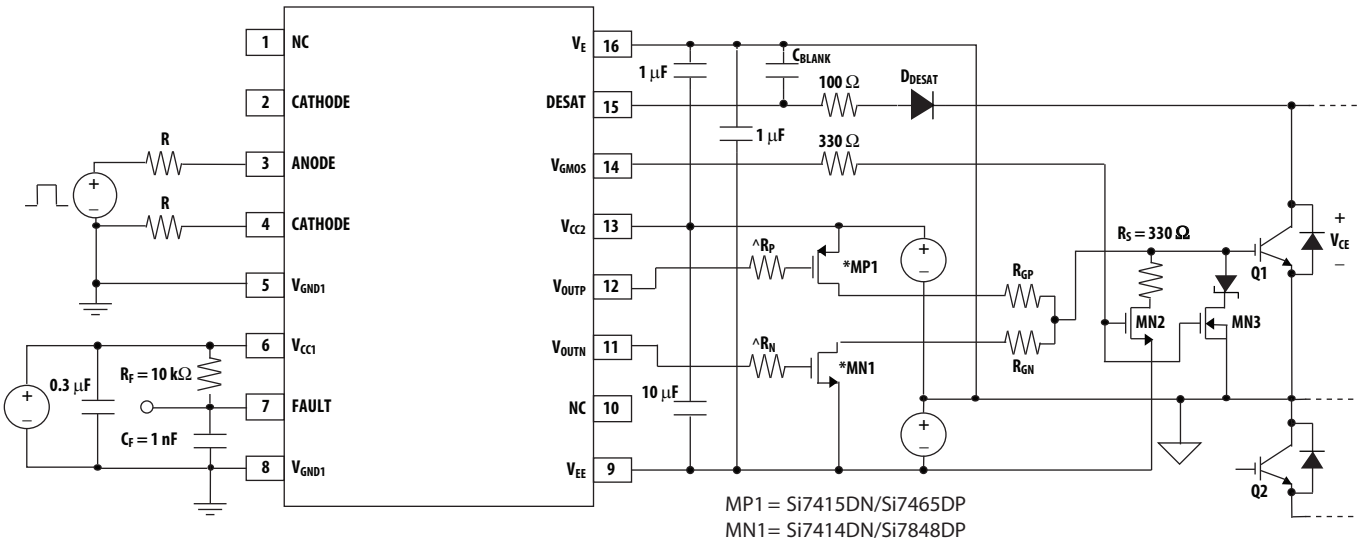


Figure 26. Block Diagram of ACPL-339J

Recommended Application Circuit



MP1 = Si7415DN/Si7465DP
MN1= Si7414DN/Si7848DP
MN2= Si2318
MN3= BSP149
* MP1 and MN1 equivalent C_{LOAD} to be < 15 nF
^ R_P and R_N is not required unless capacitive loading of MP1 or MN1 draws > 4 A of peak current.

Figure 27. Typical de-saturation protected gate drive circuit, non-inverting

Output Control

The outputs (V_{OUTP}, V_{OUTN}, V_{GMOS} and FAULT) of the ACPL-339J are controlled by the combination of I_F, UVLO and DESAT conditions. Once UVLO_P and UVLO_N is not active (V_{CC2} - V_E > V_{UVLOP+}, V_E - V_{EE} > V_{UVLON+}), V_{OUTP} is allowed to go low and V_{OUTN} is allowed to go high. Thereafter, the DESAT (pin 15) detection feature of the ACPL-339J will be the primary source of IGBT/MOSFET protection. DESAT will remain functional until V_{CC2} - V_E is decreased below V_{UVLOP-} or V_E - V_{EE} is decreased below V_{UVLON-}. Thus, the DESAT detection and UVLO features of the ACPL-339J work alternatively to ensure constant IGBT/MOSFET protection.

I_F	UVLO_P and UVLO_N	DESAT Function	Pin 7 (FAULT) Output	V_{OUTP}	V_{OUTN}	V_{GMOS}
X	Active	Not Active	V_{CC1}	V_{CC2}	V_E	V_E
ON	Not Active	Active (with DESAT fault)	V_{CC1}	V_{CC2}	V_{EE}	V_E
ON	Not Active	Active (no DESAT fault)	V_{GND1}	V_E	V_{EE}	V_{EE}
OFF	Not Active	Not Active	V_{GND1}	V_{CC2}	V_E	V_{EE}

Description of Operation during DESAT Fault Condition

The DESAT pin monitors the IGBT Vce voltage. The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the DESAT blanking time, is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor. The nominal blanking time is calculated in terms of external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as $T_{BLANK} = C_{BLANK} \times V_{DESAT}/I_{CHG}$. The nominal blanking time with the recommended 100 pF capacitor is 100 pF * 8 V/250 μA = 3.2 μsec. The capacitance value can be scaled slightly to adjust the blanking time, though a value smaller than 100 pF is not recommended. This nominal blanking time also represents the longest time it will take for the ACPL-339J to respond to a DESAT fault condition. Once DESAT fault is detected and after T_{BLANK} time, both V_{OUTP} and V_{OUTN} will turn off the respective external MP1 and MN1 and V_{GMOS} switches from low to high, turning on an external MN2 pull down device, in order to 'softly' turn-off the IGBT. Also activated is an internal feedback channel which brings the FAULT output from low to high for the purpose of notifying the micro-controller of the fault condition.

Once fault is detected, the output will be muted for T_{MUTE} time. All input LED signals will be ignored during the mute period to allow the driver to completely soft shut down the IGBT. The fault is auto-reset upon the 1ms (typical) mute time (T_{MUTE}) timeout or upon LED INPUT high to low transition, whichever is later. In this way, there is a minimum timeout but also the flexibility of lengthening the timeout freely. See Figure 28 and 29.

Soft IGBT Shut Down during Fault Condition

When a DESAT fault is detected, V_{GMOS} switches from low to high, turning on an external MN2 pull down device. MN2 slowly discharges the IGBT gate at a decay rate corresponding to the RC constant of R_S and C_{IN} (IGBT input capacitance). Based on a R_S of 330 Ω and C_{IN} of 10 nF, the entire soft shut down will decay in 4.8 * 330 Ω * 10 nF = 15.8 μs. Soft shut down prevents fast changes in the collector current that can cause damaging voltage spikes due to lead and wire inductance.

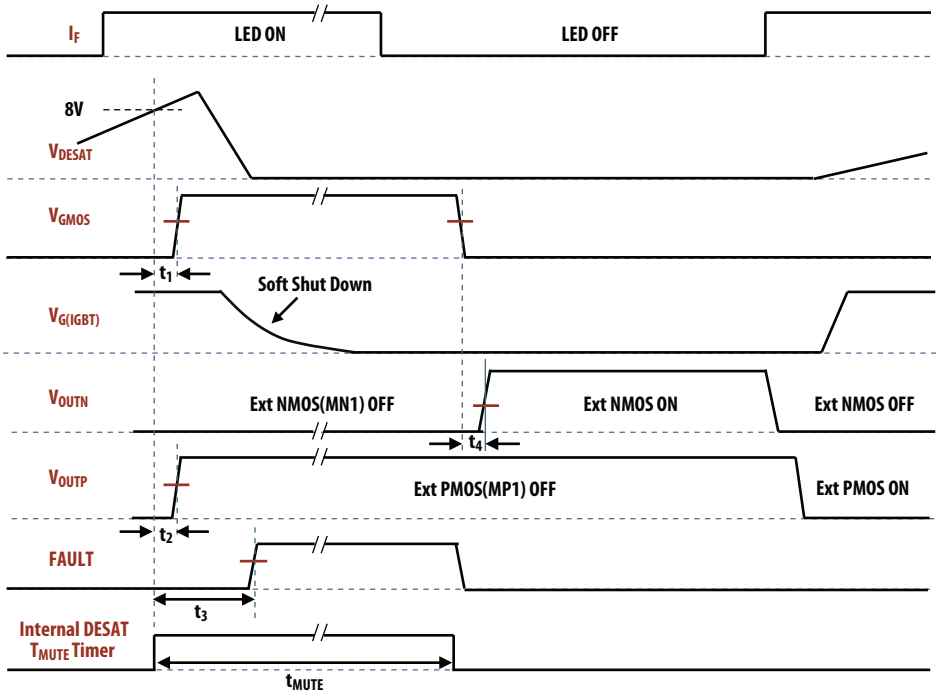


Figure 28. DESAT Fault State Timing Diagram with LED turn OFF before the T_{MUTE} timeout

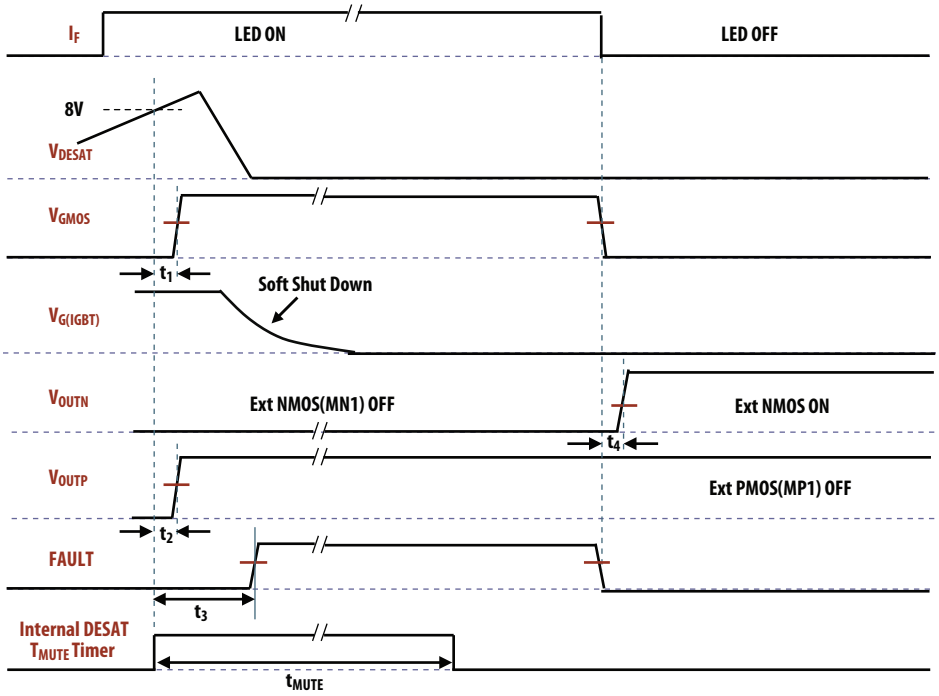


Figure 29. Desat Fault State Timing Diagram with LED OFF after the T_{MUTE} timeout

Timing Diagram & Cross-Conduction Scheme

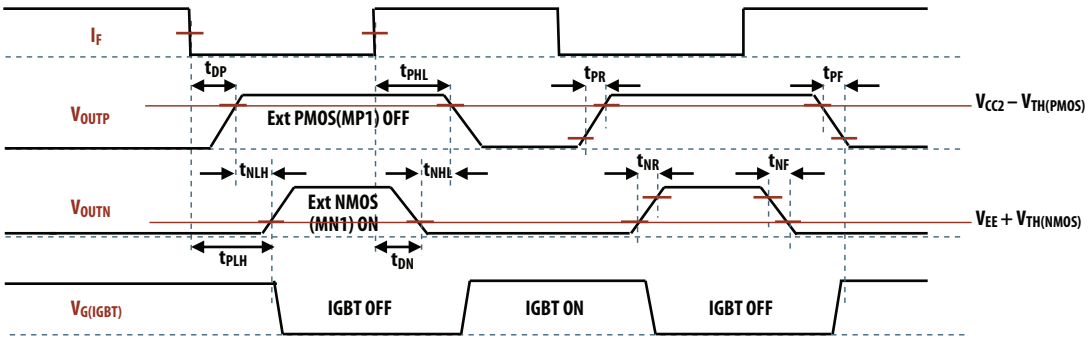


Figure 30. Timing diagram and Cross Conduction Scheme

The MOS Driver monitors V_{OUTP} & V_{OUTN} to detect for V_{CC2}-V_{OUTP} or V_{OUTN}-V_{EE} equals $V_{TH(MOS)}$ during the respective external MOSFET's turn-off transition. Upon detection, the complimentary V_{OUT} is turned on after some inherent delay t_{NLH}/t_{NHL}.

Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACPL-339J monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT from low voltage bias. ACPL-339J has two UVLO logic blocks, UVLO_P and UVLO_N to control the V_{OUTP} and V_{OUTN} respectively. The UVLO control logic takes precedence over input I_F and DESAT. In another words, I_F and DESAT are ignored when V_{CC2} and V_{EE} supplies are not sufficient causing UVLO clamp to be active. Both V_{UVLOP+} and V_{UVLON+} will need to be crossed before the clamp can be released. Thereafter, V_{OUTP} and V_{OUTN} will respond to I_F and DESAT accordingly.

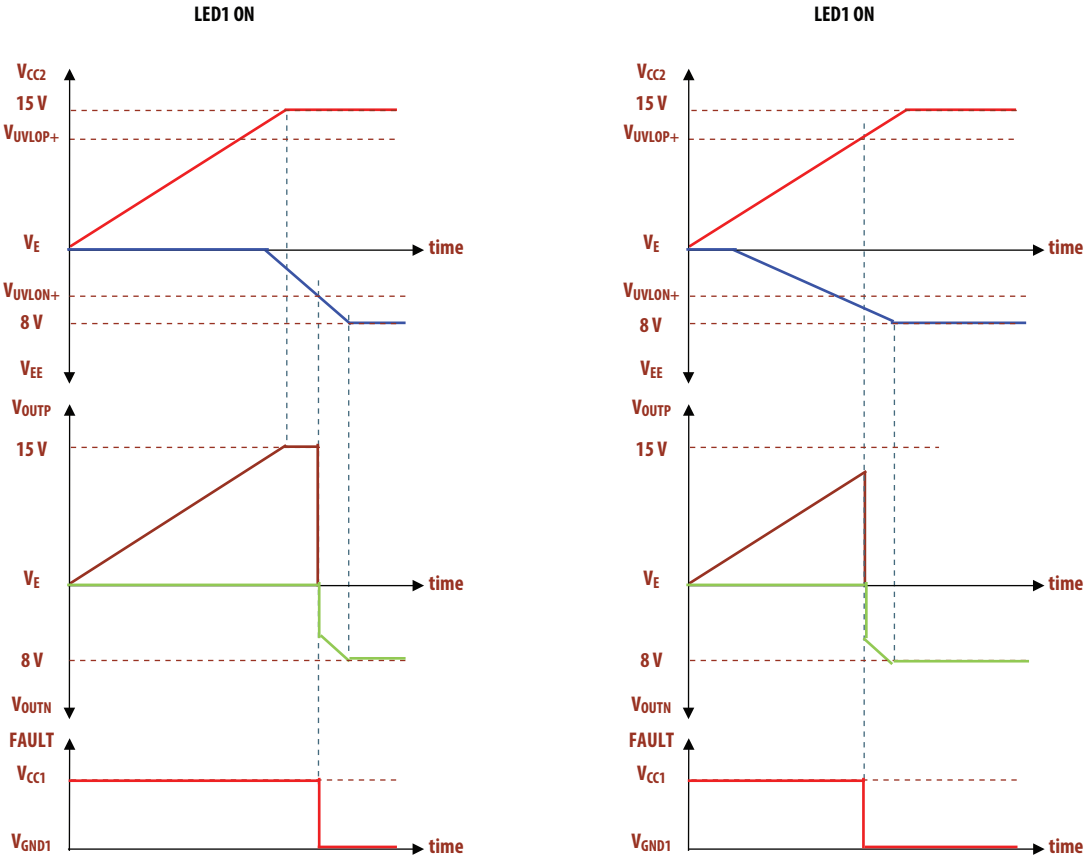


Figure 31. UVLO, V_{OUT} and FAULT logic diagram

Drive and Shutdown MOSFET Selection

The MOSFETs, MP1 and MN1 driving strength can be estimated by the gate charge and desired charge time needed. The equation below shows an example of this:

$Qg = I_{CHARGE} \times T_{CHARGE}$
Qg is the total gate charge that can be picked readily from the IGBT data sheets.

For a 1200/50 A IGBT, the typical Qg is approximately 300 nC and for desired charging time of 200 ns, the I_{CHARGE} will be,

I_{CHARGE} = 300 nC / 200 ns = 1.5 A

The charging current calculated is an average current. The peak gate current of the MOSFET driver can be estimated using the rule of thumb of doubling the I_{CHARGE}. So for this example, a 3 A peak current MOSFET driver rating will be appropriate.

Listed in the table below, are some recommended MOSFET ratings and part numbers suitable for their respective IGBT class.

Applications	IGBT Class	Qg	Estimated Peak Charging Current	MN1	MP1	MN2	MN3
Low Power	1200 V / 50 A	300 nC	3A	Sanyo ECH8619	Sanyo ECH8619	Vishay SI2308	Siemens BSS159
Mid Power	1200 V / 300 A	2000 nC	8A	Vishay SI7414	Vishay SI7415	Vishay SI2308	Siemens BSS159
High Power	1200 V / 600 A	4000 nC	16A	Vishay SIS434	Vishay SI7611	Fairchild FDC5612	CLARE CPC3703

Selecting the Gate Resistor (R_G)

The IGBT switching time is determined by the charging and discharging of the gate of the IGBT. Higher gate peak current will decrease the turn-on and turn-off time and hence reduce the the switching losses. The charging and discharging currents are controlled by the gate resistors R_{GP} and R_{GN} respectively. The R_G must be able to limit the peak current below the maximum allowed for the PMOS(MP1) and NMOS(MN1). The internal R_{DSON} of MP1 and MN1 must be taken into account when calculating the peak current.

$$R_{GP} \geq \frac{V_{CC} - V_{EE}}{I_{OP(MAX)}} - R_{DSONP} \qquad R_{GN} \geq \frac{V_{CC} - V_{EE}}{I_{ON(MAX)}} - R_{DSONN}$$

Other Recommended Components

The application circuit in Figure 27 includes a depletion-mode MOSFET, a DESAT pin protection resistor, FAULT pin capacitor and pull-up resistor, false FAULT prevention diodes.

Split Resistors Input LED Drive Circuit

Figure 32 shows the recommended drive circuit that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage change at the anode and cathode.

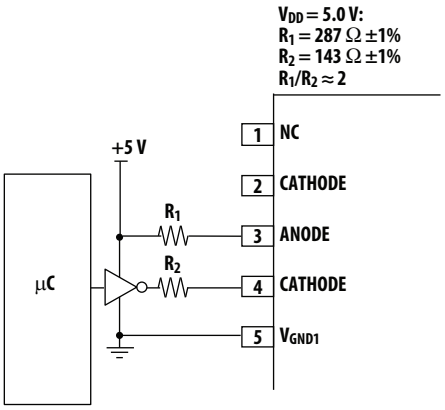


Figure 32. Split Resistors Input LED Drive Circuit

Depletion-mode MOSFET

During start-up, the supplies across V_{CC2} and V_{EE} build up slowly from 0V. It will be harmful to allow the gate driver output to turn on at low supply voltages. UVLO protection kicks in to prevent ACPL-339J outputs from turning on until the supplies reach the UVLO thresholds. But IGBT or Power MOSFET can still be triggered by Miller effect developed by any high dV/dt noise across collector and emitter pins. This miss-triggering can be prevented by depletion-mode MOSFET, MN3. A depletion-mode MOSFET will conduct even if its gate voltage is at 0V with respect to its source pin voltage. During start-up, the V_{GMOS} output voltage stays high, at V_E, to turn on MN3 to shunt away any miller current that appears at the IGBT gate. This will prevent the IGBT from miss-triggering. After the supplies cross the UVLO thresholds, V_{GMOS} output voltage will at V_{EE} to turn off MN3 and resume normal Inverter operations. MN3 is optional for extra protection.

DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, V_{CESAT}, (when the IGBT is "on") and to block high voltages (when the IGBT is "off").

During IGBT switching off and towards the end of the forward conduction of the DESAT diode, a reverse current flow for short time. This reverse recovery effect causes the diode not able to achieve its blocking capability until the mobile charge in the junction is depleted. During this time, there is commonly a very high dV_{CE}/dt voltage ramp rate across the IGBT's collector-to-emitter. This results in $I_{CHARGE} = C_{D\text{-}DESAT} \times dV_{CE}/dt$ charging current which will charge the blanking capacitor, C_{BLANK}. In order to minimize this charging current and avoid false DESAT triggering, it is best to use fast response diodes. Listed in the below table are fast-recovery diodes that are suitable for use as a DESAT diode (D_{DESAT}).

In the recommended application circuit shown in Figure 27, the voltage on pin 15 (DESAT) is $V_{DESAT} = V_F + V_{CE}$, (where V_F is the forward ON voltage of D_{DESAT} and V_{CE} is the IGBT collector-to-emitter voltage). The value of V_{CE} which triggers DESAT to signal a FAULT condition, is nominally 8 V – V_F. If desired, this DESAT threshold voltage can be decreased by using multiple DESAT diodes or low voltage zener diode in series. If n is the number of DESAT diodes, the nominal threshold value becomes $V_{CE,FAULT(TH)} = 8\text{ V} - n \times V_F$. If a Zener diode is used, the nominal threshold value becomes $V_{CE,FAULT(TH)} = 8\text{ V} - V_F - V_z$. In the case of using two diodes instead of one, diodes with half of the total required maximum reverse-voltage rating may be chosen.

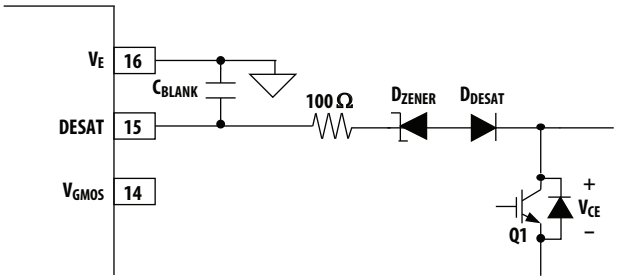


Figure 33. DESAT Diode and DESAT threshold

Part Number	Manufacturer	t_{rr}(ns)	Max. Reverse Voltage Rating, V_{RRM} (Volts)	Package Type
MUR1100E	Motorola	75	1000	59-04 (axial leaded)
MURS160T3	Motorola	75	600	Case 403A (surface mount)
UF4007	General Semi.	75	1000	DO-204AL (axial leaded)
BYM26E	Philips	75	1000	SOD64 (axial leaded)
BYV26E	Philips	75	1000	SOD57 (axial leaded)
BYV99	Philips	75	600	SOD87 (surface mount)

DESAT Pin Protection Resistor

The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the driver if protection is not used. To limit this current to levels that will not damage the driver IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

False Fault Prevention Diodes

One of the situations that may cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This can happen if the reverse recovery spikes coming from the IGBT freewheeling diodes bring the DESAT pin below ground. Hence the DESAT pin voltage will be 'brought' above the threshold voltage. This negative going voltage spikes is typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes. In order to prevent a false fault signal, it is highly recommended to connect a zener diode and schottky diode across the DESAT pin and V_E pin

This circuit solution is shown in Figure 34. The schottky diode will prevent the substrate diode of the gate driver optocoupler from being forward biased while the zener diode (value around 7.5 to 8 V) is used to prevent any positive high transient voltage to affect the DESAT pin.

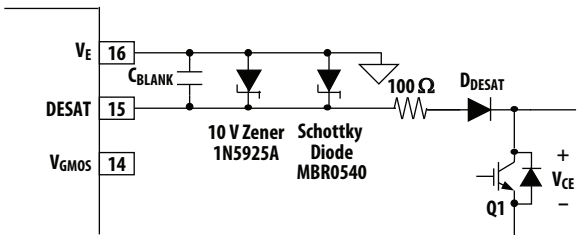


Figure 34. False fault prevention diodes

FAULT Pin Capacitor and Pull-up Resistor

UVLO fault is feedback to the FAULT pin through LED2. If LED2 is normally-off during normal operation, a V_{CC2} or V_{EE} power supplies fault might result in insufficient drive current to turn on LED2 to report the UVLO fault. To avoid such a condition, LED2 need to be normally-on during normal operations. To reduce power consumption, LED2 operates at 50% duty cycle at a frequency of 5 MHz provided by an internal oscillator. A RC network at the FAULT pin is required to filter this oscillation to read a stable "low" for no fault condition.

The RC network consists of a FAULT pin capacitor, C_F and a pull-up resistor R_F. To achieve effective filtering and high CMR, a 1 nF capacitor should be connected between the FAULT pin and ground, and a 10 KΩ pull-up resistor between FAULT pin and V_{CC1}.

Due to the active "high" FAULT logic, the FAULT pins of more than one ACPL-339J cannot be tied together to achieve a common FAULT signal for the controller. An 'OR'ing circuit shown in Figure 35 can be used to overcome the problem.

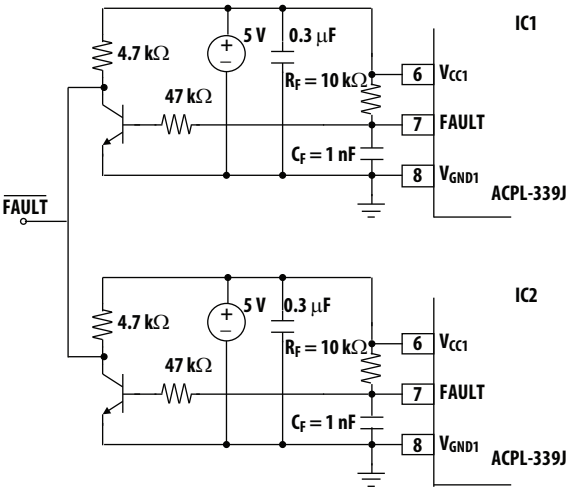


Figure 35. 'OR'ing the FAULT outputs

Dead Time and Propagation Delay Specifications

The ACPL-339J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 37) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 36. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 200 ns over the operating temperature range of -40° C to 105° C.

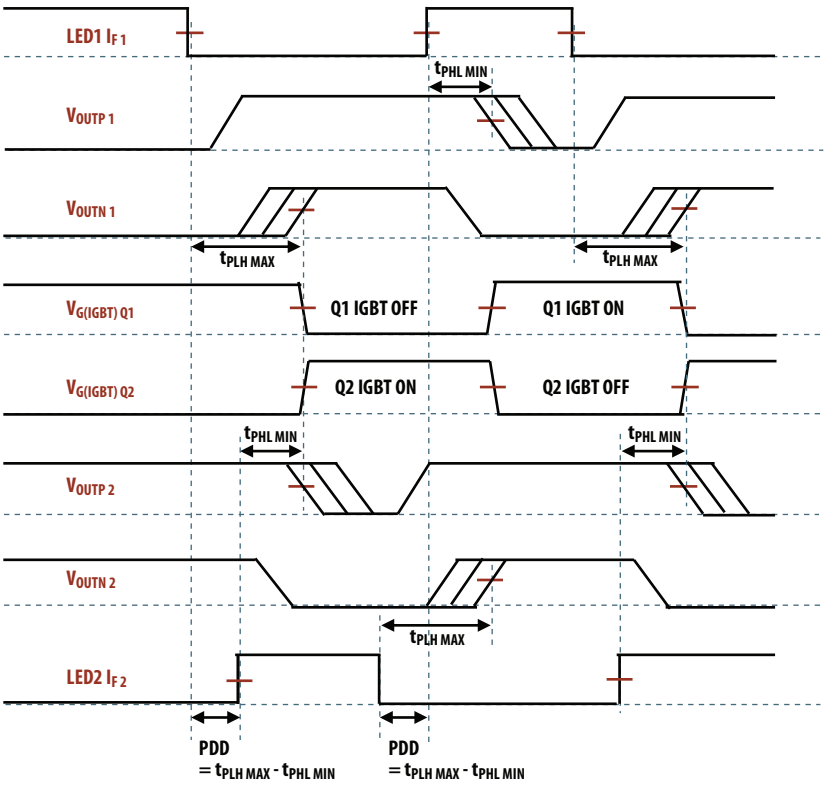


Figure 36. Minimum LED skew for zero dead time

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 37. The maximum dead time for the ACPL-339J is 400 ns (= 200 ns – (-200 ns)) over an operating temperature range of -40° C to 105° C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

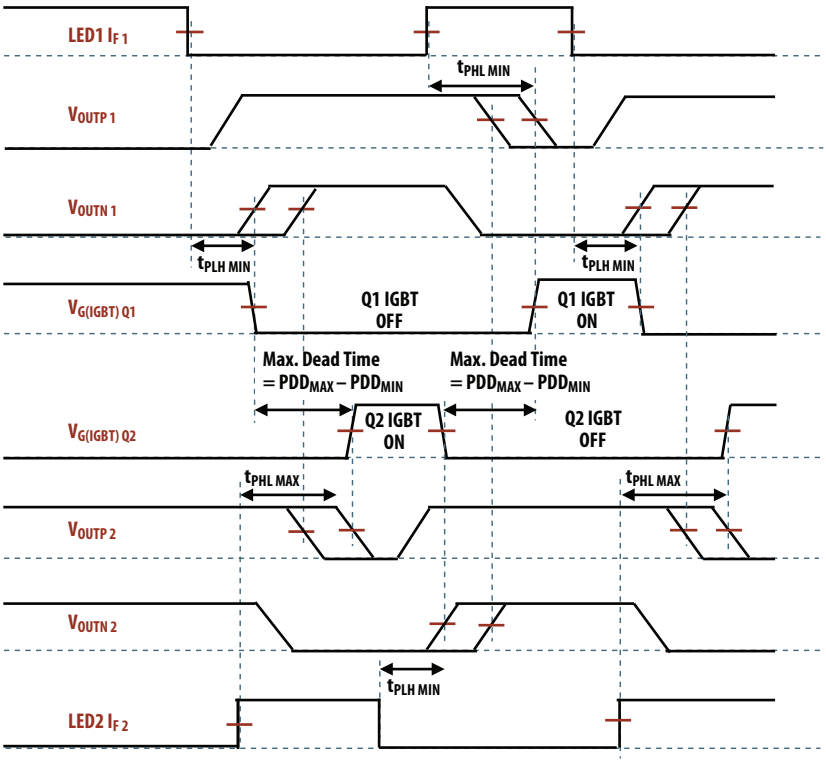


Figure 37. Waveforms for dead time

Thermal Model

Definitions	Symbol	°C/W
Junction to Ambient Thermal Resistance of LED1 due to heating of LED1	R_{11}	103
Junction to Ambient Thermal Resistance of LED1 due to heating of Feedback Detector	R_{12}	24
Junction to Ambient Thermal Resistance of LED1 due to heating of LED2	R_{13}	22
Junction to Ambient Thermal Resistance of LED1 due to heating of Output IC	R_{14}	18
Junction to Ambient Thermal Resistance of Feedback Detector due to heating of LED1	R_{21}	22
Junction to Ambient Thermal Resistance of Feedback Detector due to heating of Feedback Detector	R_{22}	80
Junction to Ambient Thermal Resistance of Feedback Detector due to heating of LED2	R_{23}	29
Junction to Ambient Thermal Resistance of Feedback Detector due to heating of Output IC	R_{24}	17
Junction to Ambient Thermal Resistance of LED2 due to heating of LED1	R_{31}	21
Junction to Ambient Thermal Resistance of LED2 due to heating of Feedback Detector	R_{32}	28
Junction to Ambient Thermal Resistance of LED2 due to heating of LED2	R_{33}	104
Junction to Ambient Thermal Resistance of LED2 due to heating of Output IC	R_{34}	24
Junction to Ambient Thermal Resistance of Output IC due to heating of LED1	R_{41}	25
Junction to Ambient Thermal Resistance of Output IC due to heating of Feedback Detector	R_{42}	23
Junction to Ambient Thermal Resistance of Output IC due to heating of LED2	R_{43}	33
Junction to Ambient Thermal Resistance of Output IC due to heating of Output IC	R_{44}	33

P_1 : Power dissipation of LED1 (W)
P_2 : Power dissipation of Feedback Detector (W)
P_3 : Power dissipation of LED2 (W)
P_4 : Power dissipation of Output IC (W)

T_1 : Junction temperature of LED1 (°C)
T_2 : Junction temperature of Feedback Detector (°C)
T_3 : Junction temperature of LED2 (°C)
T_4 : Junction temperature of Output IC (°C)

T_A : Ambient temperature.

Ambient temperatures were measured approximately 1.25 cm above optocoupler at ~25° C in still air. This thermal model assumes the device is mounted on a high conductivity test board as per JEDEC 51-7. The junction temperatures at the LED1, Feedback Detector, LED2 and Output IC junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} * P_1 + R_{12} * P_2 + R_{13} * P_3 + R_{14} * P_4) + T_A \quad \text{-- (1)}$$
$$T_2 = (R_{21} * P_1 + R_{22} * P_2 + R_{23} * P_3 + R_{24} * P_4) + T_A \quad \text{-- (2)}$$
$$T_3 = (R_{31} * P_1 + R_{32} * P_2 + R_{33} * P_3 + R_{34} * P_4) + T_A \quad \text{-- (3)}$$
$$T_4 = (R_{41} * P_1 + R_{42} * P_2 + R_{43} * P_3 + R_{44} * P_4) + T_A \quad \text{-- (4)}$$

All junction temperatures should be within the absolute maximum rating of 125° C.

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