8-BIT MICROCONTROLLER

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1 GENERAL DESCRIPTION

N79E235 series are 8-bit Turbo 51 microcontrollers which have embedded Flash that can be programmed by ICP (In Circuit Program) or by writer. The instruction sets of the N79E235 series are fully compatible with the standard 8052. N79E235 series contain a **16K/8K** bytes of main Flash EPROM; a **256** bytes of RAM; **256** bytes AUX-RAM; **256** bytes NVM Data Flash EPROM support; **two** 16-bit timer/counters; **one** 16-bit timer with 3 capture inputs; **one** 12-bit capture/compare/auto-reload timer; **8**-channel multiplexed 10-bit A/D converter; **8**-channel 12-bit PWM that includes 6-channel for 3 pairs complementary PWM; **three** serial ports that includes a SPI, an I2C and an enhanced full duplex serial port; **two** analog comparators; 3-level selectable Brownout detector. These peripherals are supported by **XX** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside N79E235 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

N79E235 series, built-in rich functions and peripheral, suit to home appliance and general application.

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller;
- Operating temperature range and operating frequency
  - N79**E**23xA/N79**E**23xRA series: **-40°C ~85°C**
    - V_{DD} = 4.5V to 5.5V @40MHz
    - V_{DD} = 3.0V to 5.5V @24MHz
    - V_{DD} = 2.4V to 5.5V @8MHz
- 85x85xFlexible CPU clock source configurable by config-bit and software:
  - High speed external oscillator: Up to 40MHz Crystal and resonator (enabled by config-bit).
  - Internal oscillator: Nominal 22MHz/11MHz (selected by config-bit)
    N79E23x**A** series: 22MHz/11MHz with ±25% accuracy
    N79E23x**RA** series: 22.1184MHz/11.0592MHz with ±2% accuracy, at 3.3V/25°C
- On-chip Memory
  - 16K/8K bytes of Application Program Flash memory, with ICP and External Writer programmable mode.
  - 256 bytes (8 pages x 32 bytes) Data Flash for customer data storage used and 10K writer cycles; Data Flash program/erase V_{DD}=3.0V to 5.5V
  - 256 bytes of on-chip scratch-pad RAM.
  - 256 bytes of auxiliary RAM, software-selectable, accessed by MOVX instruction.
- Maximum 36 I/O pins.
  - Four outputs mode and TTL/Schmitt trigger selectable Port.
- 17 interrupts source with four levels of priority.
- Four timer/counters.
  - Two 16-bit timer/counters
  - One 16-bit timer supports 3 capture inputs capability for hall sensor feedback.
  - One 12-bit timer supports 12-bit auto reload timer, capture and compare mode.
- Three serial ports
  - One enhanced full duplex UART port with framing error detection and automatic address recognition.
  - One SPI with master/slave capability.
  - One I2C with master/slave capability.
- Four independent 12-bit PWM duty control units with maximum 8 port pins:
  - Six PWM output channels with mask control for BLDC application.
  - Three pairs complementary PWM with programmable dead-time insertion
  - Independent polarity setting for each channel
  - Two brake/fault input pins

- Up to two channels PWM independent from paired PWM channels.
- Eight-channel multiplexed with 10-bits A/D converter.
- Two analog comparators with optional internal reference voltage input at negative end.
- Eight-keypad interrupt inputs.
- Built-in power management.
  - Idle mode
  - Power down mode
- LED drive capability (20mA) on all port pins.
- Config-bits selectable 3 levels(4.5V/3.8V/2.6V) Brown-Out voltage detect interrupt and reset.
- Independent Programmable Watchdog Timer.
- Program and Data Flash security protection.
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:
  - Lead Free (RoHS) LQFP 48: N79E235ALG series (-40°C ~85°C)
  - Lead Free (RoHS) LQFP 48: N79E235RALG series (-40°C ~85°C)
  - Lead Free (RoHS) LQFP 48: N79E234ALG series (-40°C ~85°C)
  - Lead Free (RoHS) LQFP 48: N79E234RALG series (-40°C ~85°C)

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

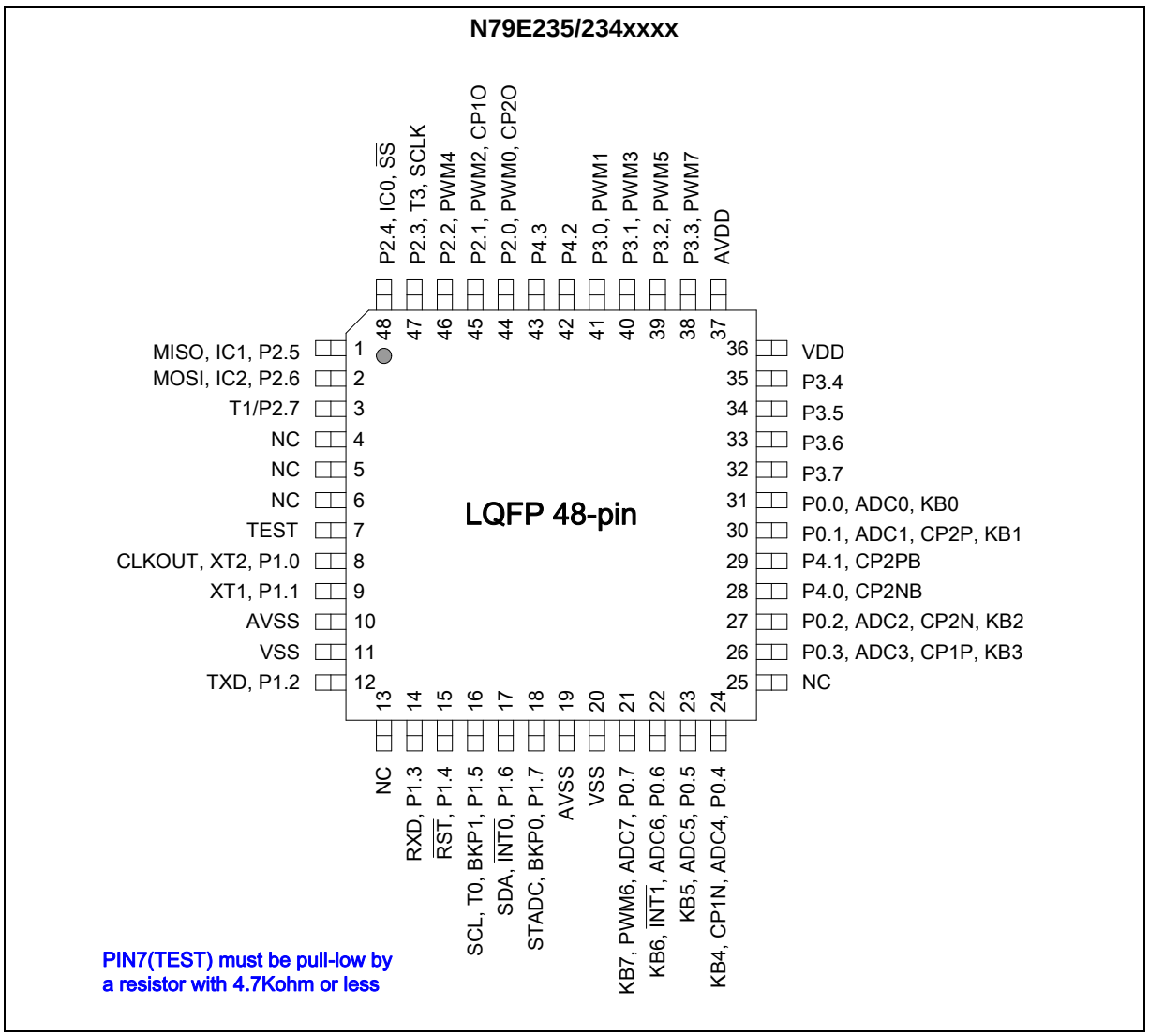
Table 3-1 Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	TEMP °C	INTERNAL RC OSC[1]	PACKAGE
N79E235ALG	16KB	256B+256B	256B	-40~85°C	22MHz ± 25%	LQFP-48
N79E235RALG	16KB	256B+256B	256B	-40~85°C	22.1184MHz ± 2%	LQFP-48
N79E234ALG	8KB	256B+256B	256B	-40~85°C	22MHz ± 25%	LQFP-48
N79234RALG	8KB	256B+256B	256B	-40~85°C	22.1184MHz ± 2%	LQFP-48

Note:

1. Factory calibration condition: V_{DD}=3.3V, TA = 25°C

4 PIN CONFIGURATION



5 PIN DESCRIPTION

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3	Type	DESCRIPTIONS
VDD				P	POWER SUPPLY: Supply voltage for operation.
VSS				P	GROUND: Ground potential.
AVDD				P	ANALOG Power Supply
AVSS				P	ANALOG GROUND.
P0.0	ADC0		KB0	I/O	Port0: Support 4 mode output and 2 mode input. Multifunction pins.
P0.1	ADC1	CP2PA	KB1	I/O	
P0.2	ADC2	CP2NA	KB2	I/O	
P0.3	ADC3	CP1P	KB3	I/O	
P0.4	ADC4	CP1N	KB4	I/O	
P0.5	ADC5		KB5	I/O	
P0.6	ADC6	/INT1	KB6	I/O	
P0.7	ADC7	PWM6	KB7	I/O	
P1.0	XT2	CLKOUT		I/O	Port1: Support 4 mode output and 2 mode input. Multifunction pins. P1.5 and P1.6 are permanently in Open-Drain type.
P1.1	XT1			I/O	
P1.2	TXD			I/O	
P1.3	RXD			I/O	
P1.4	/RST			I, H(rst)	
P1.5	T0	SCL	BKP1	D	
P1.6	/INT0	SDA		D	
P1.7		STADC	BKP0	I/O	
P2.0	PWM0	CP2O		I/O	Port2: Support 4 mode output and 2 mode input. Multifunction pins.
P2.1	PWM2	CP1O		I/O	
P2.2	PWM4			I/O	
P2.3	T3	SCLK		I/O	
P2.4	IC0	/SS		I/O	

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3	Type	DESCRIPTIONS
P2.5	IC1	MISO		I/O	
P2.6	IC2	MOSI		I/O	
P2.7	T1			I/O	
P3.0	PWM1			I/O	Port3:
P3.1	PWM3			I/O	Support 4 modes output and 2 modes input.
P3.2	PWM5			I/O	Multifunction pins.
P3.3*	PWM7			I/O	
P3.4**				I/O	
P3.5**				I/O	
P3.6**				I/O	
P3.7**				I/O	
P4.0*/**		CP2NB		I/O	Support 4 modes output and 2 modes input.
P4.1*/**		CP2PB		I/O	
P4.2*/**				I/O	
P4.3*/**				I/O	
TEST				I	**Must be pull-low by a resistor with 4.7Kohm or less**

TYPE: P: P: power, I: input, O: output, I/O: bi-directional with 4-type I/O modes,, H: Internal pull-up, L: Internal pull low, D: Open Drain

Notes:

- During Power-on-reset, all port pins are in tri-stated.
- After power-on-reset, all port pins state will follow CONFIG0.PRHI bit definition.
- All digital input pins support software enabled schmitt trigger buffer which is selected by SFR PORTS (ECH).

In application if MCU pins need external pull-up, it is recommended to add a pull-up resistor (10KΩ) between pin and power(V_{DD}) instead of directly wiring pin to V_{DD} for enhancing EMC.

6 MEMORY ORGANIZATION

N79E235 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

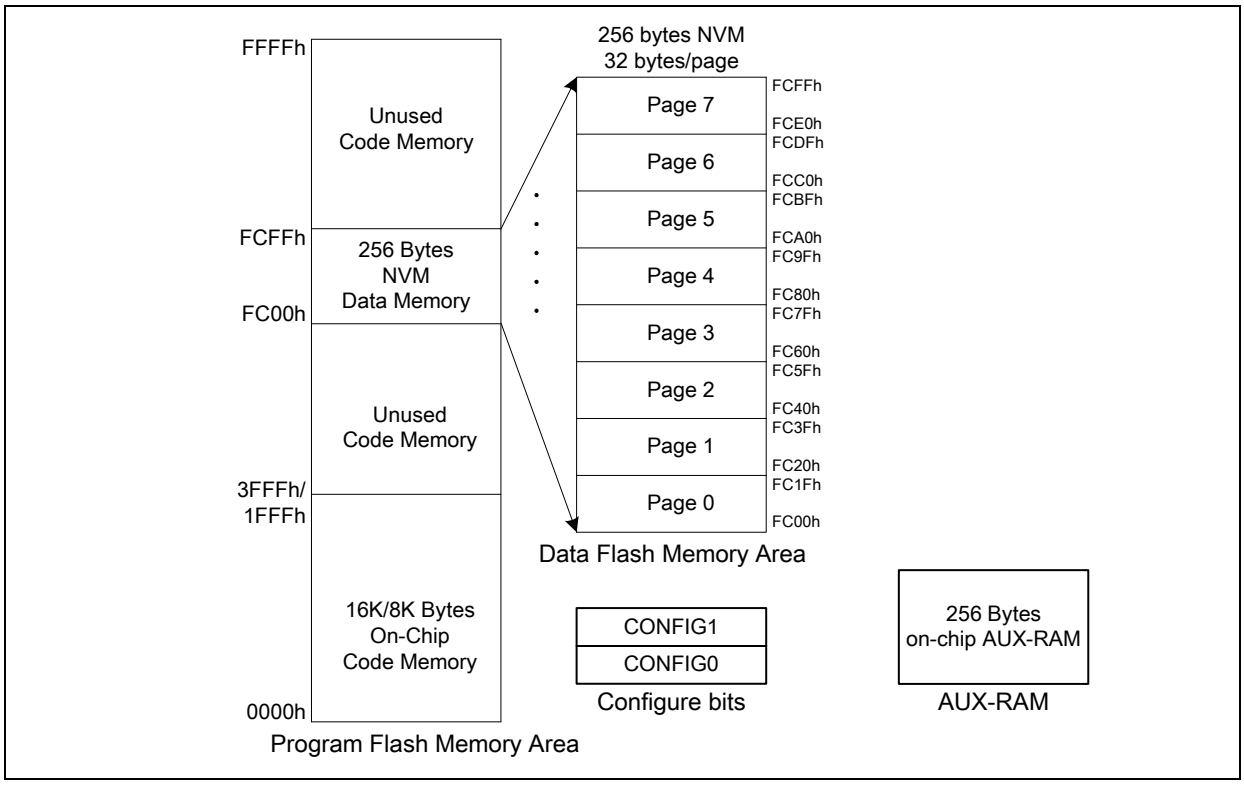


Figure 6-1 N79E235 series Memory Map

6.1 Program Flash Memory

The Program Memory on N79E235 series can be up to **16K/8K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

6.2 Data Flash Memory

The NVM Data Memory of Flash EPROM on the N79E235 series is **256** bytes long, with page size of 16 bytes. The N79E235 series read the content of data memory by using “MOVC A, @A+DPTR”. To write data is by NVMADDRL, NVMDAT and NVMCON SFR’s registers.

6.3 Data Memory (accessed by MOVX)

N79E235 provides 256 bytes AUX RAM accessed by the MOVX instruction. The data memory region is from 0000H to 00FFH. Figure 6-1 shows the memory map for this product series.

6.4 Scratch-pad RAM and Register Map

As mentioned before, N79E235 series have separate Program and Data Memory areas. The on-chip 256 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

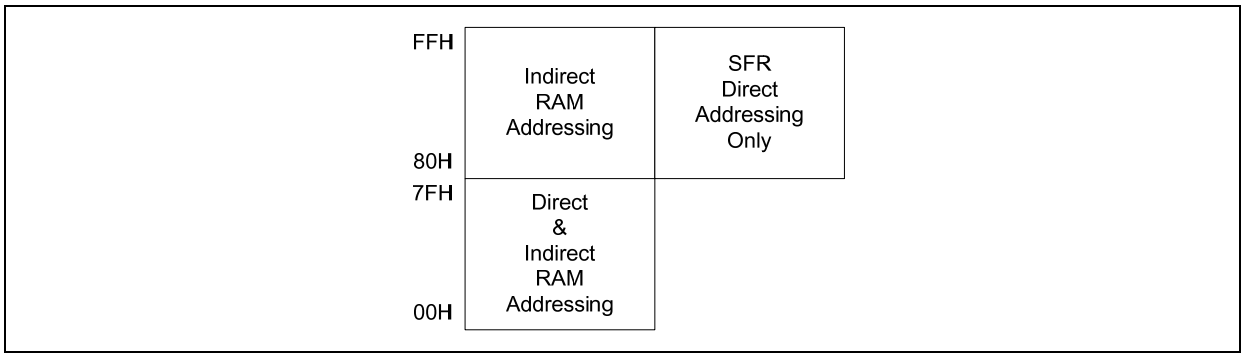


Figure 6-2 N79E235 series RAM and SFR Memory Map

Since the scratch-pad RAM is only 256 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

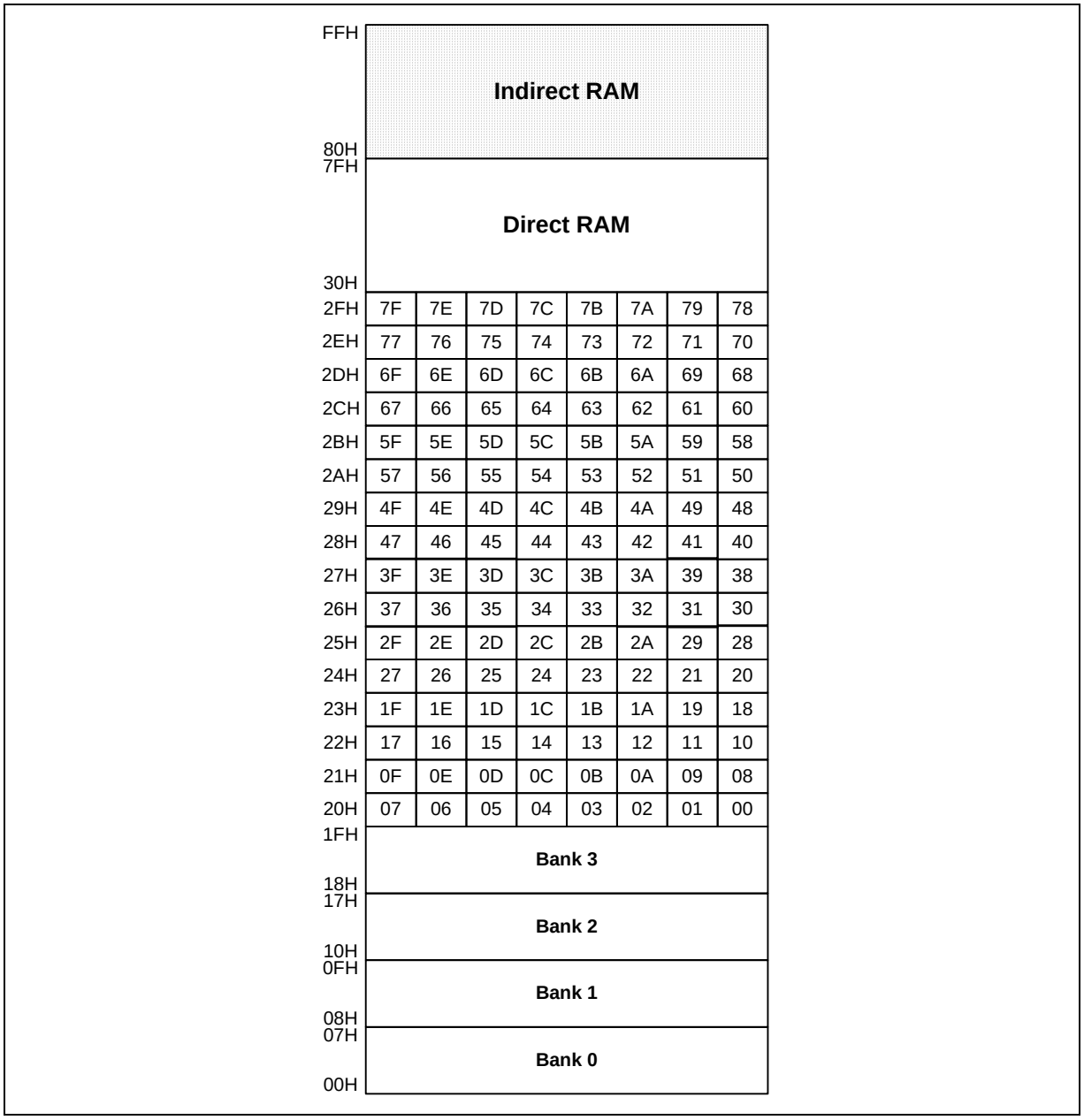


Figure 6-3 Scratch-pad RAM

6.5 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at any one time N79E235 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

6.6 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

6.7 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

7 SPECIAL FUNCTION REGISTERS

N79E235 series use Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. N79E235 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

7.1 SFR Location Table

F8	**IP1**		P4M1	P4M2	PWMCON4	PWM6L	PWM6H	AUXR2
F0	**B**			SPCR	SPSR	SPDR	PADIDS	IP1H
E8	**EIE1**				PORTS	PME	PMD	IP2H
E0	**ACC**	ADCCON	ADCH	ADCCON1	CCL0	CCH0	CCL1	CCH1
D8	**WDCON**(3)	PWMPL	PWM0L		PWMCON1	PWM2L		PWMB
D0	**PSW**	PWMPH	PWM0H		EIE2	PWM2H		PWMCON3
C8	**T2CON**	T2MOD	RCAP2L	RCAP2H	TL2	TH2	NVMCON	NVMDAT
C0	**I2CON**	I2ADDR	T3CON	PNP			NVMADDRL	TA
B8	**IP0**	SADEN			I2DATA	I2STATUS	I2CLK	I2TIMER
B0	**P3**	P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	**IE**	SADDR		DTCNT(3)	CMP1	CMP2	PDTC0(3)	ADCDLY
A0	**P2**	KBI	AUXR1	CAPCON0	CAPCON1	P4	CCL2	CCH2
98	**SCON**	SBUF	IP2	PIO	ADCRL	ADCRH	P3M1	P3M2
90	**P1**	T3L	RCAP3L	RCAP3HT3H			PWM4L	PWM4H
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	**P0**	SP	DPL	DPH			DIV	PCON

Table 7- 1 Special Function Register Location Table

Note:

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.
3. With Timed Access Protection on write operation.

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
AUXR2	AUXR2 CONTROL REGISTER	FFH	T1OE	T0OE	PCMP2DIDS.1	PCMP2DIDS.0	-	ENCLK	ADC1SEL	-	0000 0000b
PWM6H	PWM 6 HIGH BITS REGISTER	FEH		-			PWM6.11	WM6.10	PWM6.9	PWM6.8	XXXX 0000b
PWM6L	PWM 6 LOW BITS REGISTER	FDH	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0	0000 0000b
PWMCON4	PWM CONTROL REGISTER 4	FCH	BK1FILT.1	BK1FILT.0	BK0FILT.1	BK0FILT.0	AUTOBK1	-	BKEN1	BKEN0	0000 0X00b
P4M2	PORT 4 OUTPUT MODE 2	FBH	-	-	-	-	P4M2.3	P4M2.2	P4M2.1	P4M2.0	XXXX 0000b
P4M1	PORT 4 OUTPUT MODE 1	FAH	-	-	-	-	P4M1.3	P4M1.2	P4M1.1	P4M1.0	XXXX 0000b
IP1	INTERRUPT PRIORITY 1	F8H	(FF) PCAP	(FE) PPWM	(FD) PBRK	(FC) PWDI	(FB) -	(FA) PCI	(F9) PKB	(F8) PI2	0000 X000b
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PPWMH	PBRKH	PWDIH	-	PCIH	PKBH	PI2H	0000 X000b
PADIDS	PORT ADC DIGITAL INPUTS DISABLE	F6H	PADIDS.7	PADIDS.6	PADIDS.5	PADIDS.4	PADIDS.3	PADIDS.2	PADIDS.1	PADIDS.0	0000 0000b
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	XXXX XXXXb
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0XXXb
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100b
PCH	PC COUNTER HIGH REGISTER	F2H									0000 0000b
PCL	PC COUNTER LOW REGISTER	F1H									0000 0000b
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
IP2H	INTERRUPT HIGH PRIORITY 2	EFH	-	PT2H	-	-	PSPIH	-	-	PET3H	X0XX 0XX0b
PMD	PWM MASK DATA REGISTER	EEH	-	-	PMD.5	PMD.4	PMD.3	PMD.2	PMD.1	PMD.0	XX00 0000b
PME	PWM MASK ENABLE REGISTER	EDH	-	-	PME.5	PME.4	PME.3	PME.2	PME.1	PME.0	XX00 0000b
PORTS	PORT SHMITT REGISTER	ECH	-	-	-	P4S	P3S	P2S	P1S	P0S	XXX0 0000b
EIE1	INTERRUPT ENABLE 1	E8H	(EF) ECPTF	(EE) EPWM	(ED) EBRK	(EC) EWDI	(EB) -	(EA) ECI	(E9) EKB	(E8) EI2C	0000 X000b
CCH1	INPUT CAPTURE 1 HIGH	E7H	CCH1.7	CCH1.6	CCH1.5	CCH1.4	CCH1.3	CCH1.2	CCH1.1	CCH1.0	0000 0000b
CCL1	INPUT CAPTURE 1 LOW	E6H	CCL1.7	CCL1.6	CCL1.5	CCL1.4	CCL1.3	CCL1.2	CCL1.1	CCL1.0	0000 0000b
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000b
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000b
ADCCON1	ADC CONTROL REGISTER 1	E3H	ADCLK.1	ADCLK.0	STADCT.1	STADCT.0	DLYDIV	ADCCM	PWMSRC.1	PWMSRC.0	0000 0000b
ADCH	ADC CONVERTER RESULT	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	XXXX XXXXb
ADCCON	ADC CONTROL REGISTER	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	XX00 0000b
ACC	ACCUMULATOR	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWMB	PWM BRAKE OUTPUT	DFH	-	-	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B	XX00 0000b
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000b
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	LOAD	PWMF	CLRPWM	FBK1	FBK0	PMOD.1	PMOD.0	0000 0000b
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000b
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000b
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	EXTERNAL RESET: 0X00 0X00b WATCHDOG RESET: 0X000100b POWER ON RESET 0X00 0000b
PWMCON3	PWM CONTROL REGISTER 3	D7H	HZ_Even	HZ_Odd	GRP	PWMTYPE	-	-	P6CTRL	INT_TYPE	XX00 XX00b

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL							LSB	RESET
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	PWM2.11	PWM2.10	PWM2.9	PWM2.8		XXXX 0000b
EIE2	INTERRUPT ENABLE 2	D4H	-	ET2	-	-	ESPI	-	EADCP	ET3		X0XX 0X00b
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8		XXXX 0000b
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8		XXXX 0000b
PSW	PROGRAM STATUS WORD	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P		0000 0000b
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0		0000 0000b
NVMCON	NVM CONTROL	CEH	EER	EWR	-	-	-	-	-	-		00XX XXXXb
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0		0000 0000b
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0		0000 0000b
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0		0000 0000b
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0		0000 0000b
T2MOD	TIMER 2 MODE	C9H	ENLD	ICEN2	ICEN1	ICEN0	T2CR	CMPCR	-	-		0000 00XXb
T2CON	TIMER 2 CONTROL	C8H	TF2	-	-	-	-	TR2	-	CMP/RL2		0XXX X0X0b
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0		0000 0000b
NVMADDRL	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0		0000 0000b
NVMADDRH	NVM HIGH BYTE ADDRESS	C5H	-	-	-	-	-	-	-	NVMADDR.8		XXXX XXX0b
PNP	PWM NEGATIVE POLRARITY	C3H	-	-	PNP.5	PNP.4	PNP.3	PNP.2	PNP.1	PNP.0		XX00 0000b
T3CON	TIMER 3 CONTOL	C2H	TF3	EXF3	T3CNTE	T3OE	T3RST	TR3	T3MOD.1	T3MOD.0		0000 0000b
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC		XXXX XXX0b
I2CON	I2C CONTROL REGISTER	C0H	(C7) -	(C6) ENSI	(C5) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) -		X00000XXb
I2TOC	I2C TIMER-OUT COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF		XXXX X000b
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0		00000000b
I2STATUS	I2C STATUS REGISTER	BDH	B7	B6	B5	B4	B3	B2	B1	B0		1111 1000b
I2DAT	I2C DATA REGISTER	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0		XXXX XXXXb
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0		0000 0000b
IP0	INTERRUPT PRIORITY	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0		X000 0000b
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H		X000 0000b
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0		0000 0000b
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0		0000 0000b
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	-	-	-	P1M2.3	P1M2.2	P1M2.1	P1M2.0		000X 0000b
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	-	-	-	P1M1.3	P1M1.2	P1M1.1	P1M1.0		000X 0000b
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0		0000 0000b
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0		0000 0000b
P3	PORT 3	B0H	(B7) P3.7 OPN	(B6) P3.6 OPP	(B5) P3.5	(B4) P3.4	(B3) P3.3 PWM7	(B2) P3.2 PWM5	(B1) P3.1 PWM3	(B0) P3.0 PWM1		1111 1111b(1) 0000 0000b
ADCDLY	ADC DELAY START REGISTER	AFH	ADCDLY.7	ADCDLY.6	ADCDLY.5	ADCDLY.4	ADCDLY.3	ADCDLY.2	ADCDLY.1	ADCDLY.0		0000 0000b
PDTC0	PWM DEAD TIME CONTROL 0 REGISTER	AEH	-	-	-	-	-	DTENB4	DTENB2	DTENB0		XXXX X000b
CMP2	COMPARATOR 1 CONTROL REGISTER	ADH	-	HYSEN2	CMPEN2	CP2	CN2	COE2	CO2	CMF2		XX0X 0000b
CMP1	COMPARATOR 1 CONTROL REGISTER	ACH	-	HYSEN1	CMPEN1	-	CN1	COE1	CO1	CMF1		XX0X 0000b
DTCNT	PWM DEAD TIME COUNTER REGISTER	ABH	DTCNT.7	DTCNT.6	DTCNT.5	DTCNT.4	DTCNT.3	DTCNT.2	DTCNT.1	DTCNT.0		0000 0000b
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0		0000 0000b
IE	INTERRUPT ENABLE	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0		0000 0000b

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
CCH2	INPUT CAPTURE 2 HIGH	A7H	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0	0000 0000b
CCL2	INPUT CAPTURE 2 LOW	A6H	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0	0000 0000b
P4	PORT 4	A5H	-	-	-	-	P4.3	P4.2	P4.1 CP2PB	P4.0 CP2NB	XXXX 1111b(1) XXXX 0000b
CAPCON1	CAPTURE CONTROL 1	A4H	-	IC0SS	ENF2	ENF1	ENF0	CPTF2	CPTF1	CPTF0	X000 0000b
CAPCON0	CAPTURE CONTROL 0	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD.1	CCLD.0	0000 0000b
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	BOD	BOI	LPBOD	SRST	ADCEN	RCCLK	BOS	0X00 0000b
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000b
P2	PORT 2	A0H	(A7) P2.7 T1	(A6) P2.6 IC2 MOSI	(A5) P2.5 IC1 MISO	(A4) P2.4 IC0 /SS	(A3) P2.3 T3 SCLK	(A2) P2.2 PWM4	(A1) P2.1 PWM2 CP1O	(A0) P2.0 PWM0 CP2O	1111 1111b(1) 0000 0000b
P3M2	PORT 3 OUTPUT MODE 2	9FH	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0	0000 0000b
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	0000 0000b
ADCRH	ADC COMPARE REFERENCE HIGH DATA REGISTER	9DH	ADCR.9	ADCR.8	ADCR.7	ADCR.6	ADCR.5	ADCR.4	ADCR.3	ADCR.2	XXXX XXXXb
ADCRL	ADC COMPARE REFERENCE LOW DATA/COMPARE REGISTER	9CH	ADCR.1	ADCR.0	ADCPO	ADCPI	-	-	T3CSS	ENADCP	XX10 XX00b
PIO	PWM IO REGISTER	9BH	PIO.7	PIO.6	PIO.5	PIO.4	PIO.3	PIO.2	PIO.1	PIO.0	0000 0000b
IP2	INTERRUPT PRIORITY 2	9AH	-	PT2	-	-	PSPI	-	-	PET3	X0XX 0XX0b
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	XXXX XXXXb
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
PWM4H	PWM 4 HIGH BITS REGISTER	97H	-	-	-	-	PWM4.11	PWM4.10	PWM4.9	PWM4.8	XXXX 0000b
PWM4L	PWM 4 LOW BITS REGISTER	96H	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0	0000 0000b
RCAP3HT3H	TIMER 3 RELOAD MSB	93H	RCAP3.11	RCAP3.10	RCAP3.9	RCAP3.8	T3.11	T3.10	T3.9	T3.8	0000 0000b
RCAP3L	TIMER 3 RELOAD LSB	92H	RCAP3.7	RCAP3.6	RCAP3.5	RCAP3.4	RCAP3.3	RCAP3.2	RCAP3.1	RCAP3.0	0000 0000b
TL3	TIMER 3 LSB	91H	T3.7	T3.6	T3.5	T3.4	T3.3	T3.2	T3.1	T3.0	0000 0000b
P1	PORT 1	90H	(97) P1.7 STADC BKP0	(96) P1.6 /INT0 SDA	(95) P1.5 T0 SCL BKP1	(94) P1.4 /RST	(93) P1.3 RXD	(92) P1.2 TXD	(91) P1.1 XT1	(90) P1.0 XT2 CLKOUT	1111 1111b(1) 0000 0000b
CKCON	CLOCK CONTROL	8EH	-	-	-	T1M	T0M	-	-	-	XXX0 0XXXb
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000b
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000b
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000b
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000b
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000b
TCON	TIMER CONTROL	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	POWER CONTROL	87H	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL	00XX 0000b
DIV	DIVIDER	86H	CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0	0000 0000b
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000b
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000b
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111b
P0	PORT 0	80H	(87) P0.7 ADC7 PWM6 KB7	(86) P0.6 ADC6 /INT1 KB6	(85) P0.5 ADC5 KB5	(84) P0.4 ADC4 CP1N KB4	(83) P0.3 ADC3 CP1P KB3	(82) P0.2 ADC2 CP2NA KB2	(81) P0.1 ADC1 CP2PA KB1	(80) P0.0 ADC0 OPO KB0	1111 1111b(1) 0000 0000b

Note: 1. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset

7.2 SFR Detail Bit Descriptions

PORT 0 **Initial=1111_1111b/0000_0000b**

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P0.7	ADC7 or PWM6 or KB7 pin or I/O pin by alternative.
6	P0.6	ADC6 or /INT1 or KB6 or I/O pin by alternative.
5	P0.5	ADC5 or KB5 or Clock (ICP function) pin or I/O pin by alternative.
4	P0.4	ADC4 or CP1N or KB4 or Data (ICP function) pin or I/O pin by alternative.
3	P0.3	ADC3 or CP1P or KB3 pin or I/O pin by alternative.
2	P0.2	ADC2 or CP2NA or KB2 pin or I/O pin by alternative.
1	P0.1	ADC1 or CP2PA or KB1 pin or I/O pin by alternative.
0	P0.0	ADC0 or KB0 pin or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER **Initial=0000 0111b**

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION

7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DIVIDER **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0

Mnemonic: DIV Address: 86h

BIT	NAME	FUNCTION
7~6	CCDIV.1~0	Timer 2 clock select: CCDIV.1 / CCDIV.0 0 / 0 : Timer 2 clock = Fcpu 0 / 1 : Timer 2 clock = Fcpu/4 1 / 0 : Timer 2 clock = Fcpu/16 1 / 1 : Timer 2 clock = Fcpu/32
5~4	PWMDIV.1~0	PWM clock select: PWMDIV.1 / PWMDIV.0 0 / 0 : PWM clock = Fcpu 0 / 1 : PWM clock = Fcpu/2 1 / 0 : PWM clock = Fcpu/4 1 / 1 : PWM clock = Fcpu/16
3~2	T3DIV.1~0	Timer 3 clock select: T3DIV.1 / T3DIV.0 0 / 0 : Timer 3 clock = Fcpu/4 0 / 1 : Timer 3 clock = Fcpu/16

		1	0	Timer 3 clock = Fcpu/32	
		1	1	Timer 3 clock = Fcpu/128	
1~0	T0DIV.1~0	Timer 2 clock select:			
		T0DIV.1	T0DIV.0		
		0	0	Timer 0 clock = Fcpu/4	
		0	1	Timer 0 clock = Fcpu/16	
		1	0	Timer 0 clock = Fcpu/32	
		1	1	Timer 0 clock = Fcpu/128	

POWER CONTROL **Initial=00xx 0000b**

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION

7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL **Initial=xxx0 0xxxb**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks. 4/16/32/128 clocks. The divider selection bits are located in SFR DIV.T0DIV[1:0].
2~0	-	Reserved.

PORT 1 **Initial=1111_1111b/0000_0000b**

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P1.7	BKP1 or STADC or I/O pin by alternative.
6	P1.6(1)	$\overline{\text{INT0}}$ interrupt or SDA or I/O pin by alternative.

5	P1.5(1)	BKP0 or T0 or SCL or Input Pin by alternative.
4	P1.4	$\overline{RST}$ pin or digital input pin by alternative.
3	P1.3	RXD or I/O pin by alternative.
2	P1.2	TXD or I/O pin by alternative.
1	P1.1	XTAL1 or I/O pin by alternative.
0	P1.0	XTAL2 or CLKOUT or I/O pin by alternative.

Note: (1) P1.5 and P1.6 are permanently in open-drain type.

TIMER 3 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	T3.7	T3.6	T3.5	T3.4	T3.3	T3.2	T3.1	T3.0

Mnemonic: T3L Address: 91h

BIT	NAME	FUNCTION
7-0	T3.[7:0]	Timer 3 LSB Bits Register.

TIMER 3 RELOAD/COMPARE LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	RCAP3.7	RCAP3.6	RCAP3.5	RCAP3.4	RCAP3.3	RCAP3.2	RCAP3.1	RCAP3.0

Mnemonic: RCAP3L Address: 92h

BIT	NAME	FUNCTION
7-0	RCAP3L	Timer 3 Reload/Compare LSB: This register is LSB of a 12-bit reload value when timer 3 is configured in reload/compare mode. During compare mode, this register is a compare register. See SFR T3CON for reload/compare mode.

TIMER 3 RELOAD/COMPARE MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	RCAP3.11	RCAP3.10	RCAP3.9	RCAP3.8	T3.11	T3.10	T3.9	T3.8

Mnemonic: RCAP3HT3H Address: 93h

BIT	NAME	FUNCTION
7-4	RCAP3.11~8	Timer 3 Reload/Compare MSB: This register is MSB of a 12-bit reload value when timer 3 is configured in reload/compare mode. During compare mode, this register is a compare register. See SFR T3CON for reload/compare mode.
3-0	T3.11~8	Timer 3 MSB Bits Register.

PWM 4 LOW BITS REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0

Mnemonic: PWM4L Address: 96h

BIT	NAME	FUNCTION
7:0	PWM4	PWM 4 LSB Bits Register.

PWM 4 HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM4.11	PWM4.10	PWM4.9	PWM4.8

Mnemonic: PWM4H Address: 97h

BIT	NAME	FUNCTION
7:4	-	Reserved.
3:0	PWM4	PWM 4 MSB Bits Register.

SERIAL PORT CONTROL **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.

3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

MODE	SM0	SM1	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER **Initial=xxxx xxxxb**

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7-0	SBUF.[7:0]	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

INTERRUPT PRIORITY 2 **Initial=x0xx 0xx0b**

Bit:	7	6	5	4	3	2	1	0
	-	PT2	-	-	PSPI	-	-	PET3

Mnemonic: IP2 Address: 9Ah

BIT	NAME	FUNCTION
7	-	Reserved.
6	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
5-4	-	Reserved.
3	PSPI	1: To set interrupt priority of SPI is higher priority level.

2~1	-	Reserved.
0	PET3	1: To set interrupt priority of Timer 3 is higher priority level.

PWM IO REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PIO7	PIO6	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

Mnemonic: PIO Address: 9Bh

BIT	NAME	FUNCTION
7~0	PIOn	PWM or IO Function Select bit: Select pin output source from PWM or I/O register. 0: Port pin output from port I/O bit register. 1: Port pin output from PWM generator. (Note: n = 0~7). If users select 0 as I/O function, bit0~1 of config1 will be set “1”. Set PWM_Even/ PWM_Odd pins are forced to Hi_Z mode.

ADC COMPARE REFERENCE LOW DATA/COMPARE REGISTER **Initial=0010 xx00b**

Bit:	7	6	5	4	3	2	1	0
	ADCR.1	ADCR.0	ADCPO	ADCPI	-	-	T3CSS	ENADCP

Mnemonic: ADCRL Address: 9Ch

BIT	NAME	FUNCTION
7-6	ADCR.1-0	The 2 MSB bits of ADC compare reference data. Note: These 2 bits are writable only when they are written with ENADCP = 0.
5	ADCPO	ADC Compare output (Read Only). 0: The conversion result is less than reference value. 1: The conversion result is equal or larger than reference value.
4	ADCPI	ADC Compare Change Flag If the ADC compare output status is changed, this bit will be set by hardware. This flag is cleared by software only.
3-2	-	Reserved.
1	T3CSS	Timer 3 external trigger source: 0: T3EX pin is the timer 3 trigger source. 1: ADC compare result, ADCPO, is timer 3 trigger source.
0	ENADCP	ADC Compare Function Enable bit: 0: Disable ADC compare function. 1: Enable ADC compare function.

ADC COMPARE REFERENCE HIGH DATA REGISTER **Initial=xxxx xxxxb**

Bit:	7	6	5	4	3	2	1	0
	ADCR.9	ADCR.8	ADCR.7	ADCR.6	ADCR.5	ADCR.4	ADCR.3	ADCR.2

Mnemonic: ADCRH Address: 9Dh

BIT	NAME	FUNCTION
7-0	ADCR.9-2	The 8 MSB bits of ADC compare reference data. Note: These bits are writable only when ADC compare function is disabled (ENADCP=0)

PORT 3 OUTPUT MODE 1 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0

Mnemonic: P3M1 Address: 9Eh

BIT	NAME	FUNCTION
7-0	P3M1	To control the output configuration of P3 [7:0].

PORT 3 OUTPUT MODE 2 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M1.2	P3M2.1	P3M2.0

Mnemonic: P3M2 Address: 9Fh

BIT	NAME	FUNCTION
7-0	P3M2	See as below table.

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) PORTS.PxS=0, TTL input PORTS.PxS=1, Schmitt input
1	1	Open Drain

Note: X = 0-4. Y = 0-7 (for port0-3), Y = 0-3 (for port4).

PORT 2 **Initial=1111 111b/0000 0000b**

Bit:	7	6	5	4	3	2	1	0

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P2.7	T1 or I/O pin by alternative.
6	P2.6	IC2 or MOSI or I/O pin by alternative.
5	P2.5	IC1 or MISO or I/O pin by alternative.
4	P2.4	IC0 or $\overline{SS}$ pin or I/O pin by alternative.
3	P2.3	T3 or SCLK or I/O pin by alternative.
2	P2.2	PWM4 or I/O pin by alternative.
1	P2.1	PWM2 or CP1O or I/O pin by alternative.
0	P2.0	PWM0 or CP2O or I/O pin by alternative.

KEYBOARD INTERRUPT **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX FUNCTION REGISTER 1 **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

KBF	BOD	BOI	LPBOD	SRST	ADCEN	RCCLK	BOS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Brownout detection will cause chip brownout reset. 1: This prevents brownout detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOD	Low Power Brown Out Detect control: 0: If bit BOD=0, the Brown Out detection is always active. 1: If bit BOD=0, the Brown Out detection repeats to senses the voltage for 64/f_{BRC} then turn off detector for 960/fBRC, therefore, it saves 15/16 of the Brownout circuit power.
3	SRST	Software reset: 1: Reset the chip as if a hardware reset occurred. **(User must specially take care of setting SRST when a write access on AUXR1)**
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	RCCLK	0: The CPU clock is used as ADC clock source. 1: The internal RC 22.1184MHz/11.0592MHz (selectable by CONFIG1.FS1 bit) clock is used as ADC clock source. Note: *This bit can only be set/cleared when ADCEN=0.* The ADC clock source will goes through pre-scalar of /1, /2, /4 or /8, selectable by ADCLK bits (SFR ADCCON1.6-7).
0	BOS	Brownout Status bit(Read only) 0: V_{DD} is above V_{BOR+} 1: V_{DD} is below V_{BOR-}

CAPTURE CONTROL 0 REGISTER **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

CCT2	CCT1	CCT0	CCLD

Mnemonic: CAPCON0 Address: A3h

BIT	NAME	FUNCTION

7~6	CCT2.1~0	Capture 2 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved.
5~4	CCT1.1~0	Capture 1 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved.
3~2	CCT0.1~0	Capture 0 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved
1~0	CCLD.1~0	Reload trigger select: 00 : Timer 2 overflow. 01 : Reload by capture 0 block. 10 : Reload by capture 1 block. 11 : Reload by capture 2 block.

CAPTURE CONTROL 1 REGISTER **Initial=x000 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	IC0SS	ENF2	ENF1	ENF0	CPTF2	CPTF1	CPTF0

Mnemonic: CAPCON1 Address: A4h

BIT	NAME	FUNCTION
7	-	Reserved.
6	IC0SS	Input capture 0 source select: 0: P2.4 pin as input capture 0 trigger source. 1: ADC compare result, ADCPO, as input capture 0 trigger source.
5	ENF2	Enable filter for capture input 2.
4	ENF1	Enable filter for capture input 1.

3	ENF0	Enable filter for capture input 0.
2	CPTF2	External capture/reload 2 interrupt flag.
1	CPTF1	External capture/reload 1 interrupt flag.
0	CPTF0	External/ADCPO capture/reload 0 interrupt flag.

PORT 4 **Initial=xxxx 1111b/xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is xxxx_1111b at reset. If config0.PRHI=0, the initial value is xxxx_0000b at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7-4	-	Reserved.
3	P4.3	Dedicated I/O pin.
2	P4.2	Dedicated I/O pin.
1	P4.1	CP2PB or I/O pin by alternative.
0	P4.0	CP2NB or I/O pin by alternative.

INPUT CAPTURE 2 LOW REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0

Mnemonic: CCL2 Address: A6h

BIT	NAME	FUNCTION
7~0	CCL2.7~0	Capture 2 LSB bits.

INPUT CAPTURE 2 HIGH REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0

Mnemonic: CCH2 Address: A7h

BIT	NAME	FUNCTION
7~0	CCH2.7~0	Capture 2 MSB bits.

INTERRUPT ENABLE **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

PWM DEAD-TIME CONNTER REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	DTCNT.7	DTCNT.6	DTCNT.5	DTCNT.4	DTCNT.3	DTCNT.2	DTCNT.1	DTCNT.0

Mnemonic: DTCNT Address: ABh

BIT	NAME	FUNCTION
7~0	DTCNT.7~0	Dead-time counter. Unsigned 8-bit dead time value bits for Dead Time Unit. Dead-time = F_{CPU} * (DTCNT.[7:0]+1)

Note: This SFR is TA protected.

COMPARATOR 1 CONTROL REGISTER **Initial=x00x 0000b**

Bit:	7	6	5	4	3	2	1	0

-	HYSEN1	CMPEN1	-	CN1	COE1	CO1	CMF1

Mnemonic: CMP1 Address: ACh

BIT	NAME	FUNCTION
7	-	Reserved.
6	HYSEN1	Hysterisis function enable (comparator 1): 0: Without Hysterisis at comparator 1 inputs. (Default). 1: Enable Hysterisis function at comparator 1 that the typical range is about 20mV.
5	CMPEN1	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CMPEN1 is first set.
4	-	Reserved.
3	CN1	Comparator negative input select: 0: The comparator reference pin CNG1 is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	COE1	Output enable: 1: The comparator output is connected to the CMP1 pin if the comparator is enabled (CMPEN1 = 1). This output is asynchronous to the CPU clock.
1	CO1	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CMPEN1 = 0).
0	CMF1	Comparator interrupt flag: This bit is set by hardware whenever the comparator output changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CMPEN1 = 0).

COMPARATOR 2 CONTROL REGISTER **Initial=x000 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	HYSEN2	CMPEN2	CP2	CN2	COE2	CO2	CMF2

Mnemonic: CMP2 Address: ADh

BIT	NAME	FUNCTION
7	-	Reserved.

6	HYSEN2	Hysterisis function enable (comparator 2): 0: Without Hysterisis at comparator 2 inputs. (Default). 1: Enable Hysterisis function at comparator 2 that the typical range is about 20mV.
5	CMPEN2	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CMPEN2 is first set.
4	CP2	Comparator 2 inputs select: 0: (CP2PA, CP2NA) pair comparator 2 input pair is selected. 1: (CP2PB, CP2NB) pair comparator 2 input pair is selected.
3	CN2	Comparator negative input select: 0: The comparator reference pin CNG2 is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	COE2	Output enable: 1: The comparator output is connected to the CMP2 pin if the comparator is enabled (CMPEN2 = 1). This output is asynchronous to the CPU clock.
1	CO2	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CMPEN2 = 0).
0	CMF2	Comparator interrupt flag: This bit is set by hardware whenever the comparator output changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CMPEN2 = 0).

PWM DEAD-TIME CONTROL 0 REGISTER **Initial=xxxx x000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	DTENB4	DTENB2	DTENB0

Mnemonic: PDTC0 Address: AEh

BIT	NAME	FUNCTION
7-3	-	Reserved.

2	DTENB4	Enable dead-time insertion for PWM pair (PWM4, PWM5): Dead-time insertion is only active when this pair of complementary PWM is enabled. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 0: Disable dead-time insertion on the pin pair (PWM4, PWM5). 1: Enable dead-time insertion on the pin pair (PWM4, PWM5).
1	DTENB2	Enable dead-time insertion for PWM pair (PWM2, PWM3): Dead-time insertion is only active when this pair of complementary PWM is enabled. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 0: Disable dead-time insertion on the pin pair (PWM2, PWM3). 1: Enable dead-time insertion on the pin pair (PWM2, PWM3).
0	DTENB0	Enable dead-time insertion for PWM pair (PWM0, PWM1): Dead-time insertion is only active when this pair of complementary PWM is enabled. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 0: Disable dead-time insertion on the pin pair (PWM0, PWM1). 1: Enable dead-time insertion on the pin pair (PWM0, PWM1).

Note: This SFR is TA protected.

ADC DELAY START REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	ADCDLY.7	ADCDLY.6	ADCDLY.5	ADCDLY.4	ADCDLY.3	ADCDLY.2	ADCDLY.1	ADCDLY.0

Mnemonic: ADCDLY Address: AFh

BIT	NAME	FUNCTION
7~0	ADCDLY	These are 8 bits start register to delay start of ADC conversion after detection of ADC start conversion edge by PWM trigger source (controllable through SFR ADCCON1.PWMSRC.1~0) and trigger type (controllable through SFR ADCCON1.STADCT.1~0). An internal 8 bits delay counter will run on PWM clock. When the internal counter matches ADCDLY value, ADC will start conversion. PMU trigger delay time = (ADCDLY+1)/(Fcpu/(4*Divider)). Divider is defined in SFR ADCCON1.3.

Note: User required to clear AUXR1.ADCEN (A2H.2) when re-configure this SFR.

PORT 3 **Initial=1111 1111b/0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is 1111_1111b at reset. If config0.PRHI=0, the initial value is 0000_0000b at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P3.7	OPN or I/O pin by alternative.
6	P3.6	OPP or I/O pin by alternative.
5	P3.5	Dedicated I/O pin.
4	P3.4	Dedicated I/O pin.
3	P3.3	PWM7 or I/O pin by alternative.
2	P3.2	PWM5 or I/O pin by alternative.
1	P3.1	PWM3 or I/O pin by alternative.
0	P3.0	PWM1 or I/O pin by alternative.

PORT 0 OUTPUT MODE 1 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1 **Initial=0xxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	-	-	-	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION

7	P1M1.7	To control the output configuration of P1 bit [7].
6-4	-	Reserved.
3-0	P1M1.3-0	To control the output configuration of P1 bits [3:0].

PORT 1 OUTPUT MODE 2 **Initial=0xxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	-	-	-	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

BIT	NAME	FUNCTION
7	P1M2	To control the output configuration of P1 bits [7].
6-4	-	Reserved.
3-0	P1M2.3-0	To control the output configuration of P1 bits [3:0].

PORT 2 OUTPUT MODE 1 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7-0	P2M1	To control the output configuration of P2 bits [7:0]

PORT 2 OUTPUT MODE 2 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

BIT	NAME	FUNCTION
7-0	P2M2	To control the output configuration of P2 bits [7:0]

INTERRUPT HIGH PRIORITY **Initial=x000 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	-	Reserved
6	PADCH	1: To set interrupt high priority of ADC is highest priority level.
5	PBOH	1: To set interrupt high priority of Brown Out Detector is highest priority level.

4	PSH	1: To set interrupt high priority of Serial port 0 is highest priority level.
3	PT1H	1: Ro set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

INTERRUPT PRIORITY 0 **Initial=x000 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PBO	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

BIT	NAME	FUNCTION
7	-	Reserved
6	PADC	1: To set interrupt priority of ADC is higher priority level.
5	PBO	1: To set interrupt priority of Brown Out Detector is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

I2C DATA REGISTER **Initial=xxxx xxxxb**

Bit:	7	6	5	4	3	2	1	0

I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: BCh

BIT	NAME	FUNCTION
7-0	I2DAT.[7:0]	The data register of I2C.

I2C STATUS REGISTER **Initial=1111 1000b**

Bit:	7	6	5	4	3	2	1	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Mnemonic: I2STATUS Address: BDh

BIT	NAME	FUNCTION
7-0	I2STATUS.[7:0]	The status register of I2C: The three least significant bits are always 0. The five most significant bits contain the status code. There are 26 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C BAUD RATE CONTROL REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7-0	I2CLK.[7:0]	The I2C clock rate bits.

I2C TIMER-OUT COUNTER REGISTER **Initial=xxxx x000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI	DIV4	TIF

Mnemonic: I2TOC Address: BFh

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ENTI	Enable I2C 14-bits Timer Counter: 0: Disable 14-bits Timer Counter count. 1: Enable 14-bits Timer Counter count. After enable ENTI and ENSI, the 14-bit counter will be counted. When SI flag of I2C is set, the counter will stop to

		count and 14-bits Timer Counter will be cleared.
1	DIV4	I2C Timer Counter clock source divide function: 0: The 14-bits Timer Counter source clock is Fcpu clock. 1: The 14-bits Timer Counter source clock is divided by 4.
0	TIF	The I2C Timer Counter count flag: 0: The 14-bits Timer Counter is not overflow. 1: The 14-bits Timer Counter is overflow and I2C interrupt is requested if the I2C interrupt is enabled. Before enable I2C Timer (ENTI, ENSI = [1,1]) the SI must be cleared. This bit is cleared by software.

I2C CONTROL REGISTER **Initial=x000 00xxb**

Bit:	7	6	5	4	3	2	1	0
	-	ENSI	STA	STO	SI	AA	-	-

Mnemonic: I2CON Address: C0h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ENSI	0: Disable I2C Serial Function. The SDA and SCL output are in a high impedance state. SDA and SCL input signals are ignored, I2C is not in the addressed slave mode or it is not addressable, and STO bit in I2CON is forced to “0”. No other bits are affected. Note that P1.5 (SCL) and P1.6 (SDA) are open drain I/O ports. 1: Enable I2C Serial Function. The P1.2 and P1.3 port latches must be to logic 1.
5	STA	The START flag. 0: The STA bit is reset, no START condition or repeated START condition will be generated. 1: The STA bit is set to enter a master mode. The I2C hardware checks the status of I2C bus and generates a START condition if the bus is free. If bus is not free, then I2C waits for a STOP condition and generates a START condition after a delay. If STA is set while I2C is already in a master mode and one or more bytes are transmitted or received, I2C transmits a repeated START condition. STA may be set any time. STA may also be set when I2C interface is an addressed slave mode.
4	STO	In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode. This means it is NO LONGER in the slave receiver mode to receive data from the master transmit device. When I2C is in master mode and If the STA and STO bits are both set, a STOP and a START condition will be transmitted to the I2C bus When I2C is in slave mode and if the STA and STO bits are both set, I2C generates an internal STOP condition which is not transmitted to the I2C bus.
3	SI	I2C Serial Port Interrupt Flag

		0: When the SI flag is reset, no serial interrupt is requested, and there is no stretching on the serial clock on the SCL line. 1: When a new SIO state is present in the I2STATUS register, the SI flag is set by hardware, and, if the EA and EI2C(EIE1.0) bits are both set, an I2C interrupt is requested when SI is set. Only one state that does not cause SI is set is I2STATUS=F8H, which indicates that no relevant state information is available. When SI is set, the low level cycle of the serial clock on the SCL line is stretched, and the serial transfer is suspended. The high level cycle on the SCL line is unaffected by the serial interrupt flag. SI must be cleared by software.
2	AA	The Assert Acknowledge Flag 0: A not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on SCL when: 1) A data has been received while SIO is in the master receiver mode. 2) A data byte has been received while SIO is in the addressed slave receiver mode. 1: An acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when: 1) The own slave address has been received. 2) A data byte has been received while SIO is in the master receiver mode. 3) A data byte has been received while SIO is in the addressed slave receiver mode. 4) The General Call address has been received while the general call bit (GC) in I2ADDR is set.
1~0	-	Reserved.

I2C ADDRESS REGISTER **Initial=xxxx xxx0b**

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR Address: C1h

BIT	NAME	FUNCTION
7~1	I2ADDR.[7:1]	I2C Address register: The content of this register is irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own address. The I2C hardware will react if either of the address is matched.
0	GC	General Call Function. 0: Disable General Call Function. 1: Enable General Call Function.

TIMER 3 CONTROL REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TF3	EXF3	T3CNTE	T3OE	T3RST	TR3	T3MOD.1	T3MOD.0

Mnemonic: T3CON Address: C2h

BIT	NAME	FUNCTION
7	TF3	Timer 3 overflow interrupt flag: This bit is set when Timer 3 overflows. It is cleared only by software. Software can also set this bit.
6	EXF3	Timer 3 capture and compare match interrupt flag: It is set when there is a capture event in capture mode or the count is equal to the capture register in compare mode. It is cleared only by software. Software can also set this bit.
5	T3CNTE	Timer or counter select: When clear, Timer 3 is incremented by the internal clock. When set, the timer counts falling edges on the T3 pin.
4	T3OE	Timer 3 output enable: 1: The T3 pin is toggled whenever Timer 3 overflows. The output frequency is therefore one half of the Timer 3 overflow rate.
3	T3RST	Timer 3 capture/compare match reset: In the Timer 3 capture/compare modes, this bit enables/disables hardware automatically reset timer 3 while the value in TL3 and TH3 have been transferred into the capture register, or compare matched occur.
2	TR3	Timer 3 run control:

		This bit enables/disables the operation of timer 3. Halting this will preserve the current count in TH3 and TL3.
1~0	T3MOD.1~0	Timer 3 mode selection bits: 00: Timer mode 01: Capture mode 10: Auto-reload mode 11: Compare mode

PWM Negative Polarity **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PNP.5	PNP.4	PNP.3	PNP.2	PNP.1	PNP.0

Mnemonic: PNP Address: C3h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5~0	PNP.n	PWM negative polarity bit: The register bit control the initial state as well as polarity/active state of PWM output. 0 = PWMx output is active high (initial state = 0). 1 = PWMx output is active low (initial state = 1).

NVM HIGH BYTE ADDRESS **Initial=xxxx xxx0b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	NVMADDR.8

Mnemonic: NVMADDRH Address: C5h

BIT	NAME	FUNCTION
7-1	-	Reserved.
0	NVMADDR.[8]	The NVM high address: The register indicates NVM data memory of high byte address on On-Chip code memory space.

NVM LOW BYTE ADDRESS **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDRL Address: C6h

BIT	NAME	FUNCTION
7~0	NVMADDR.[7:0]	The NVM low byte address: The register indicates NVM data memory of low byte address on On-Chip code memory space.

TIMED ACCESS **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

TIMER 2 CONTROL **Initial=0xxx x0x0b**

Bit:	7	6	5	4	3	2	1	0
	TF2	-	-	-	-	TR2	-	CMP/ $\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in compare mode. It is cleared only by software. Software can also set this bit.
6~3	-	Reserved.
2	TR2	Timer 2 Run Control: This bit enables/disables the operation of timer 2. Halting this will preserve the current count in TH2, TL2.
1	-	Reserved.
0	CMP/ $\overline{RL2}$	Compare/Reload Select. This bit determines whether the compare or reload function will be used for timer 2. 0: Auto reload will occur when timer 2 overflows. And reload will be from RCAP register if ENLD = 1. 1: When timer 2 value matches RCAP value, timer 2 will reset to 0.

TIMER 2 MODE CONTROL **Initial=0000 00xxb**

Bit:	7	6	5	4	3	2	1	0
	ENLD	ICEN2	ICEN1	ICEN0	T2CR	CMPCR	-	-

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION

7	ENLD	Enable reload from RCAP2 registers to timer 2 counters.
6	ICEN2	Capture 2 External Enable: This bit enables the capture/reload function on the T2 pin. An edge trigger (programmable by CAPCON0.CCT2[1:0] bits) detected on the T2 pin will result in capture from free running timer 2 counters to input capture 2 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.
5	ICEN1	Capture 1 External Enable: This bit enables the capture/reload function on the T1 pin. An edge trigger (programmable by CAPCON0.CCT1[1:0] bits) detected on the T1 pin will result in capture from free running timer 2 counters to input capture 1 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.
4	ICEN0	Capture 0 External Enable: This bit enables the capture/reload function on the T0 pin. An edge trigger (programmable by CAPCON0.CCT0[1:0] bits) detected on the T0 pin will result in capture from free running timer 2 counters to input capture 0 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.
3	T2CR	Timer 2 Capture Reset: In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset timer 2 while the value in TL2 and TH2 have been transferred into the capture register.
2	CMPCR	Compare Counter Reset: Enable counter reset when a match occurs. 0: Disable counter auto-reset in compare mode. 1: Enable counter auto-reset in compare mode.
1~0	-	Reserved.

TIMER 2 RELOAD LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

BIT	NAME	FUNCTION
7-0	RCAP2L	Timer 2 Reload LSB: This register is LSB of a 16-bit reload value when timer 2 is configured in reload mode. During compare mode, this register is a compare register. See CMP/RL2 for reload/compare mode.

TIMER 2 RELOAD MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

BIT	NAME	FUNCTION
7-0	RCAP2H	Timer 2 Reload MSB: This register is MSB of a 16-bit reload value when timer 2 is configured in reload mode. During compare mode, this register is a compare register. See CMP/RL2 for reload/compare mode.

TIMER 2 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

TIMER 2 MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

NVM CONTROL **Initial=00xx xxxxb**

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has **8** pages and each page have 16 bytes data memory. Initiate page selected by writing NVMADDRH and NVMADDL registers, which will automatically enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5-0	-	Reserved

NVM DATA **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	NVMDAT.7	NVMDAT.6	NVMDAT.5	NVMDAT.4	NVMDAT3	NVMDAT.2	NVMDAT.1	NVMDAT.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDAT.[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4~3	RS1~RS0	Register bank select bits.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-0	PWMP.[11:8]	The PWM Counter Register bits 11~8.

PWM 0 HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3~0	PWM0.11~8	The PWM 0 Register bit 11~8.

EXTENDED INTERRUPT ENABLE 2 REGISTER **Initial=x0xx 0x00b**

Bit:	7	6	5	4	3	2	1	0
	-	ET2	-	-	ESPI	-	EADCP	ET3

Mnemonic: EIE2 Address: D4h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ET2	Timer 2 interrupt enable: 0: Disable Timer 2 Interrupt. 1: Enable Timer 2 Interrupt.
5-4	-	Reserved.
3	ESPI	SPI interrupt enable: 0: Disable SPI Interrupt. 1: Enable SPI Interrupt.
2	-	Reserved.
1	EADCP	Enable ADC Compare Interrupt. 0: Disable ADC compare interrupt source. 1: Enable ADC compare interrupt source.

0	ET3	Timer 3 interrupt enable: 0: Disable Timer 3 Interrupt. 1: Enable Timer 3 Interrupt.

PWM 2 HIGH BITS REGISTER **Initial=xxxx xx00b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM2.9~8	The PWM2 Register bit 9~8.

PWM CONTROL REGISTER 3 **Initial=xx00 xx00b**

Bit:	7	6	5	4	3	2	1	0
	HZ_Even	HZ_Odd	GRP	PWMTYPE	-	-	P6CTRL	INT_TYPE

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7	HZ_Even	Control the even PWM ports driving mode: 0: The driving mode of even PWM pins is controlled by output mode registers (PxMy). 1: The driving mode of even PWM pins is forced in Hi-Z mode all the time. The initial value is loaded from config-bit PWM_Even after any reset.
6	HZ_Odd	Control the odd PWM ports driving mode. 0: The driving mode of odd PWM pins is controlled by output mode registers (PxMy). 1: The driving mode of odd PWM pins is forced in Hi-Z mode all the time. The initial value is loaded from config-bit PWM_Odd after any reset.
5	GRP	Group bit 1: Unify the signals timing of PWM0, PWM2 and PWM4 in the same phase which is controlled by PWM0. 0: The signals timing of PWM0, PWM2 and PWM4 are independent.
4	PWMTYPE	PWM mode select bit: 0: Edge-aligned mode. 1: Centre-aligned mode.
3~2		Reserved

1	P6CTRL	PG6 output selection bit: 0: PWM6 output comes from PWM6 frequency/duty generator (if PIO.6 = 1). 1: PWM6 output comes from PWM2 frequency/duty generator (if PIO.6 = 1).
0	INT_TYPE	PWM interrupt type select bit: 0: PWMF will be set if PWM counter underflow. 1: PWMF will be set if PWM counter matches PWMP register. Note: This bit is effective when PWM in central align mode only.

WATCHDOG CONTROL **Initial= Refer to the table below**

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5~4	WD1~WD0	Watchdog Timer Time-out values selected. WD1 / WD0 / WATCHDOG INTERVAL 0 / 0 / 2^{12} 0 / 1 / 2^{16} 1 / 0 / 2^{18} 1 / 1 / 2^{20}
3	WDIF	Watchdog Timer Interrupt flag: 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset flag: 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.

0	WDCLR	Reset Watchdog Timer: This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt (if EWDI (IE.4) is set), and 512 clocks after that a watchdog timer reset will be generated (if EWRST is set). This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x000000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

Reset Type	By external reset	By Watchdog reset	By Power on reset
Value after the reset	0x00 0x00b	0x00 0100b	0x00 000b

All the bits in this SFR have unrestricted read access. WDRUN, WD0, WD1, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH            ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0             ; Reset watchdog timer
ORL     WDCON, #00110000B   ; Select 20 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B   ; Enable watchdog
```

PWM COUNTER LOW BITS REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

BIT	NAME	FUNCTION
7~0	PWMP	PWM Counter Low Bits Register.

PWM 0 LOW BITS REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION

7~0	PWM0	PWM 0 Low Bits Register.

PWM CONTROL REGISTER 1 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	LOAD	PWMF	CLRPWM	FBK1	FBK0	PMOD.1	PMOD.0

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	**Start PWMRUN Control Bit** 0: The PWM is not running. 1: The PWM counter is running.
6	LOAD	**Re-load PWM period registers(PWMP) and PWM duty registers (PWM0~3) control bit.** 0: The value of PWM period register (PWMP) and PWM duty registers (PWM0~PWM3) are not loaded to PWM counter and Comparator registers. 1: Hardware will update the value of PWM period register (PWMP) and PWM duty registers (PWM0~PWM3) to PWM Counter and Comparator register at the time of PWM Counter matches PWMP in edge and central aligned modes or at the time of PWM Counter down counts with underflow in central aligned mode.
5	PWMF	**PWM underflow/match PWMP Flag.** 0: No underflow or match. 1: PWMF is set by hardware when PWM Counter matches PWMP in edge and central aligned modes or when PWM Counter down counts with underflow in central aligned mode. The flag is set depending on PWM edge or central aligned mode as follow; PWM interrupt is requested if PWM interrupt is enabled. **Note**: PWMF must be cleared by software.
4	CLRPWM	**Clear PWM Counter Control Bit.** 1: Clear 12-bit PWM counter to 000H. It is automatically cleared by hardware.
3	FBK1	**The external brake BKP1 pin Flag**. 0: The PWM is not brake by BKP1 pin. 1: The PWM is brake by external brake BKP1 pin. It will be cleared by software.

	Bit PWMCON3.INT_TYPE	PWM counter
Edge Aligned Mode	X	Match PWMP.
Central Aligned Mode	0	Underflow
	1	Match PWMP.

2	FBK0	**The external brake BKP0 pin Flag**. 0: The PWM is not brake by BKP0 pin. 1: The PWM is brake by external brake BKP0 pin. It will be cleared by software.
1-0	PMOD.1-0	**PWM mode selection bits:** 00: Independent mode. 01: Pair/Complementary mode. 10: Synchronized mode 11: Reserved.

PWM 2 LOW BITS REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7:0	PWM2	PWM 2 Low Bits Register.

PWM BRAKE OUTPUT **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMB Address: DFh

BIT	NAME	FUNCTION
7-6	-	Reserved.
5~0	PWMnB	0 = The PWMn output is low, when Brake is asserted. 1 = The PWMn output is high, when Brake is asserted. (Note: n = 0~5).

ACCUMULATOR **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

ADC CONTROL REGISTER **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	ADDR2	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7~6	ADC.1~0	2 LSB bits of the 10-bit ADC conversion result.
5	ADCEX	Enable STADC and PWM-triggered conversion: 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.7) or rising/falling edge on PWM. **Note**: PWM trigger will be enabled if ADCCON1.STADCT.1 = 1 and ADCEX = 1. This product supports 4 PWM channels for ADC start conversion triggers. User may also select the trigger type of rising or falling edge. User may also control the delay timing of PWM's ADC start trigger. See ADC section for descriptions.
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. While this flag is 1, the ADC cannot start a new conversion. This bit will be cleared by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. Notes: 1. It is recommended to clear ADCI ***before*** ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel. 2. Software clearing of ADCS will abort conversion in progress. 3. If ADC is not in Continuous Mode, it cannot start a new conversion while ADCS or ADCI is high.
2~0	AADR2~0	The ADC input select.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADDR2, AADR1, AADR0: ADC Analog Input Channel select bits:

(Note : These bits should only be changed when ADCI and ADCS are both zero.)

AADR2	AADR1	AADR0	Selected Analog Channel
0	0	0	ADC0 (P0.0)
0	0	1	ADC1 (P0.1)

0	1	0	ADC2 (P0.2)
0	1	1	ADC3 (P0.3)
1	0	0	ADC4 (P0.4)
1	0	1	ADC5 (P0.5)
1	1	0	ADC6 (P0.6)
1	1	1	ADC7 (P0.7)

ADC CONVERTER RESULT REGISTER **Initial=xxxx xxxxb**

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

BIT	NAME	FUNCTION
7~0	ADC.9~2	8 MSB bits of the 10-bit ADC conversion result.

ADC CONTROL REGISTER 1 **Initial=0100 0000b**

Bit:	7	6	5	4	3	2	1	0
	ADCLK.1	ADCLK.0	STADCT.1	STADCT.0	DLYDIV	ADCCM	PWMSRC.1	PWMSRC.0

Mnemonic: ADCCON1 Address: E3h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7~6</td><td>ADCLK.1~0</td><td>ADC Clock Prescaler:
The 10-bit ADC needs a clock to drive the converting and the clock frequency need to be within 200KHz to 20MHz. ADCLK[1:0] controls the frequency of the clock to ADC block as below table;
<table>
<tr><th>ADCLK.1</th><th>ADCLK.0</th><th>ADC Clock Frequency</th></tr>
<tr><td>0</td><td>0</td><td>ADCCLK/1</td></tr>
<tr><td>0</td><td>1</td><td>ADCCLK/2 (default)</td></tr>
<tr><td>1</td><td>0</td><td>ADCCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>ADCCLK/8</td></tr>
</table></td></tr>
<tr><td>5~4</td><td>STADCT.1~0</td><td>STADC Trigger Type selection bits:
These bits select rising or falling edge for ADC start trigger type.
00: Triggered by P1.7 rising edge (default).
01: Trigger by PWM rising edge.
10: Trigger by PWM falling edge.
11: Trigger by PWM centre-align (at centre point).</td></tr>
</table>

3	DLYDIV	ADC Delay Clock divider select bit: 0: Divider = 1. 1: Divider = 2. The internal counter for PMU trigger delay is clocked by machine clock, Fcpu/4. This bit is meant for dividing the machine clock (Fcpu/4) clock source as per PMU trigger delay time equation below; PMU trigger delay time = (ADCDLY+1)/(Fcpu/(4*DLYDIV)).
2	ADCCM	ADC Continuous Mode 0: Disable ADC continuous mode. 1: Enable ADC continuous mode.
1-0	PWMSRC.1~0	PWM Source selection bits: These bits select PWM channel to cause ADC start conversion. 00: PWM Channel 0. 01: PWM Channel 2. 10: PWM Channel 4. 11: PWM Channel 6.

Note:

User required to clear ADCEN (ADCEN = 0) when re-configure this SFR.

For PWM trigger ADC start conversion in centre align mode, ADC start conversion point will be at the same, regardless of which pwm channel is selected.

INPUT CAPTURE 0 LOW REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0

Mnemonic: CCL0 Address: E4h

BIT	NAME	FUNCTION
7~0	CCL0	Capture 0 low byte.

INPUT CAPTURE 0 HIGH REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0

Mnemonic: CCH0 Address: E5h

BIT	NAME	FUNCTION
7~0	CCH0	Capture 0 high byte.

INPUT CAPTURE 1 LOW REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0

CCL1.7	CCL1.6	CCL1.5	CCL1.4	CCL1.3	CCL1.2	CCL1.1	CCL1.0

Mnemonic: CCL1 Address: E6h

BIT	NAME	FUNCTION
7~0	CCL1	Capture 1 low byte.

INPUT CAPTURE 1 HIGH REGISTER **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

CCH1.7	CCH1.6	CCH1.5	CCH1.4	CCH1.3	CCH1.2	CCH1.1	CCH1.0

Mnemonic: CCH1 Address: E7h

BIT	NAME	FUNCTION
7~0	CCH1	Capture 1 high byte.

INTERRUPT ENABLE REGISTER 1 **Initial=0000 x000b**

Bit: 7 6 5 4 3 2 1 0

ECPTF	EPWM	EBRK	EWDI	-	ECI	EKB	EI2C

Mnemonic: EIE1 Address: E8h

BIT	NAME	FUNCTION
7	ECPTF	0: Disable capture interrupts. 1: Enable capture interrupts.
6	EPWM	0: Disable PWM Interrupt when PWM counter match/underflow. 1: Enable PWM Interrupt when PWM counter match/underflow.
5	EBRK	0: Disable PWM brake interrupt. 1: Enable PWM brake interrupt.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3	-	Reserved.
2	ECI	0: Disable Comparator 1 and 2 Interrupt. 1: Enable Comparator 1 and 2 Interrupt.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	EI2C	0: Disable I2C Interrupt. 1: Enable I2C Interrupt.

PORTS SHMITT REGISTER **Initial=xxx0 0000b**

Bit: 7 6 5 4 3 2 1 0

-	-	-	P4S	P3S	P2S	P1S	P0S

Mnemonic: PORTS Address: ECh

BIT	NAME	FUNCTION
7~5	-	Reserved.
4	P4S	1: Enables Schmitt trigger inputs on Port 4.
3	P3S	1: Enables Schmitt trigger inputs on Port 3.
2	P2S	1: Enables Schmitt trigger inputs on Port 2.
1	P1S	1: Enables Schmitt trigger inputs on Port 1.
0	P0S	1: Enables Schmitt trigger inputs on Port 0.

PWM MASK ENABLE REGISTER **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PME.5	PME.4	PME.3	PME.2	PME.1	PME.0

Mnemonic: PME Address: EDh

BIT	NAME	FUNCTION
7~6	-	Reserved.
5~0	PME.n	PWM Mask Enable bit: The PWM generator signal will be masked when this bit is enabled. The corresponding PWMn channel will be output with PMD.n data. 0: PWM generator signal is output to next stage. 1: PWM generator signal is masked and PMD.n is output to next stage. (Note: n = 0~5).

PWM MASK DATA REGISTER **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PMD.5	PMD.4	PMD.3	PMD.2	PMD.1	PMD.0

Mnemonic: PMD Address: EEh

BIT	NAME	FUNCTION
7~6	-	Reserved.
5~0	PMD.n	PWM Mask Data bit: This data bit control the state of PWMn output pin, if corresponding PME.n = 1. 0: Output logic low to PWMn. 1: Output logic high to PWMn. (Note: n = 0~5).

INTERRUPT HIGH PRIORITY 2 **Initial=x0xx 0xx0b**

Bit:	7	6	5	4	3	2	1	0
	-	PT2H	-	-	PSPIH	-	-	PET3H

Mnemonic: IP2H Address: EFh

BIT	NAME	FUNCTION
7	-	Reserved.
6	PT2H	1: To set interrupt high priority of Timer 2 is highest priority level.
5~4	-	Reserved.
3	PSPIH	1: To set interrupt high priority of SPI is highest priority level.
2~1	-	Reserved.
0	PET3H	1: To set interrupt high priority of Timer 3 is highest priority level.

B REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

BIT	NAME	FUNCTION
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

SERIAL PERIPHERAL CONTROL REGISTER **Initial=0000 0100b**

Bit:	7	6	5	4	3	2	1	0
	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0

Mnemonic: SPCR Address: F3h

BIT	NAME	FUNCTION

<table>
<tr><td>7</td><td>SSOE</td><td>Slave Select Output Enable Bit.
The $\overline{SS}$ output feature is enabled only in master mode by asserting the SSOE bit.
$\overline{SS}$ input not effected by SSOE when the device in slave mode.
0: $\overline{SS}$ input (with mode fault).
1: $\overline{SS}$ output (no mode fault).
<table>
<tr><th>DRSS</th><th>SSOE</th><th>Master Mode</th><th>Slave Mode</th></tr>
<tr><td>0</td><td>0</td><td>$\overline{SS}$ input (With Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>1</td><td>0</td><td>$\overline{SS}$ General purpose I/O (No Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>1</td><td>1</td><td>$\overline{SS}$ output (No Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
</table></td></tr>
<tr><td>6</td><td>SPE</td><td>Serial Peripheral System Enable Bit:
When the SPE bit is set, SPI block functions is enable. When MODF is set, SPE always reads 0.
0: SPI system disabled.
1: SPI system enabled.</td></tr>
<tr><td>5</td><td>LSBFE</td><td>LSB - First Enable:
This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0: Data is transferred most significant bit first.
1: Data is transferred least significant bit first.</td></tr>
<tr><td>4</td><td>MSTR</td><td>Master Mode Select Bit:
It is customary to have an external pull-up resistor on lines that are driven by open-drain devices.
0: Slave mode.
1: Master mode</td></tr>
<tr><td>3</td><td>CPOL</td><td>Clock Polarity Bit:
When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high.</td></tr>
</table>

2	CPHA	Clock Phase Bit: The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols.
1~0	SPR1~0	SPI Baud Rate Selection Bits: These bits specify the SPI baud rates.

SPR1	SPR0	Divider
0	0	16
0	1	32
1	0	64
1	1	128

Note: In master mode, a change of LSBFE, MSTR, CPOL, CPHA and SPR [1:0] will abort a transmission in progress and force the SPI system into idle state.

SERIAL PERIPHERAL STATUS REGISTER **Initial=0000 0xxxb**

Bit:	7	6	5	4	3	2	1	0
	SPIF	WCOL	SPOVF	MODF	DRSS	-	-	-

Mnemonic: SPSR Address: F4h

BIT	NAME	FUNCTION
7	SPIF	SPI Interrupt Complete Flag: SPIF is set upon completion of data transfer between this device and external device or when new data has been received and copied to the SPDR. If SPIF goes high, and if ESPI (located at EIE2.3) is set, a serial peripheral interrupt is generated. SPIF is clear by software, by writing a 0.
6	WCOL	Write Collision Bit: Clearing the WCOL bit is accomplished by software writing a 0. 0: No write collision. 1: Write collision.
5	SPOVF	SPI overrun flag: SPIOVF is set if a new character is received before a previously received character is read from SPDR. Once this bit is set, it will prevent SPDR register from accepting new data. It must be cleared before any new data can be written. This flag is cleared by software, by writing a 0. 0: No overrun. 1: Overrun detected.
4	MODF	SPI Mode Error Interrupt Status Flag: Clearing this bit is by software writing a 0. 0: No mode fault. 1: Mode fault.

3	DRSS	Data Register Slave Select: Refer to above table in SPCR register.
2~0	-	Reserved.

SERIAL PERIPHERAL DATA I/O REGISTER **Initial=xxxx xxxxb**

Bit:	7	6	5	4	3	2	1	0
	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0

Mnemonic: SPDR Address: F5h

BIT	NAME	FUNCTION
7-0	SPDR	SPDR is used when transmitting or receiving data on serial bus.

PORT ADC DIGITAL INPUT DISABLE **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PADIDS.7	PADIDS.6	PADIDS.5	PADIDS.4	PADIDS.3	PADIDS.2	PADIDS.1	PADIDS.0

Mnemonic: PADIDS Address: F6h

BIT	NAME	FUNCTION
7	PADIDS.7	P0.7 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 7.
6	PADIDS.6	P0.6 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 6.
5	PADIDS.5	P0.5 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 5.
4	PADIDS.4	P0.4 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 4/Comparator 1 (CP1N) input.
3	PADIDS.3	P0.3 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 3/Comparator 1 (CP1P) input.
2	PADIDS.2	P0.2 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 2/Comparator 2 (CP2N) input.

1	PADIDS.1	P0.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 1/Comparator 2 (CP2P) input.
0	PADIDS.0	P0.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 0.

INTERRUPT HIGH PRIORITY 1 **Initial=0000 x000b**

Bit: 7 6 5 4 3 2 1 0

PCAPH	PPWMH	PBRKH	PWDIH	-	PCIH	PKBH	PI2H

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	PCAPH	1: To set interrupt high priority of Capture 0/1/2 as highest priority level.
6	PPWMH	1: To set interrupt high priority of PWM's counter match/underflow is highest priority level.
5	PBRKH	1: To set interrupt high priority of PWM's brake is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3	-	Reserved.
2	PCIH	1: To set interrupt high priority of Comparator 1 and 2, is highest priority level.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	PI2H	1: To set interrupt high priority of I2C is highest priority level.

INTERRUPT PRIORITY 1 **Initial=0000 x000b**

Bit: 7 6 5 4 3 2 1 0

PCAP	PPWM	PBRK	PWDI	-	PCI	PKB	PI2

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	PCAP	1: To set interrupt priority of Capture 0/1/2 as higher priority level.
6	PPWM	1: To set interrupt priority of PWM's counter match/underflow is higher priority level.
5	PBRK	1: To set interrupt priority of PWM's brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3	-	Reserved.
2	PC1	1: To set interrupt priority of Comparator 1 and 2, is higher priority level.

1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	PI2	1: To set interrupt priority of I2C is higher priority level.

PORT 4 OUTPUT MODE 1 **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4M1.3	P4M1.2	P4M1.1	P4M1.0

Mnemonic: P4M1 Address: FAh

BIT	NAME	FUNCTION
3-0	P4M1	To control the output configuration of P4 bits [3:0]

PORT 4 OUTPUT MODE 2 **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4M2.3	P4M2.2	P4M2.1	P4M2.0

Mnemonic: P4M2 Address: FBh

BIT	NAME	FUNCTION
3-0	P4M2	To control the output configuration of P4 bits [3:0]

PWM CONTROL REGISTER 4 **Initial=0000 0x00b**

Bit:	7	6	5	4	3	2	1	0
	BK1FILT.1	BK1FILT.0	BK0FILT.1	BK0FILT.0	AUTOBK1	-	BKEN1	BKEN0

Mnemonic: PWMCON4 Address: FCh

BIT	NAME	FUNCTION
7-6	BK1FILT.1-0	Brake 1 (BKP1 pin) edge detector filter type bits: 00: Filter clock = Fcpu. 01: Filter clock = Fcpu/2. 10: Filter clock = Fcpu/4. 11: Filter clock = Fcpu/8.
5-4	BK0FILT.1-0	Brake 0 (BKP0 pin) edge detector filter type bits: 00: Filter clock = Fcpu. 01: Filter clock = Fcpu/2. 10: Filter clock = Fcpu/4. 11: Filter clock = Fcpu/8.

3	AUTOBK1	Auto-clear Brake condition: 0: No change in PWM0-5 output. PWM0-5 output will remain following PWM generators, if brake is caused by BRK1 pin. 1: This will cause PWM0-5 output to follow PWMnB bits (see note), when low level is detected at BKP1 pin. Note: PNP bits are also able to control the polarity of PWMnB. If PNP.n=0, PWMn output = PWMnB. If PNP.n=1, PWMn output = invert(PWMnB).
2	-	Reserved.
1	BKEN1	Enable brake 1 (BKP1 pin) falling edge detection: 0: Disable brake 1, BKP1 pin, falling edge detect function (default). 1: Enable brake 1, BKP1 pin, falling edge detection. FBK1 flag will set if this brake occurs.
0	BKEN0	Enable brake 0 (BKP0 pin) falling edge detection: 0: Disable brake 0, BKP0 pin, edge detect function (default). 1: Enable brake 0, BKP0 pin, falling edge detection. FBK0 flag will set if this brake occurs.

PWM 6 LOW BITS REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0

Mnemonic: PWM6L Address: FDh

BIT	NAME	FUNCTION
7:0	PWM6	PWM 6 Low Bits Register.

PWM 6 HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM6.11	PWM6.10	PWM6.9	PWM6.8

Mnemonic: PWM6H Address: FEh

BIT	NAME	FUNCTION
7:4	-	Reserved.
3:0	PWM6	PWM 6 High Bits Register.

AUX FUNCTION REGISTER 2 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	T1OE	T0OE	PCMP2DIDS.1	PCMP2DIDS.0	-	ENCLK	ADC1SEL	-

Mnemonic: AUXR2 Address: FFh

BIT	NAME	FUNCTION

7	T1OE	1: The P2.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
6	T0OE	1: The P1.5 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate.
5	PCMP2DIDS.1	P4.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of Comparator 2 (CP2NB) input.
4	PCMP2DIDS.0	P4.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of Comparator 2 (CP2PB) input.
3	Reserved	Reserved
2	ENCLK	1: To use the on-chip RC oscillator, a clock output is enabled on the XTAL2 pin.
1	ADC1SEL	ADC 1 source select bit: 0: From P0.1 input. 1: From Brownout 1.2V output, VBF.
0	Reserved	Reserved

8 INSTRUCTION

The N79E235 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the N79E235 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the N79E235 series reduces the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5

Op-code	HEX Code	Bytes	N79E235 series Machine Cycle	N79E235 series Clock cycles	8032 Clock cycles	N79E235 series vs. 8032 Speed Ratio
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 8-1: Instruction Set for N79E235

9 POWER MANAGEMENT

N79E235 series are provided with idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

9.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the peripheral blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR is completed, the program execution returns to the instruction after one which put the device into Idle mode and continues from there.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When N79E235series are exiting from Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

9.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity, except the functions of Brownout reset, KBI, $\overline{\text{INT1}}$, $\overline{\text{INT0}}$, watchdog timer(Config0.WDTCK=0), ADC(RCCLK=1) and Analog Comparator(if enabled), is completely stopped and the power consumption is reduced to the lowest possible value. The port pins hold at the states of the values held by their respective SFRs.

The interrupt sources that can wake up CPU from the power down mode **are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), comparators interrupt(CMF1/CMF2), ADC interrupt(if ADC clock is from internal RC) and watchdog timer interrupt (if WDTCK = 0).** The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

Besides, the /RST pin trigger by a low pulse of at least two machine cycle terminates the Power Down mode and restarts the clock. The program execution will restart from 0000h.

Note:

1. Either **a low-level or a falling-edge at external interrupt pins /INT0 and INT1** will re-start the oscillator if the global interrupt is enabled(EA=1) and the corresponding interrupt is enabled.
2. **The /INT0 pin is permanently in open-drain type therefore it is recommended with an external pull-up resistor on pin in application**

10 RESET CONDITIONS

The user has several hardware related options for placing N79E235 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. The sources of resets are external reset, power-on-reset, watchdog timer reset and software reset (brownout is also able to reset the device if enabled).

10.1 External Reset

The device continuously samples the /RST pin at state C4 of every machine cycle. Therefore the /RST pin must be held low for at least 2 machine cycles to ensure detection of a valid /RST low. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as /RST is 0. Even after /RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

10.2 Power-On Reset (POR)

When power up, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. During power-on-reset, all port pins will be tri-stated. After power-on-reset, the port pins state will determined by PRHI value.

10.3 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag (WDIF at WDCON.3) will be set by hardware. If the Watchdog reset is enabled (WDRUN at WDCON.7) and the watchdog timer is not cleared before the time-out of 512 clock period since WINTF is set, the watchdog timer will set watchdog reset flag (WTRF at WDCON.2) and generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h. The watchdog reset flag WTRF keeps high after watchdog reset, it must be cleared by software.

10.4 Software Reset

User can software reset the device by setting SRST bit in SFR AUXR1. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h. **User must specially take care of setting SRST when a write access on AUXR1.**

10.5 Brownout Reset

When the power voltage(V_{DD}) is lower than brownout voltage(V_{BOD}), the brownout detector will set brownout interrupt flag(BOF at PCON.5), if brownout reset function is enabled(BOD=1 and BOI=0 at AUXR1) a hardware brownout reset will be triggered and the device keeps in reset state until the V_{DD} raises above brownout voltage. Note that BOF won't be cleared by brownout reset, it must be cleared by software

10.6 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM data retention. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

The WDCON SFR bits are set or cleared in reset condition depending on the source of the reset.

WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0x00b Watchdog reset: 0x00 0100b Power on reset 0x00 0000b

11 INTERRUPTS

N79E235 series have four priority level interrupts structure with 17 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

11.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1 (SFR TCON). The bits IE0 and IE1 in TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE14, then an interrupt will occur.

The timer 2 interrupt is generated through TF2 (due timer 2 overflows or compare match events). The flag must be software cleared.

The timer 3 interrupt is generated through TF3 (due to timer 3 overflows, compare match or capture events). The flag must be software cleared.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE14, then an interrupt will occur.

The capture interrupt is generated through logical OR CPTF0-2 flags. CPTF0-2 flags are set by capture/reload events. Software has to resolve the cause of the interrupt among CPTF0-2. The flags must be software cleared.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. The flag must be software cleared.

I2C will generate an interrupt due to a new SIO state present in I2STATUS register, if both EA and ES bits (in IE register) are both enabled.

SPI asserts interrupt flag, SPIF, upon completion of data transfer with an external device. If SPI interrupt is enabled (ESPI at EIE2.3), a serial peripheral interrupt is generated. SPIF flag is software clear, by writing a 0. MODF and SPIOVF also will generate interrupt if occur. They share the same vector address as SPIF.

Keyboard interrupt is generated when any of the keypad connected to P0 pins is pressed. Each keypad interrupt can be individually enabled or disabled. The flag must be cleared by software.

Comparators 1 and 2 can generate interrupts when detected change in any of the comparator output. CMF1 or CMF2 flag will be asserted, accordingly. The flags must be cleared by software.

PWM period interrupt flag PWMF is set by hardware when its' 12-bit counter underflows/match and is only be cleared by software. The PWM brake interrupt flag0 FBK0 is set when the external brake pin0(BKP0) detects a falling edge if BKEN0 is enabled. Alternatively, the brake interrupt flag1 FBK1 is set by the external brake pin1(BKP1) detecting a falling change if BKEN1 is enabled.

The ADC can generate interrupt after finished ADC converter. There are two ADC interrupt sources; one is obtained by the ADCI bit in the ADCCON SFR and another from ADCPI bit in ADCRL SFR. The flags must be software cleared.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (IE.5) and global interrupt enable are set.

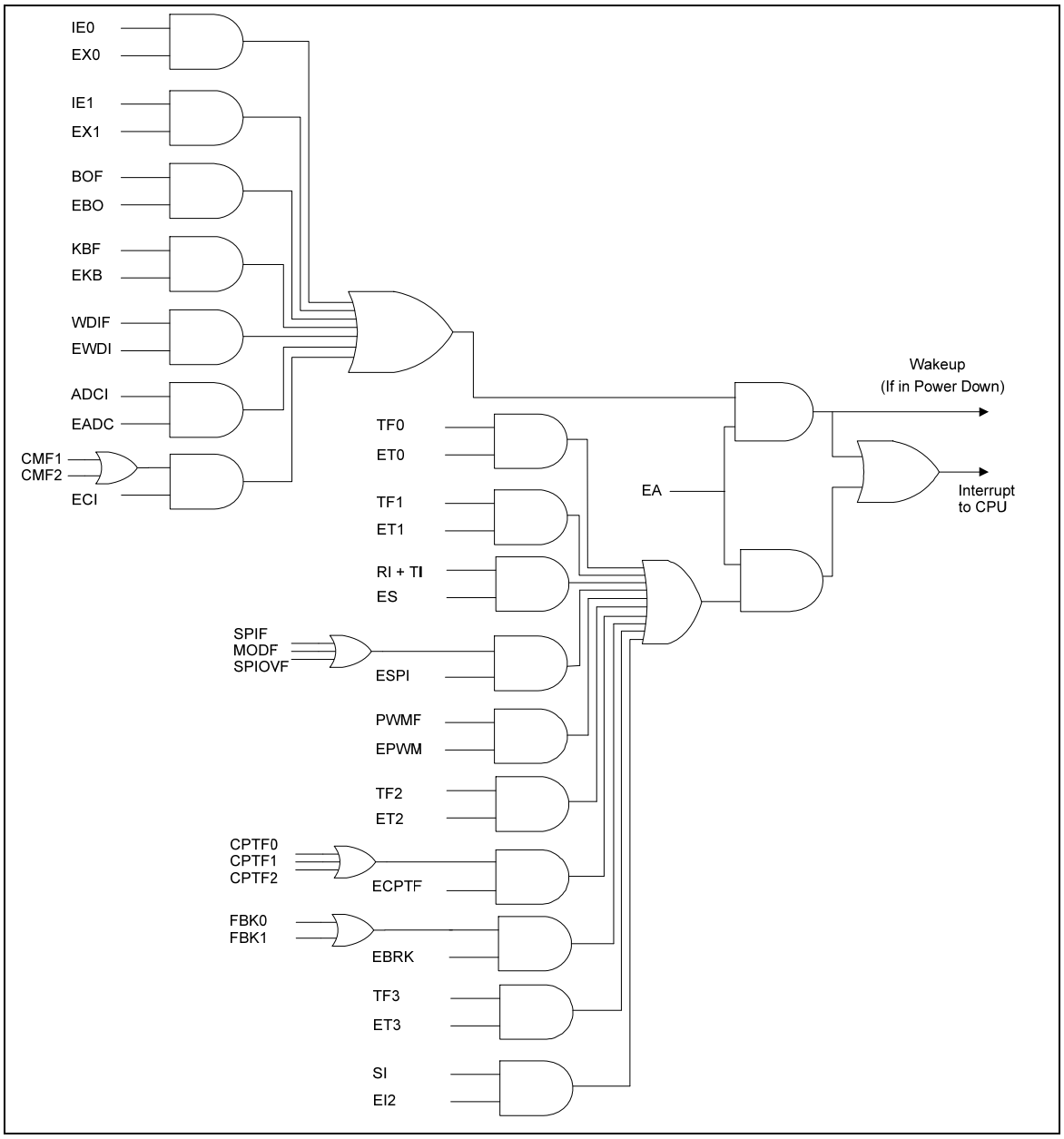


Figure 11-1 Interrupt Source

11.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 11-1 Four-level interrupts priority.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, EIE, EIE2, IP0, IP0H, IP1, IPH1, IP2 or IP2H registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on Table 11-2 Summary of interrupt sources. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

N79E235 series use a four priority level interrupt structure. This allows great flexibility in controlling the handling of the interrupt sources.

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPxH	IPx	

0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 11-1 Four-level interrupts priority

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE, EIE or EIE2. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, IP1H, IP2 and IP2H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector address, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Flag cleared by	Priority bit	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, Software	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (IE.5)	Hardware	IP0H.5, IP0.5	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE14)	Software	IP1H.4, IP1.4	3	Yes[1]
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, Software	IP0H.1, IP0.1	4	No
SPI	SPIF + MODF + SPIOVF	004BH	ESPI (EIE2.3)	Software	IP2H.3, IP2.3	5	No
I2C	SI	0033H	EI2C (EIE1.0)	Software	IP1H.0, IP1.0	6	No
A/D Converter	ADCI+ ADCPI	005BH	EADC (IE.6) + EADCP (EIE2.1)	Software	IP0H.6, IP0.6	7	Yes[2]

External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, Software	IP0H.2, IP0.2	8	Yes
KBI	KBF	003BH	EKB (EIE1.1)	Software	IP1H.1, IP1.1	9	Yes
Comparator 1 & 2	CMF1+ CMF2	0063H	ECI (EIE1.2)	Software	IP1H.2, IP1.2	10	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, Software	IP0H.3, IP0.3	11	No
Serial Port	RI + TI	0023H	ES (IE.4)	Software	IP0H.4, IP0.4	12	No
Timer 2 Overflow/ Match	TF2	007BH	ET2 (EIE2.6)	Software	IP2H.6, IP2.6	13	No
PWM brake	FBK0, FBK1	0083H	EBRK (EIE1.5)	Software	IP1H.2, IP1.2	14	No
Capture	CPTF0-2	006BH	ECPTF (EIE1.7)	Software	IP1H.7, IP1.7	15	No
Timer 3 Overflow/ Match/ Capture	TF3	008BH	ET3 (EIE2.0)	Software	IP2H.0, IP2.0	16	No
PWM match/ underflow	PWMF	0073H	EPWM (EIE1.6)	Software	IP1H.5, IP1.5	17 (lowest)	No

Table 11-2 Summary of interrupt sources

Note:

The Watchdog Timer can wake up Power Down Mode when its clock source is used internal RC.

ADC Converter interrupt source, ADCI, can wake up Power Down Mode when its clock source is used internal RC. However, ADC compare interrupt source, ADCPI, is not able to wake up from Power Down Mode.

11.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all

three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, EIE1, EIE2, IP0, IP0H, IP1, IP1H, IP2 or IP2H and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, EIE1, EIE2, IP0, IP0H, IP1, IP1H, IP2 or IP2H access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

12 OSCILLATOR

N79E235 series provide three oscillator input options. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 40MHz, and optionally with capacitor or resister.

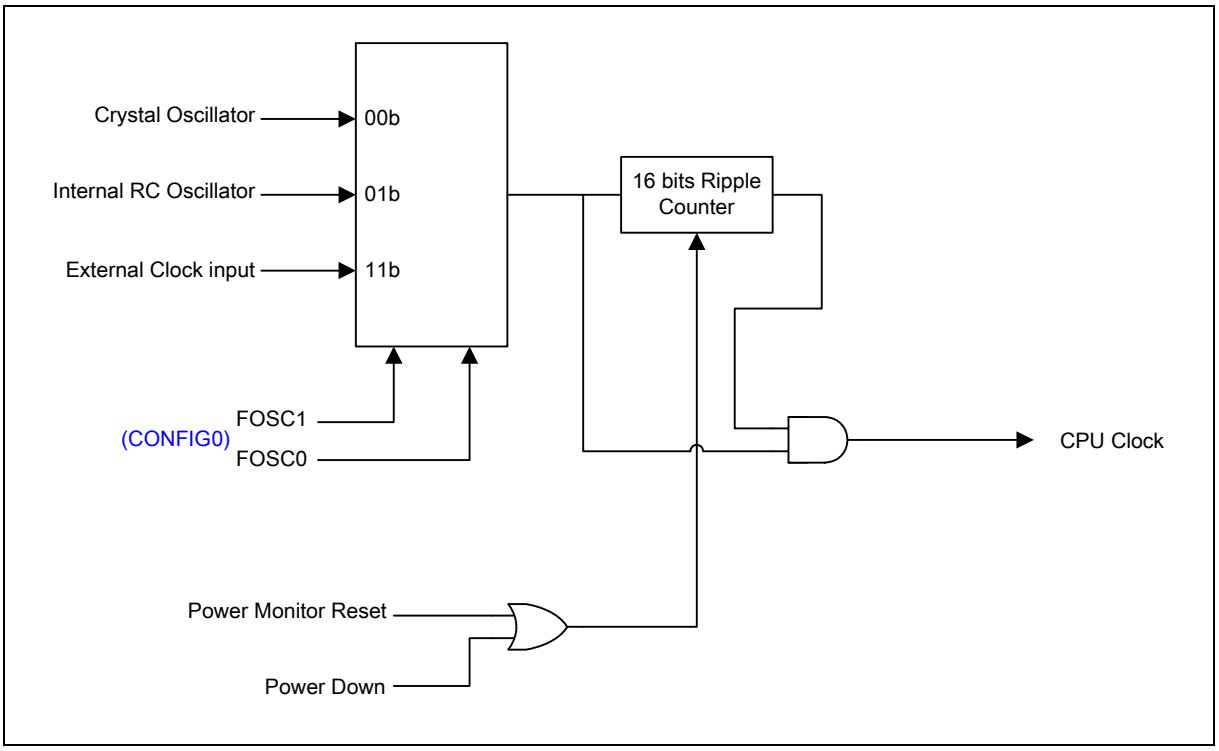


Figure 12-1: Oscillator

12.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is programmable to 22.1184MHz/11.0592MHz +/- 2% (selectable by FS1 config bit) frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled. A clock output on P1.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

12.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 0Hz up to 40MHz. A clock output on P1.0 (XTAL2) may be enabled when External Clock Input is used.

N79E235 series support a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the AUXR2 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

13 POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in N79E235 series to prevent incorrect operation during power up and power drop or loss.

13.1 Power On Detect

The Power–On Detect function is a design to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

13.2 Brownout Detect

The N79E235 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{DD} level during operation by comparing it to a fixed trigger level. There are 3 trigger levels of BOD selected by 2 config0 bits BOV[1:0] suited for wide voltage use. The following table shows the brownout voltage levels supported;

BOV bits (CONFIG0.4-3)	Brownout voltage detect level
00	4.5V
01	3.8V
1x	2.6V (default)

Table 13-1: Brownout Voltage Detect Levels

When the Brownout voltage is drop to the select level, the brownout detector will detect and keeps this active until V_{DD} is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

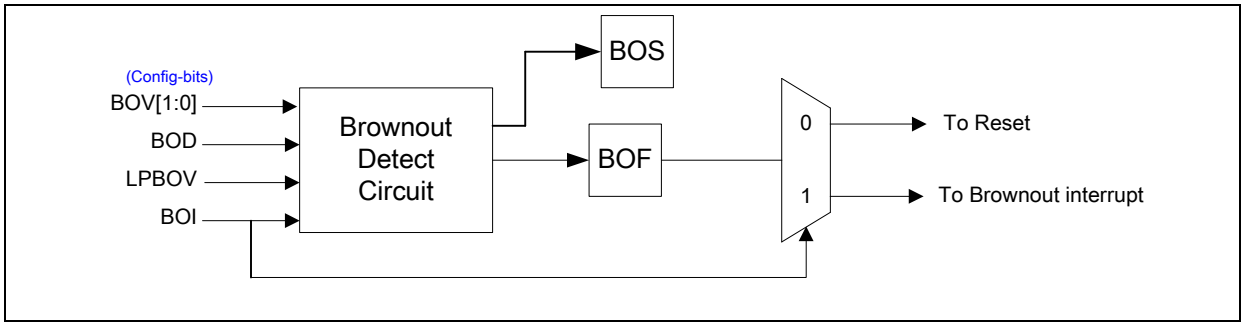


Figure 13-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it causes brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

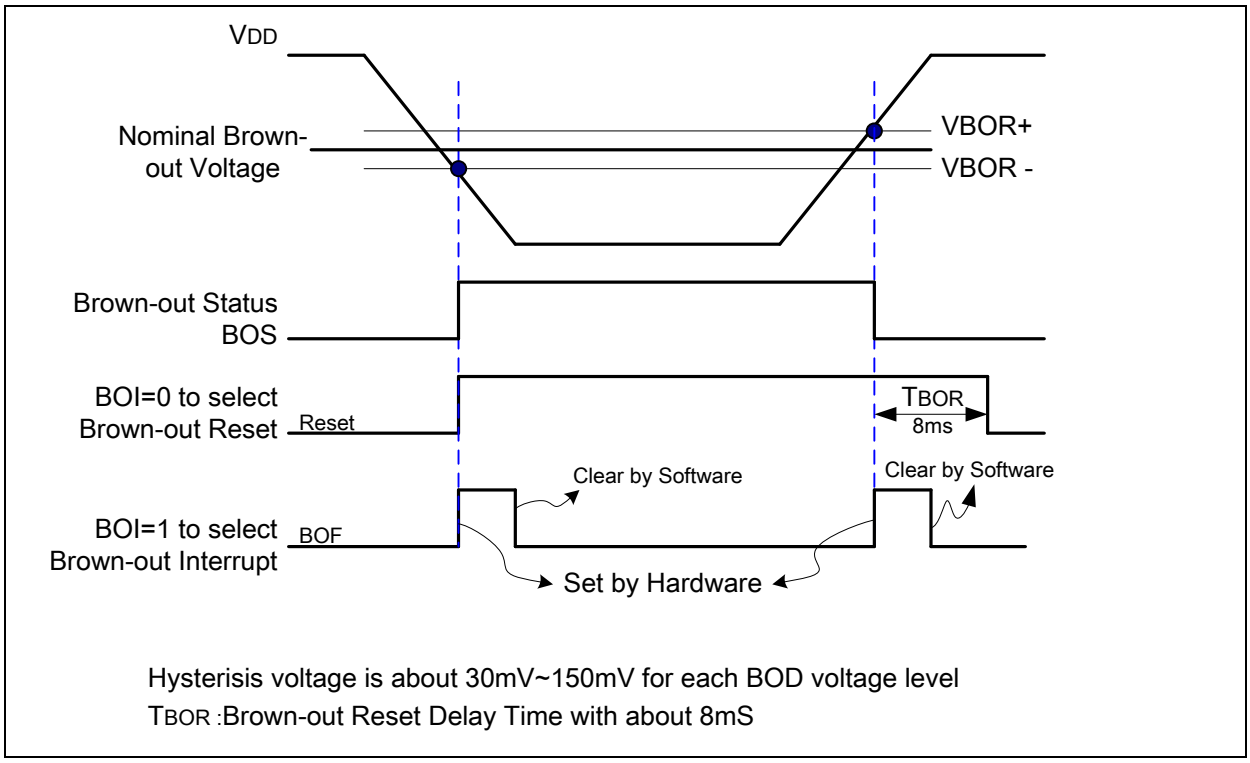


Figure 13-2: Brown-out Voltage Detection

13.3 SFR of Brown-out Detection

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	**BOD**	**BOI**	**LPBOD**	SRST	ADCEN	RCCLK	**BOS**	0X00 0000B
PCON	POWER CONTROL	87H	SMOD	SMOD0	**BOF**	POR	GF1	GF0	PD	IDL	00XX 0000B

14 NVM MEMORY

The N79E235 series have NVM data memory of **256** bytes for customer's data store used. The NVM data memory has **8** pages area and each page has **32** bytes. The page addresses are shown on Figure 14-1.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDAT and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which high and low byte address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDRL and NVMDAT, then set EWR of NVMCON.6 to initiate NVM data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

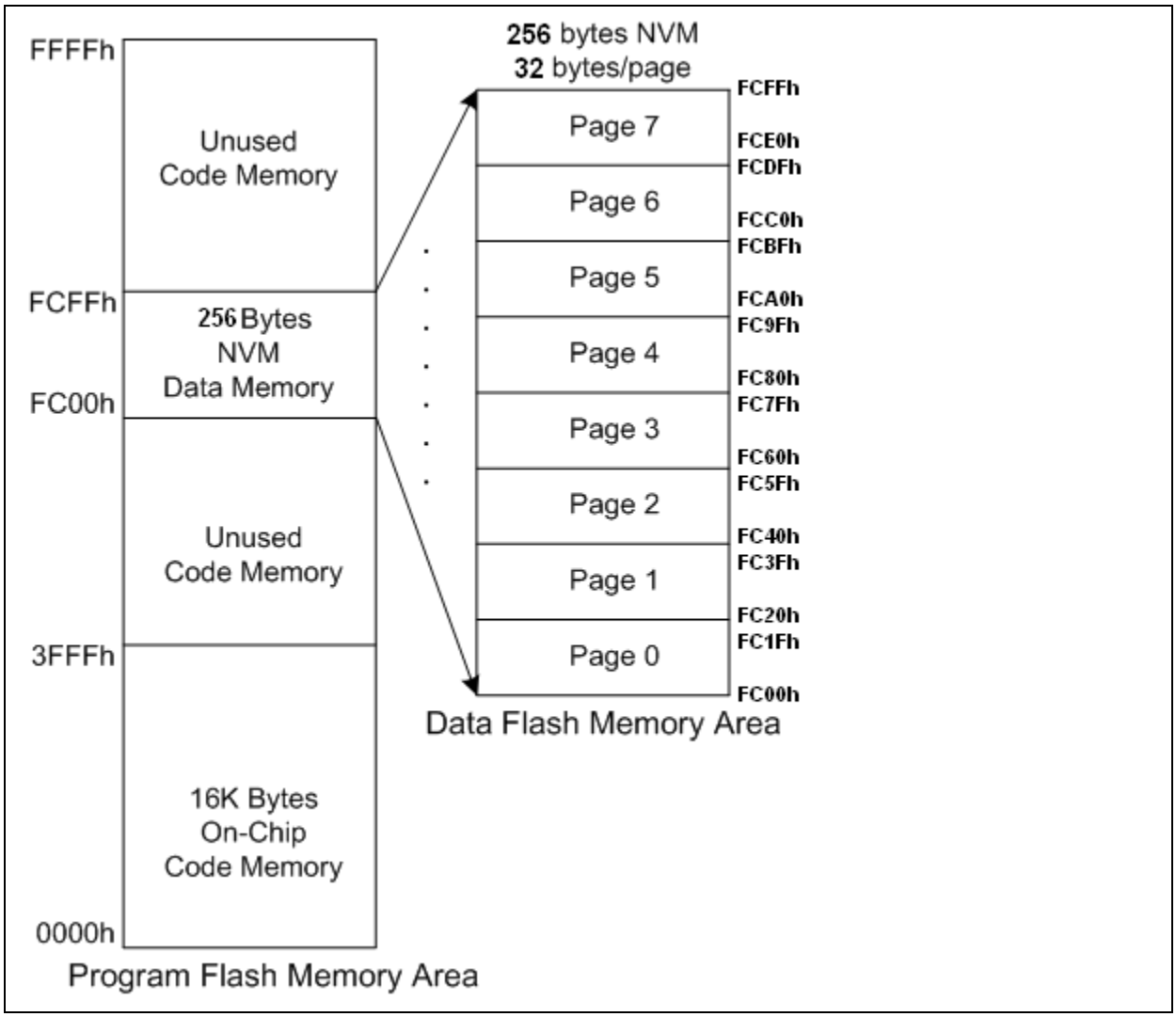


Figure 14-1 N79E235 On-chip Flash Memory Space

15 KEYBOARD INTERRUPT (KBI)

The N79E235 series provide 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the N79E235 series, as shown below figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

Keyboard function is supported through by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register, as shown below figure. The Keyboard Interrupt Flag, KBF in the AUXR1(A2H).7, is set when any enabled pin is triggered while the KBI interrupt function is active, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.

KBI1~KBI3 support both rising and falling edge detection, and the remaining pins support low level detection only.

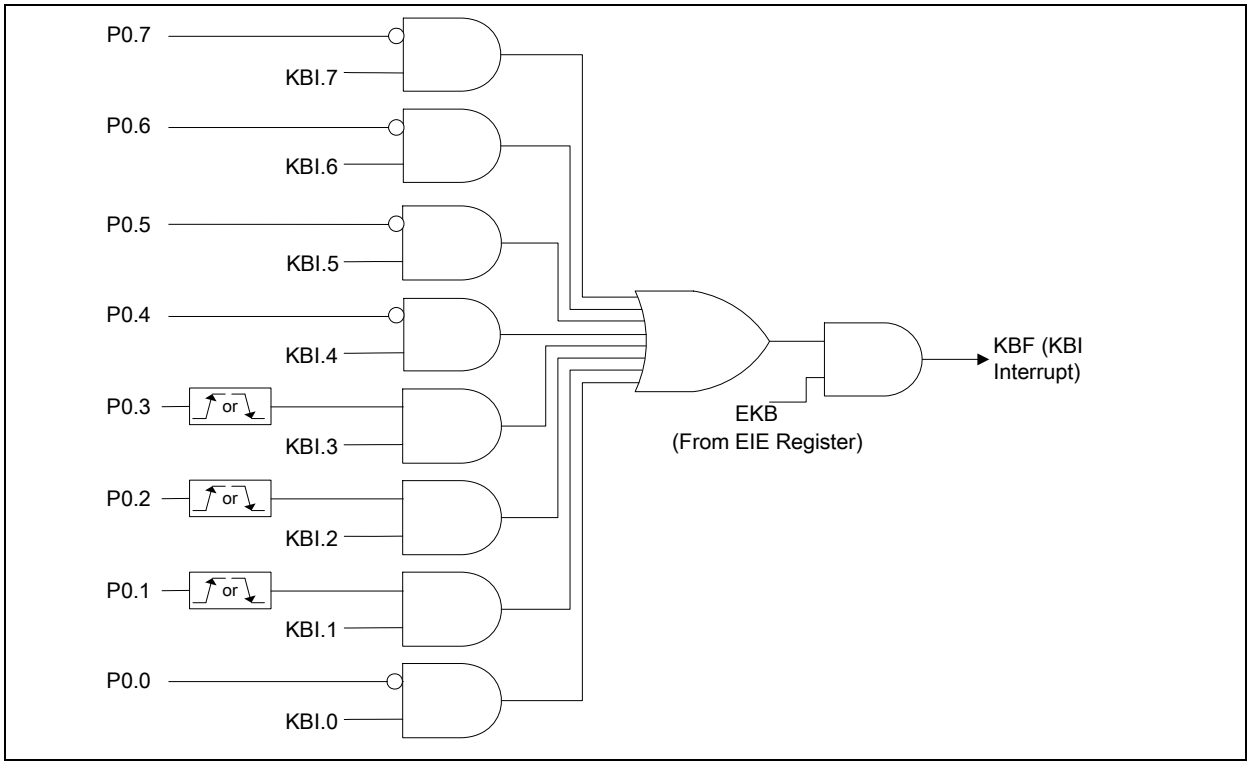


Figure 15-1: KBI inputs

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
AUXR1	AUX FUNCTION REGISTER 0	A2H	**KBF**	BOD	BOI	LPBOD	SRST	ADCEN	RCCLK	BOS	0X00 0000B
KBI	KEYBOARD INTERRUPT	A1H	**KBI.7**	**KBI.6**	**KBI.5**	**KBI.4**	**KBI.3**	**KBI.2**	**KBI.1**	**KBI.0**	0000 0000B

16 I/O PORT CONFIGURATION

N79E235 series have maximum **four** 8 bits I/O ports; port 0, port 1, port 2, port 3 and **one** partial port 4; P4.0 to P4.3. All pins of I/O ports can be configured to one of four types by software except **P1.4** is only input pin or set to reset pin. When P1.4 is configured reset pin by RPD=0 in the CONFIG0 register, the device can support 33 I/O pins by use Crystal. If used on-chip RC oscillator and the P1.4 is configured input pin, the device can be supported up to 36 I/O pins. The I/O ports configuration setting as below table.

PxM1.y	PxM2.y	Port Input/Output Mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Table 16-1: I/O port configuration table

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG0 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.4 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by **T0OE and T1OE on AUXR2** register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of N79E235 series may be selected to use TTL level inputs or Schmitt inputs by **P(n)S** bit on **PORTS** register; where n is **0, 1, 2, 3 or 4**. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The **P1.0** (XTAL2) can be configured as clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

P1.5 and **P1.6(/INT0)** that supported I2C are permanent open drain pins.

16.1 Quasi-Bidirectional Output Configuration

The default port output configuration for standard N79E235 series I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1.

When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again. The quasi-bidirectional port configuration is shown as below.

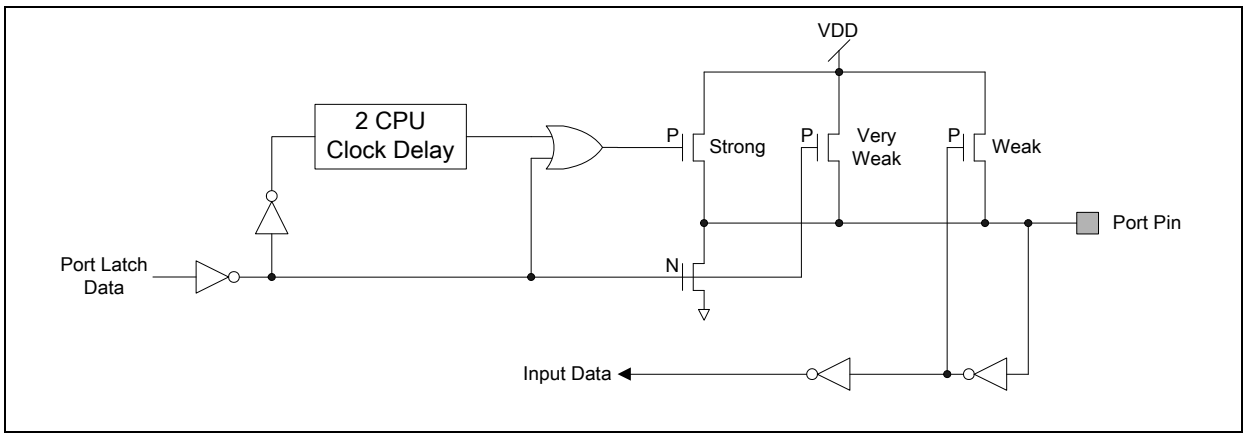


Figure 16-1: Quasi-Bidirectional Output

16.2 Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to VDD. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown as below.

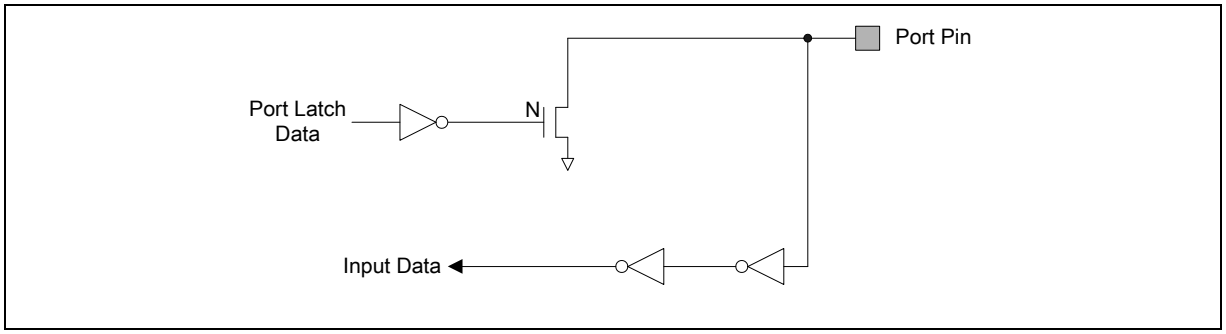


Figure 16-2: Open Drain Output

16.3 Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown below. One port pin that cannot be configured is P1.4. P1.4 may be used as a Schmitt trigger input if the device has been configured for an internal reset and is not using the external reset input function /RST.

The value of port pins at reset is determined by the PRHI bit in the CONFIG0 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current. Every output on the device may potentially be used as a **20mA** sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the device have slew rate controlled outputs. This is to limit noise generated by quickly

switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times. The PORTS SFR bits can enable Schmitt trigger inputs on each I/O port. The AUXR2 register has bits to enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in the Timer/Counters and Oscillator sections respectively. Each I/O port of this device may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pin P1.4 always has a Schmitt trigger input.

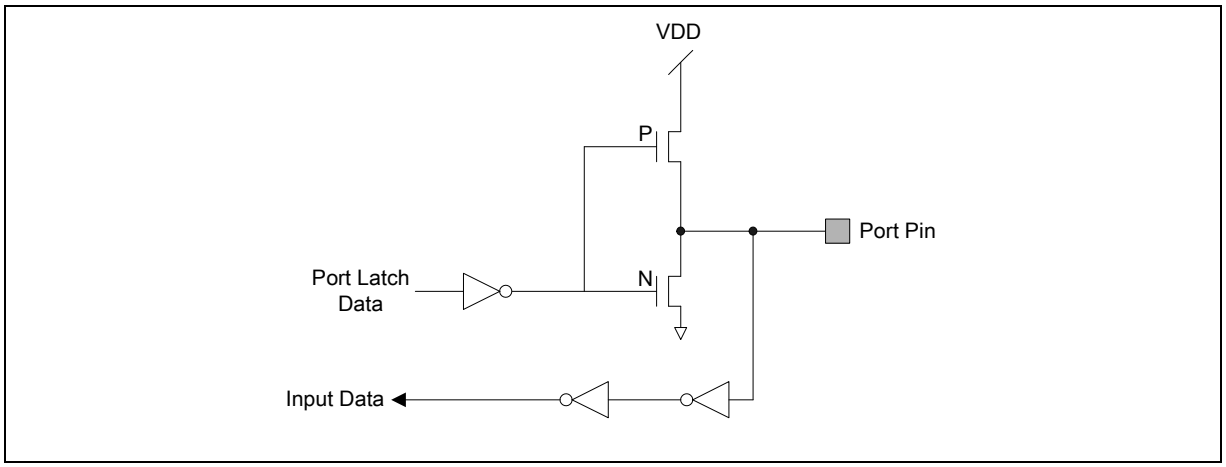


Figure 16-3: Push-Pull Output

16.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The N79E235 series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.

16.5 SFR of I/O Port Configuration

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
P4M2	PORT 4 OUTPUT MODE 2	FBH	-	-	-	-	P4M2.3	P4M2.2	P4M2.1	P4M2.0	XXXX 0000b
P4M1	PORT 4 OUTPUT MODE 1	FAH	-	-	-	-	P4M1.3	P4M1.2	P4M1.1	P4M1.0	XXXX 0000b
PORTS	PORT SHMITT REGISTER	ECH	-	-	-	P4S	P3S	P2S	P1S	P0S	XXX0 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	0000 0000b
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	0000 0000b
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	-	-	-	P1M2.3	P1M2.2	P1M2.1	P1M2.0	000X 0000b
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	-	-	-	P1M1.3	P1M1.2	P1M1.1	P1M1.0	000X 0000b
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000b
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	0000 0000b
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	0000 0000b

17 PROGRAMMABLE TIMERS/COUNTERS

The N79E235 series have two 16-bit programmable timer/counters which have additional timer 0 or timer 1 overflow toggle output enable feature as compare to conventional timer/counters. This timer overflow toggle output can be configured to automatically toggle T0 or T1 pin output whenever a timer overflow occurs.

17.1 TIMER/COUNTERS 0 & 1

N79E235 series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. For timer 0, the timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4, 1/16, 1/32, 1/128 (selectable through SFR DIV.T0DIV bits) of the system clock. As for timer 1, the timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

17.2 Time-Base Selection

N79E235 series provide users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on N79E235 series and the standard 8051 can be matched. This is the default mode of operation of the N79E235 series timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed (timer 1) or rate of 1/4,1/16,1/32,1/128 clock speed (timer 0). This will straight-away increase the counting speed up to three times. This selection is done by the T0M and T1M bit in CKCON SFR, and T0DIV bits in DIV SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits accordingly if the timers are to operate in turbo mode.

17.3 MODE 0

In Mode 0, the timer/counters act as an 8-bit counter with a 5-bit, divide by 32 pre-scale. In this mode we have a 13-bit timer/counter. The 13-bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set

and either GATE = 0 or $\overline{INTx}$ = 1. When C/$\overline{T}$ is set to 0, then it will count clock cycles, and if C/$\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P1.5) for timer 0 and T1 (P2.7) for timer 1. When the 13-bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur.

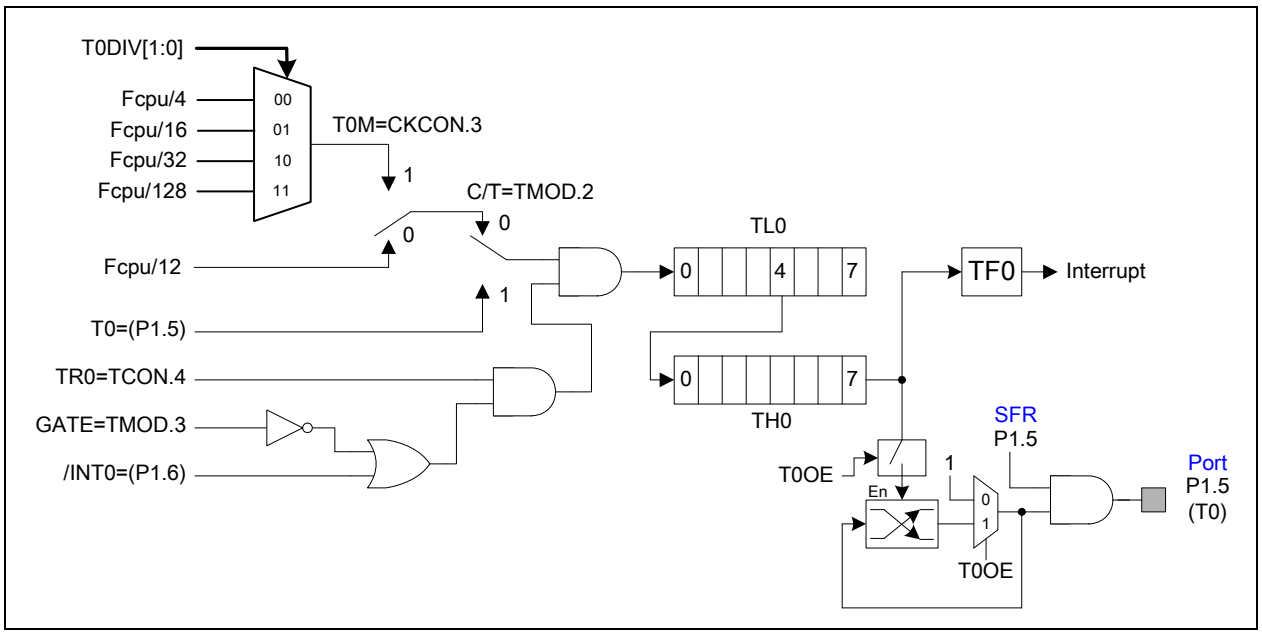


Figure 17-1 Timer 0 Mode 0

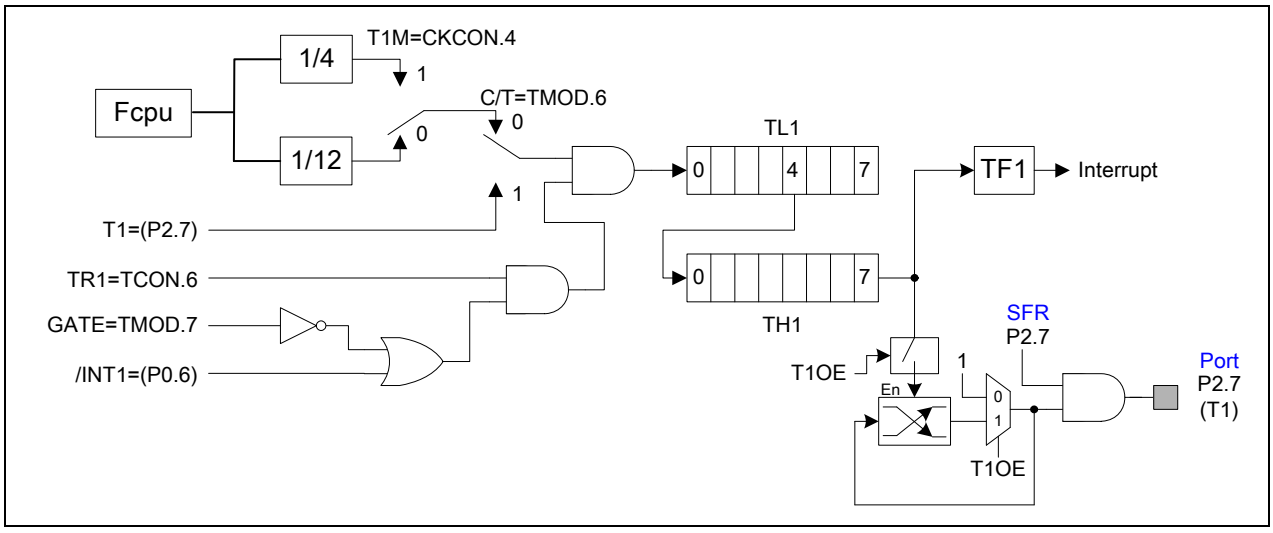


Figure 17-2 Timer 1 Mode 0

17.4 MODE 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

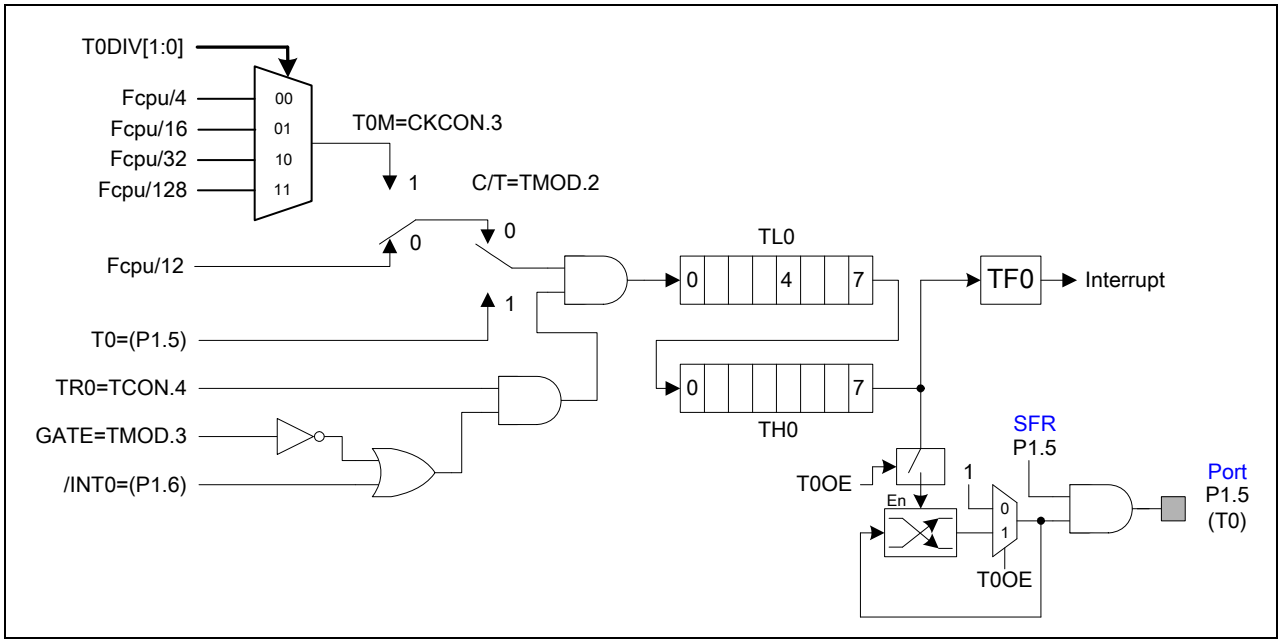


Figure 17-3 Timer 0 Mode 1

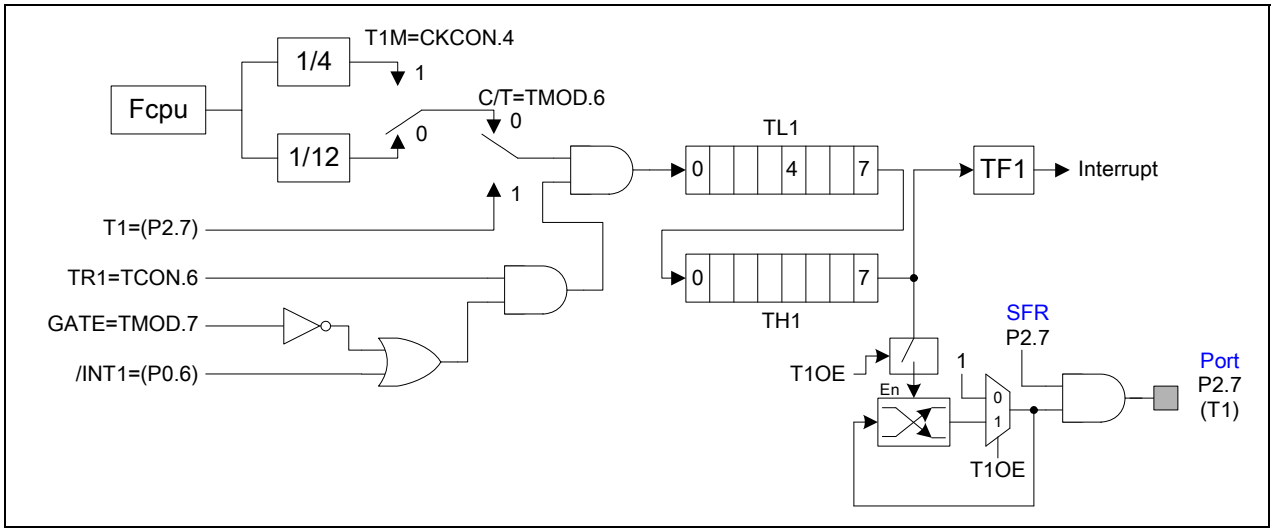


Figure 17-4 Timer 1 Mode 1

17.5 MODE 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1, mode 2 allows counting of either clock cycles or pulses on pin Tn.

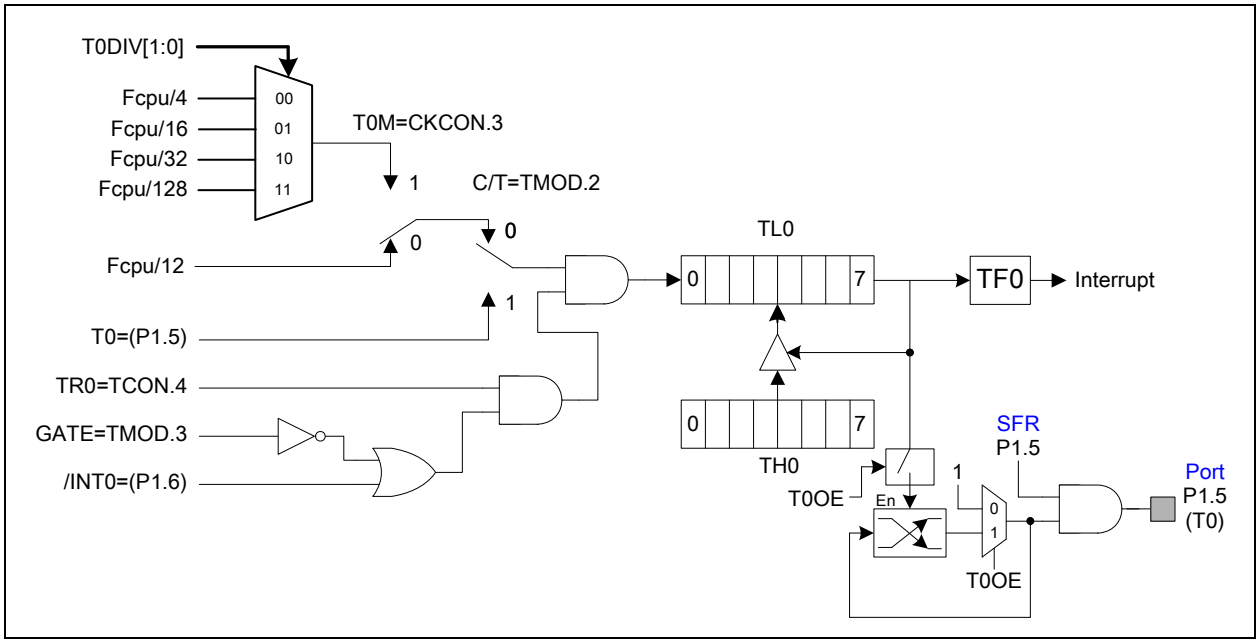


Figure 17-5 Timer 0 Mode 2 (8-bit Auto-reload Mode)

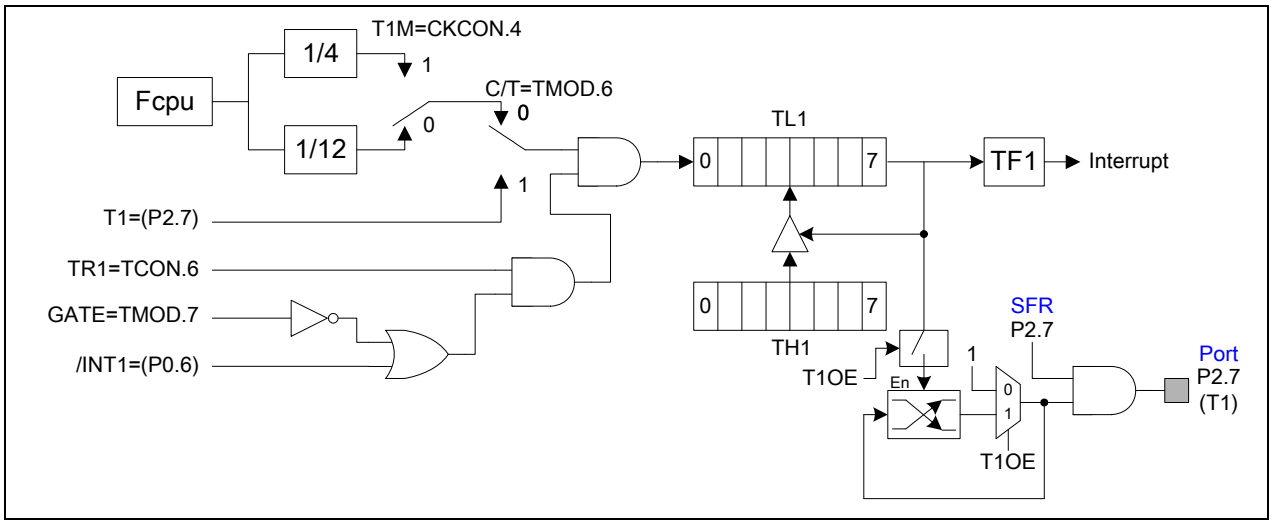


Figure 17-6 Timer 1 Mode 2 (8-bit Auto-reload Mode)

17.6 MODE 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. When timer 0 configure to mode 3, the TL0 can be used to count clock cycles (clock/12 or clock/4,16,32,128) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4,16,32,128) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0-2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1.

Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

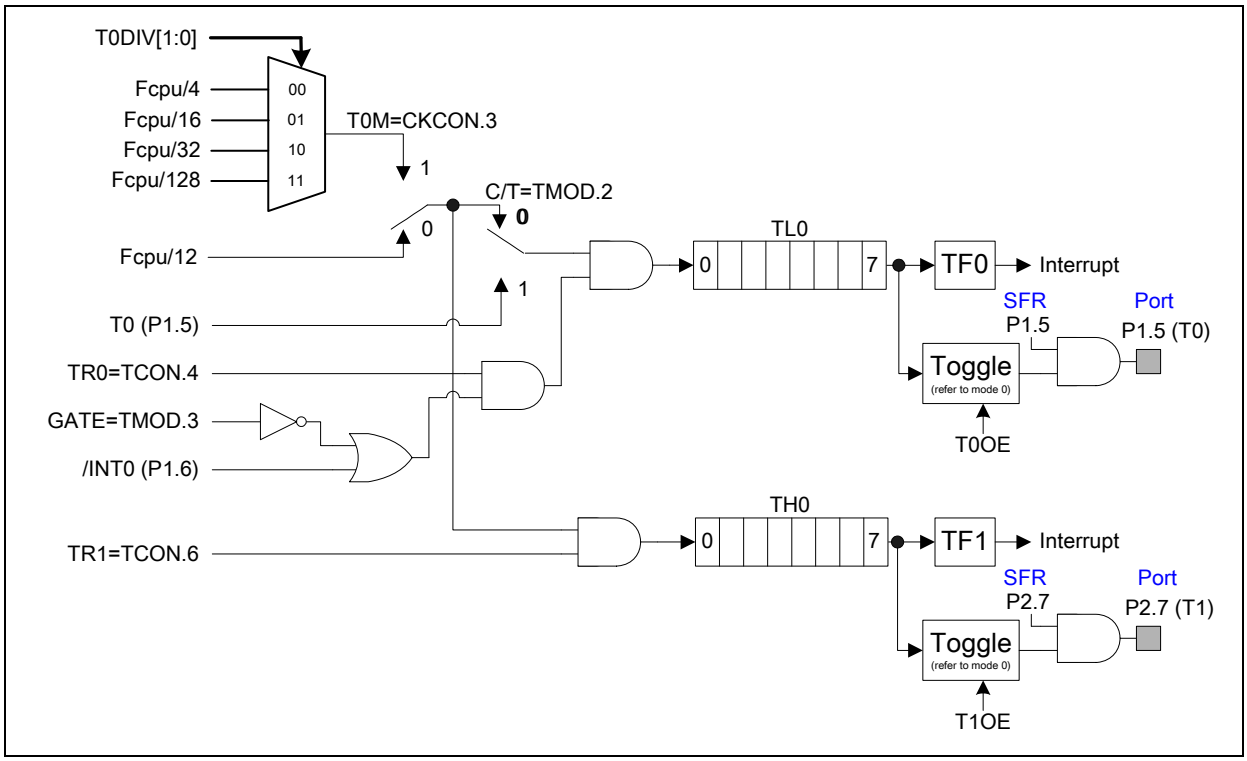


Figure 17-7 Timer 0 Mode 3 (Two 8-bit Counters)

18 TIMER2/INPUT CAPTURE MODULES

Timer/Counter 2 is a 16 bit up counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is also equipped with 3 input captures and reloads capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 crystal oscillator is divided by 1,4,16 or 32 (selectable with CCDIV.1~0 in DIV SFR). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

18.1 Capture Mode

The capture modules are function to detect and measure pulse width and period of a square wave. It supports 3 capture inputs and digital noise rejection filter. The modules are configured by CAPCON0 and CAPCON1 SFR registers. Input Capture 0, 1 & 2 have their own edge detector but share with one timer i.e. Timer 2. If the Schmitt trigger enable bits at SFR PORTS are set, the Input Capture pins are in the structure with Schmitt trigger. For this operation it basically consists of;

- 3 capture module function blocks
- Timer 2 block

Each capture module block consists of 2 bytes capture registers, noise filter and programmable edge triggers. Noise Filter is used to filter the unwanted glitch or pulse on the trigger input pin. The noise filter can be enabled through CAPCON1.ENFx bit. If enabled, the capture logic required to sample 4 consecutive same capture input value in order to recognize an edge as a capture event. A possible implementation of digital noise filter is as follow;

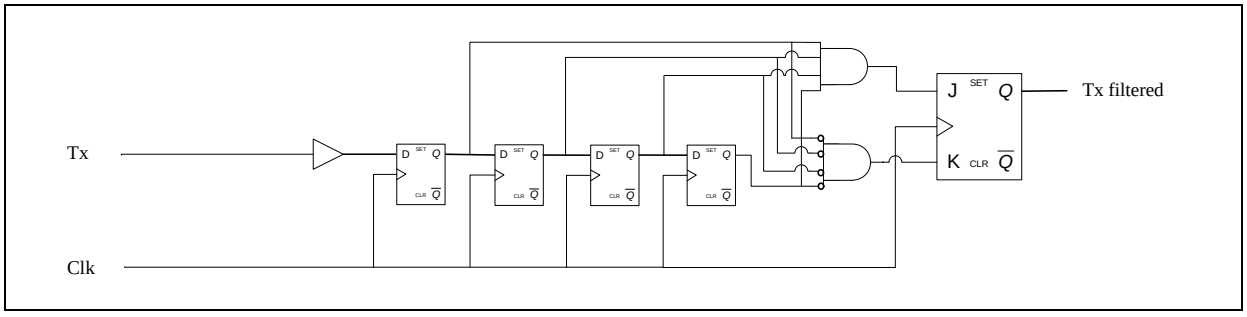


Figure 18-1 Noise filter

The interval between pulses requirement for input capture is 1 machine cycle width, which is the same as the pulse width required to guarantee a trigger for all trigger edge mode. For less than 3 system clocks, anything less than 3 clocks will not have any trigger and pulse width of 3 or more but less than 4 clocks will trigger but will not guarantee 100% because input sampling is at stage C3 of the machine cycle.

The trigger option is programmable through CAPCON0.CCTx.1~0 bits. It supports positive edge, negative edge and both edge triggers. Each capture module consists of an enable, ICEN0-2.

[Note: x=0/1/2, for capture 0/1/2 block].

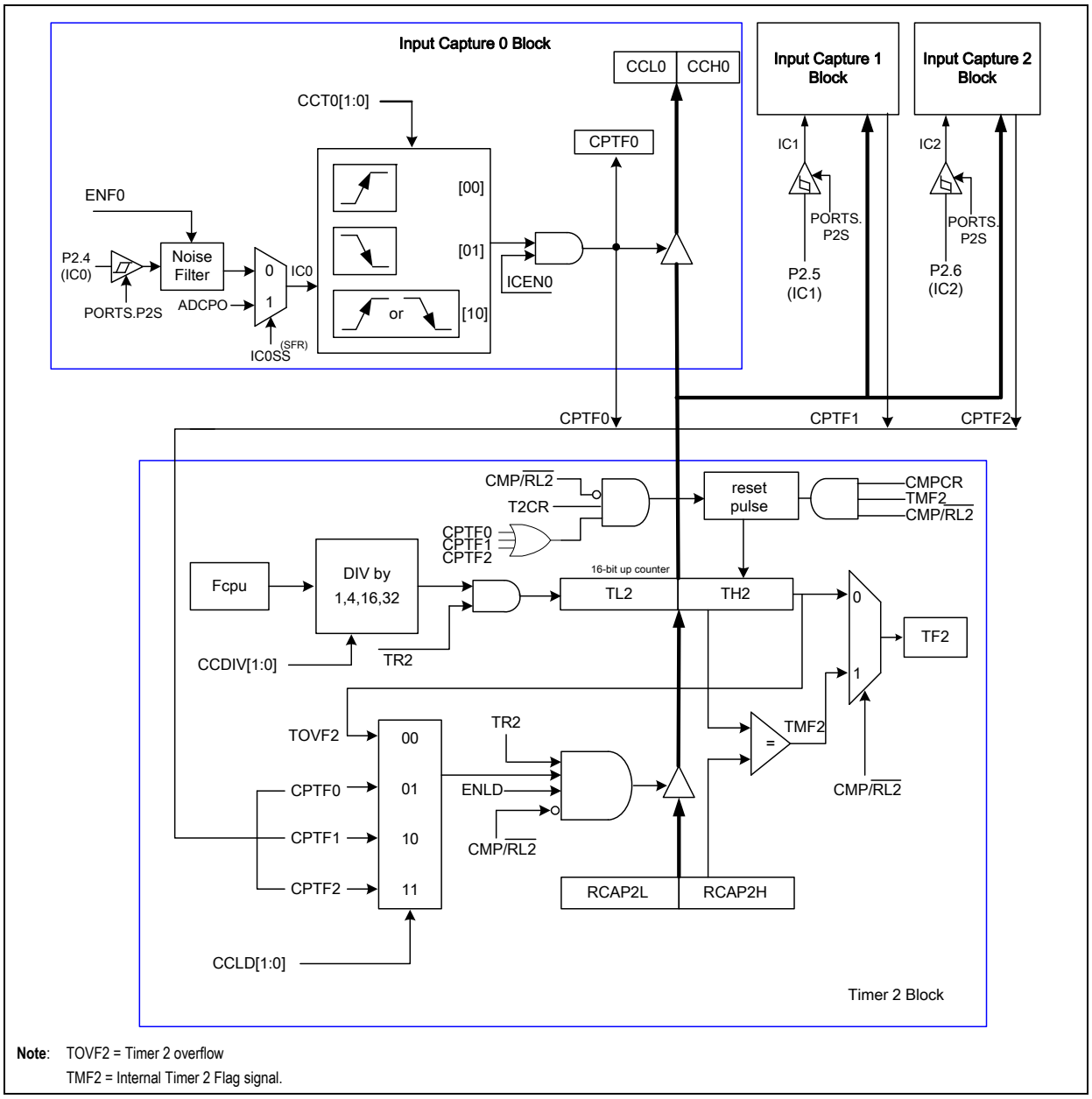
Timer/Counter 2 serves as a 16 bit up counter. It supports reload and compared modes. More details are described in next sections.

Capture blocks can be triggered by the following pins/bit;

- IC0 (P2.4) or ADC compare result bit, ADCPO.
- IC1 (P2.5)
- IC2 (P2.6)

If ICENx is enabled, each time the external pin trigger, the content of the free running 16 bits counter, TL2 & TH2 (from Timer 2 block) will be captured/transferred into the capture registers, CCLx and CCHx, depending which external pin trigger. This action also causes the CPTFx flag bit in CAPCON1 to be set, which will also generate an interrupt (if enabled by ECPTF bit in SFR EIE1.7). The CPTF0-2 flags are logical “OR” to the interrupt module. Flag is set by hardware and clear by software. Software will have to resolve on the priority of the interrupt flags.

Setting the T2CR bit (T2MOD.3), will allow hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured. Priority is given to T2CR to reset counter after capture the timer value into the capture register.



Note: TOVF2 = Timer 2 overflow
TMF2 = Internal Timer 2 Flag signal.

Figure 18-2 Timer2/capture modules

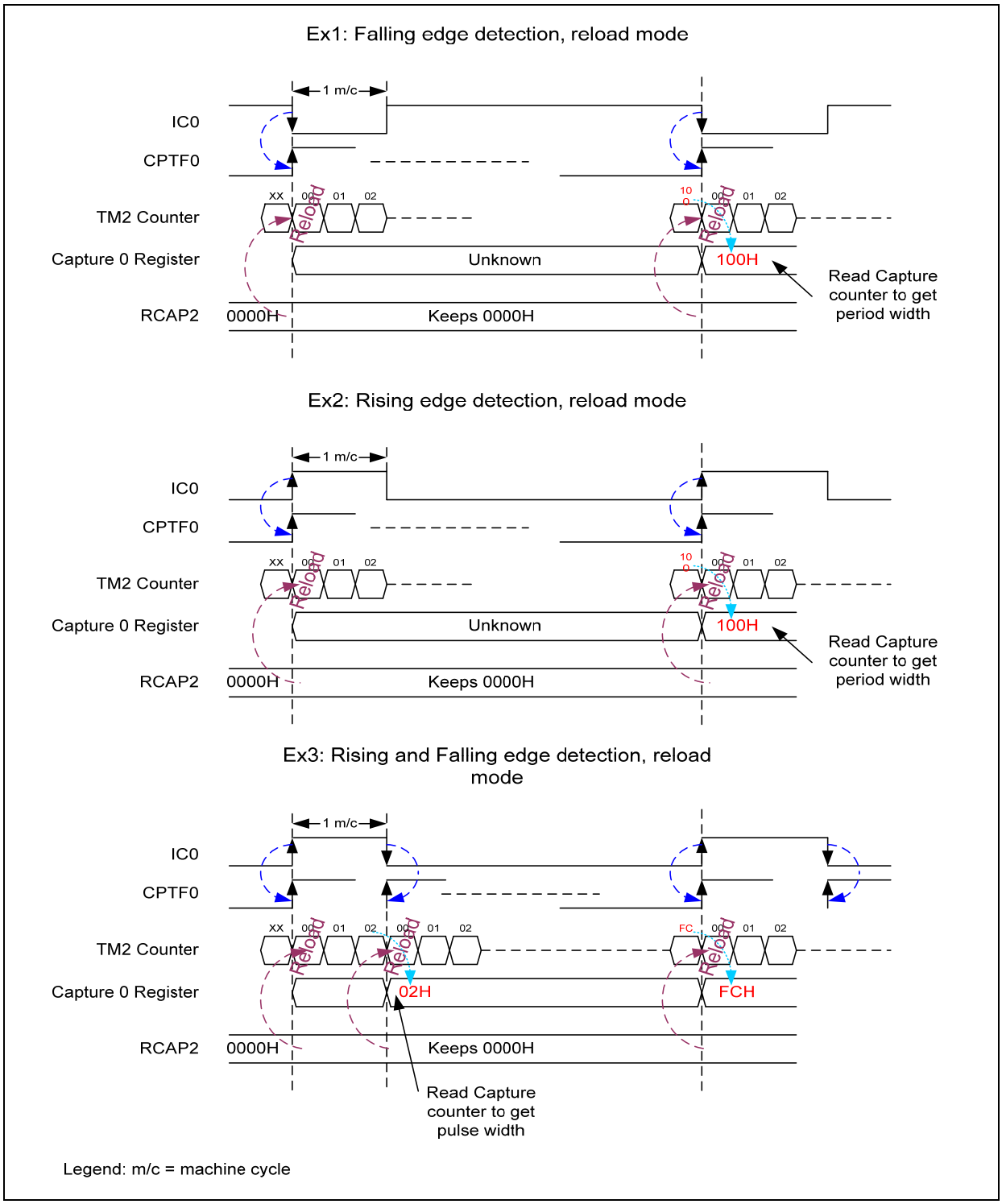


Figure 18-3 Timing diagram for Input Capture, IC0

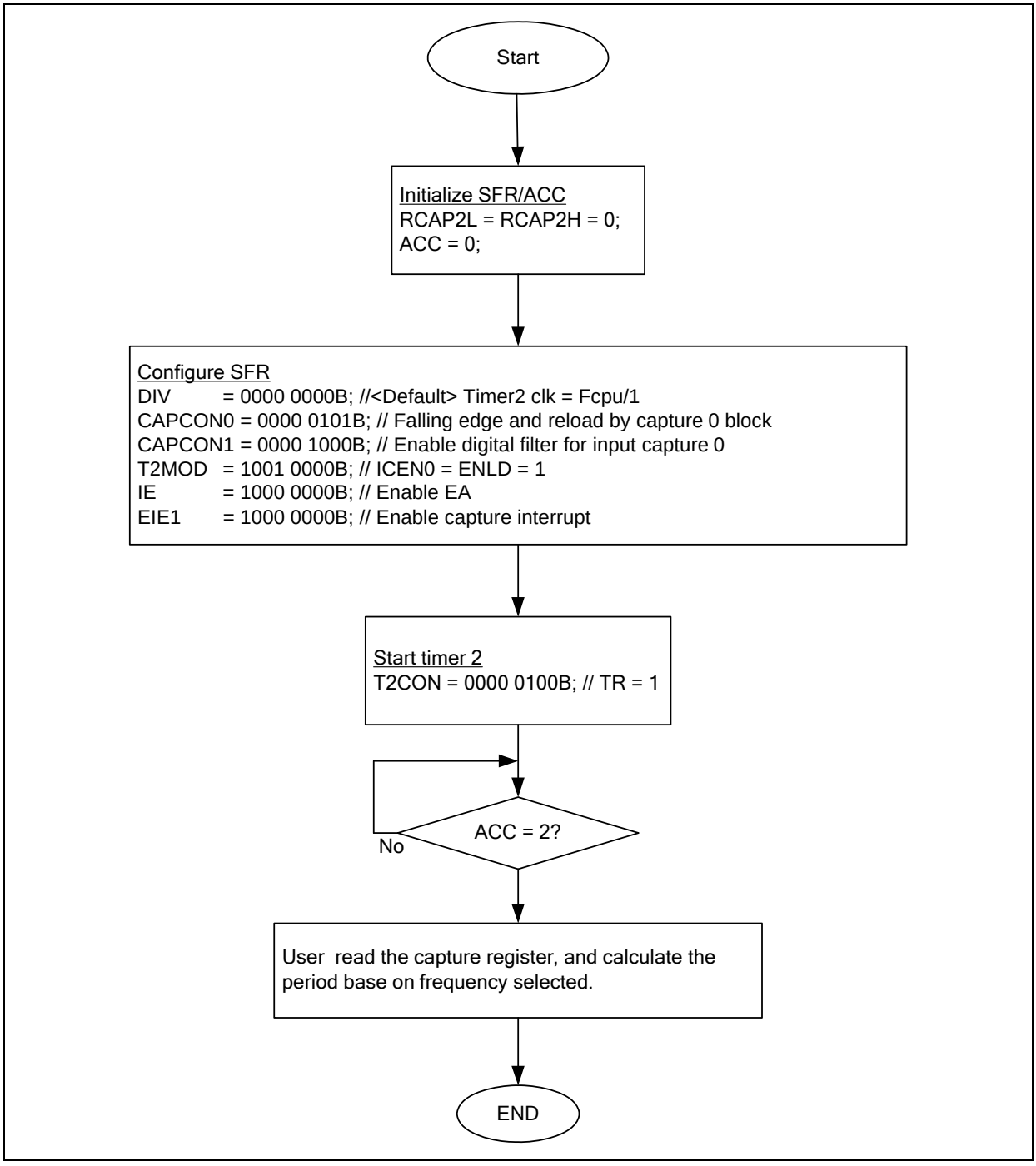


Figure 18-4 Program flow for measurement with IC0 between pulses with falling edge detection (ACC is incremented in interrupt service routine).

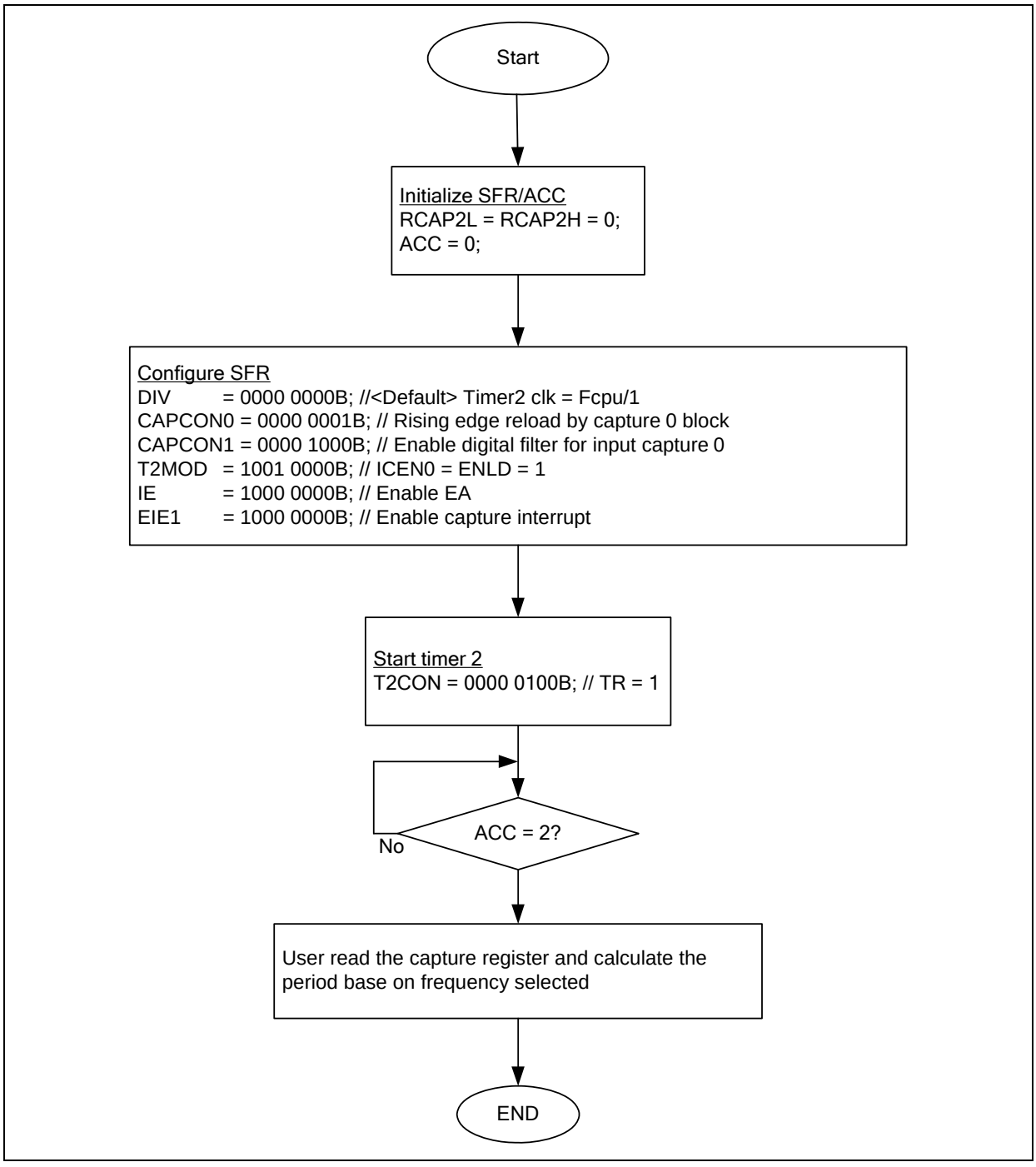


Figure 18-5 Program flow for measurement with IC0 between pulses with rising edge detection (ACC is incremented in interrupt service routine).

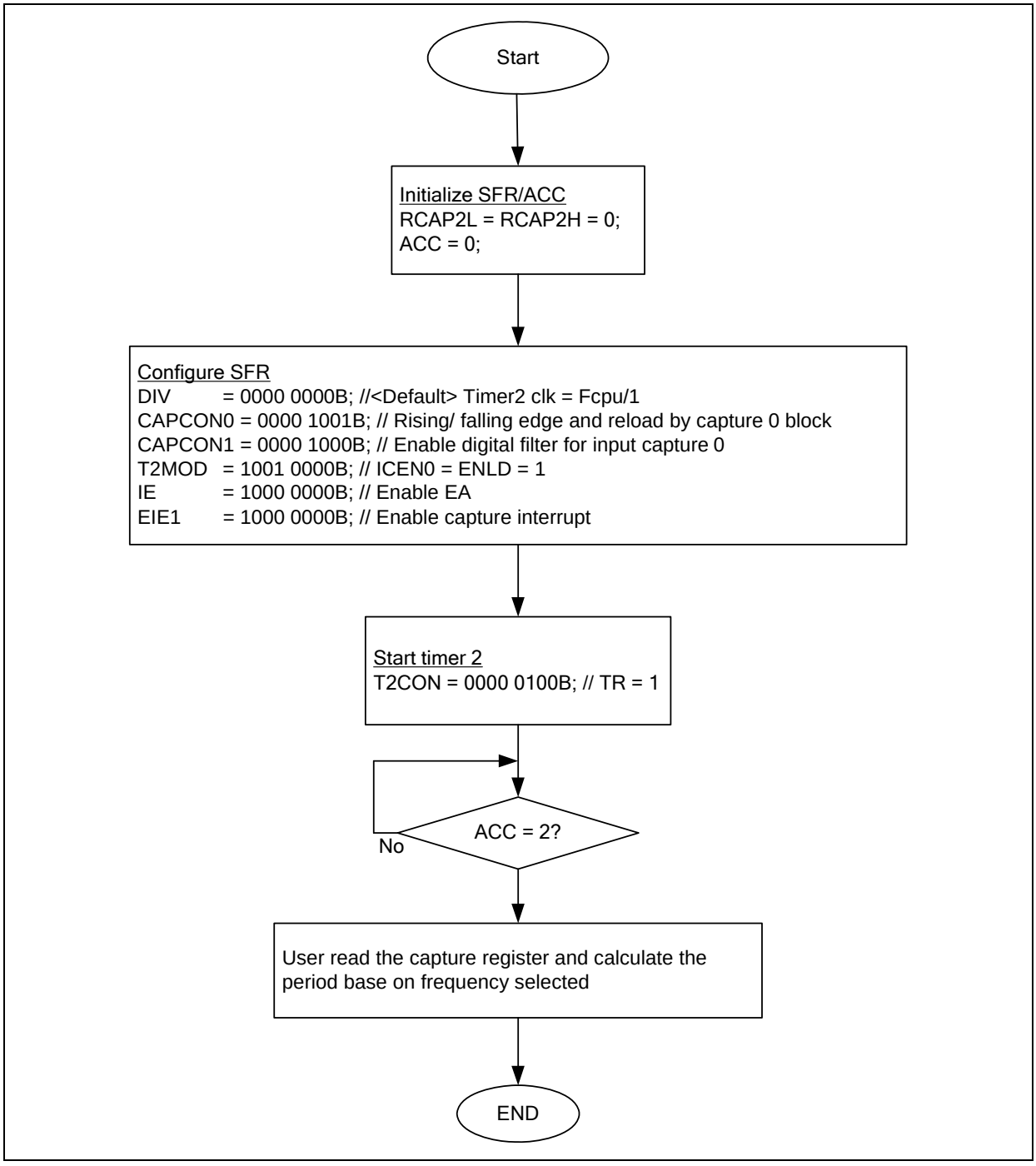


Figure 18-6 Program flow for measurement with IC0 pulse width with rising and falling edge detection (ACC is incremented in interrupt service routine).

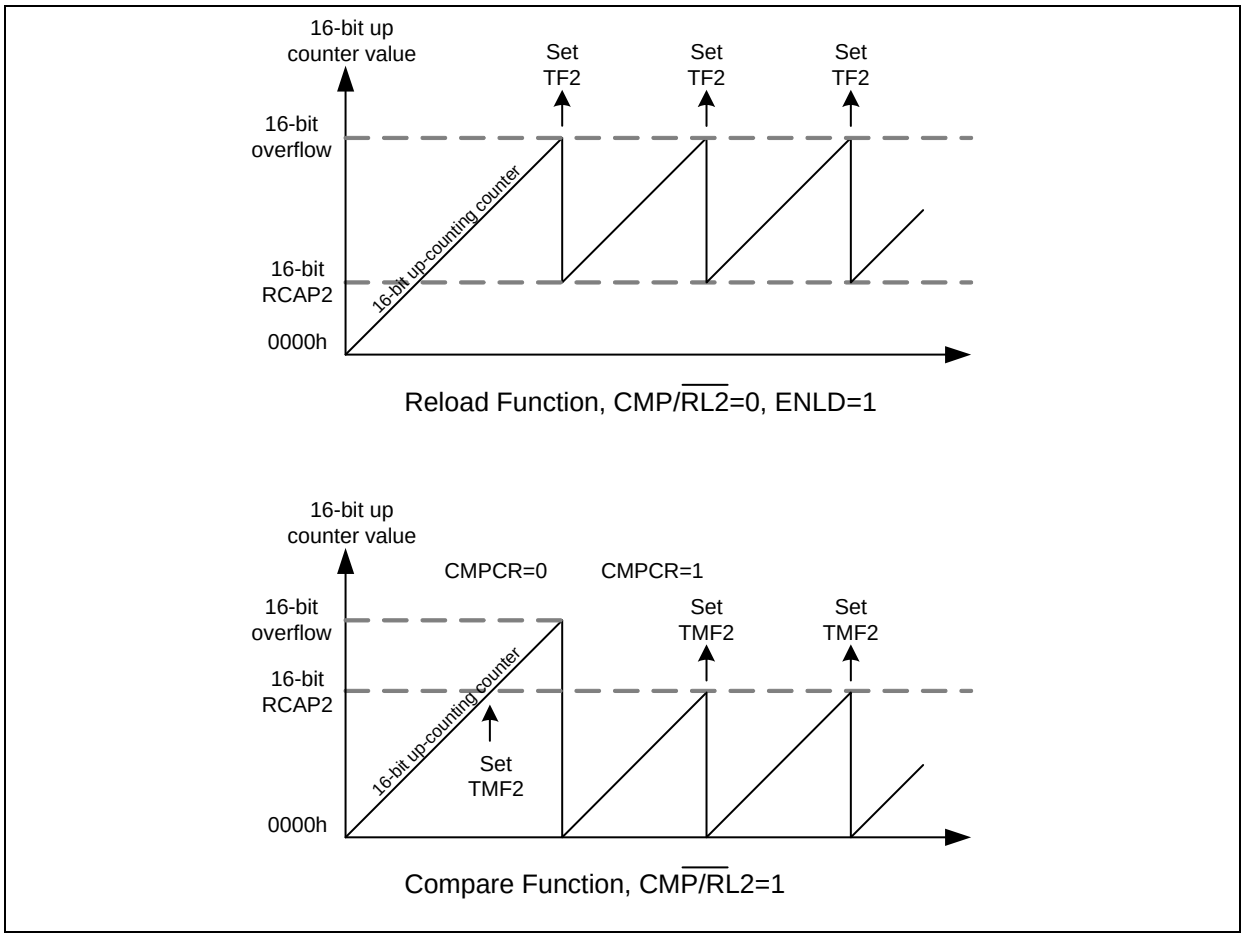


Figure 18-7 Timer 2 - Compare/Reload Function

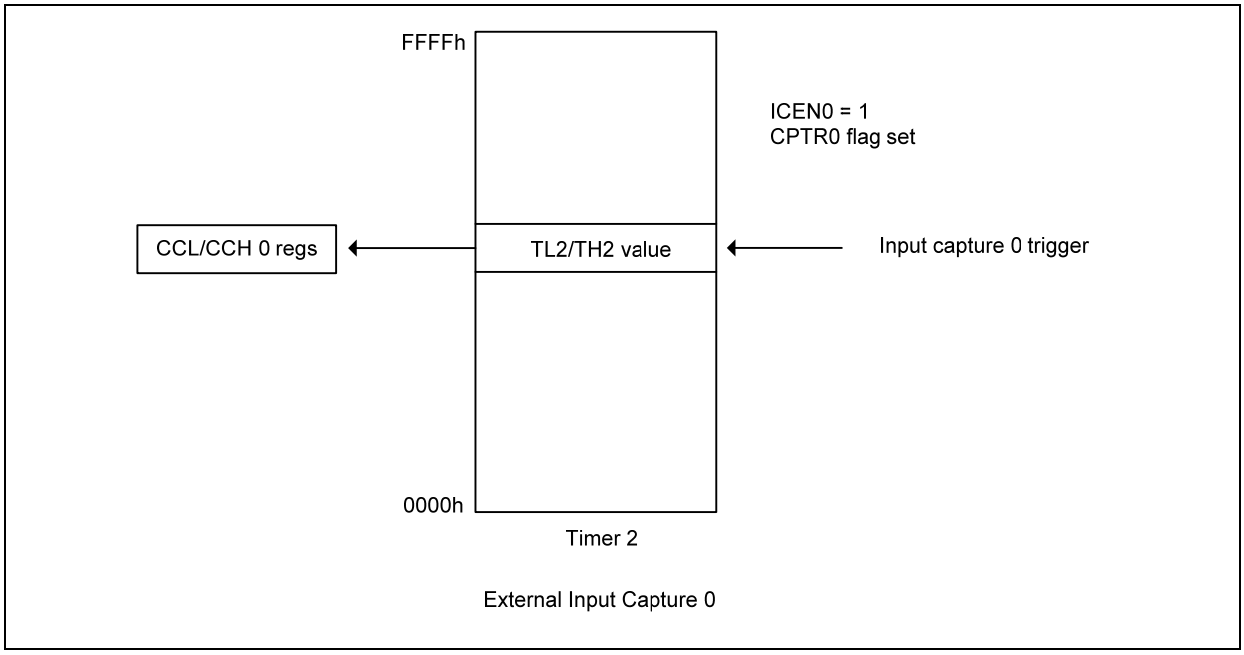


Figure 18-8 Capture module - Input Capture 0 triggers

18.2 Compare Mode

Timer 2 can be configured for compare mode. The compare mode is enabled by setting the CMP/RL2 bit to 1 in the T2CON register. RCAP2 will serves as a compare register. As Timer 2 counting up, upon matching with RCAP2 value, TF2 will be set (which will generate an interrupt request if enable Timer 2 interrupt ET2 is enabled) and the timer reload from 0 and starts counting again.

Setting the CMPCR bit (T2MOD.2), will allow hardware to reset timer 2 automatically after a match has occurred.

18.3 Reload Mode

Timer 2 can be also be configured for reload mode. The reload mode is enabled by clearing the CMP/RL2 bit to 0 in the T2CON register. In this mode, RCAP serves as a reload register. When timer 2 overflows, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers, if ENLD is set. TF2 flag is set, and interrupt request is generated if enable Timer 2 interrupt ET2 is enabled. However, if ENLD = 0, timer 2 will be reload with 0, and count up again.

Alternatively, other reload source is also possible by the input capture pins by configuring the CCLD.1~0 bits. If the ICENx bit is set, then a trigger of external IC0, IC1 or IC2 pin (respectively) will also cause a reload. This action also sets the CPTF0, CPTF1 or CPTF2 flag bit in SFR CAPCON1, respectively.

19 TIMER3

This device consists of an additional timer; Timer 3. Timer 3 is a 12-bit up counter which supports operation in any one of four possible modes: Timer/counter mode, capture mode, auto-reload mode and compare mode.

SFR T3CON.1~0	T3 mode	T3RST = 0	T3RST = 1
00b	Timer/Counter mode	Timer 3 counts from 000h to FFFh.	
01b	Capture mode	RCAP3L, RCAP3HT3H.7-4 capture content of timer 3. Timer 3 counts from 000h to FFFh.	RCAP3L, RCAP3HT3H.7-4 capture content of timer 3. Timer 3 reset after capture occurs.
10b	Auto-reload mode	RCAP3L, RCAP3HT3H.7-4 serve as reload registers. Timer 3 counts from reload registers content to FFFh.	
11b	Compare mode	RCAP3L, RCAP3HT3H.7-4 serve as compare registers. Timer 3 counts from 000h to FFFh.	RCAP3L, RCAP3HT3H.7-4 serve as compare registers. Timer 3 counts from 000h to compare value.

The following figure shows the timer 3 block diagram.

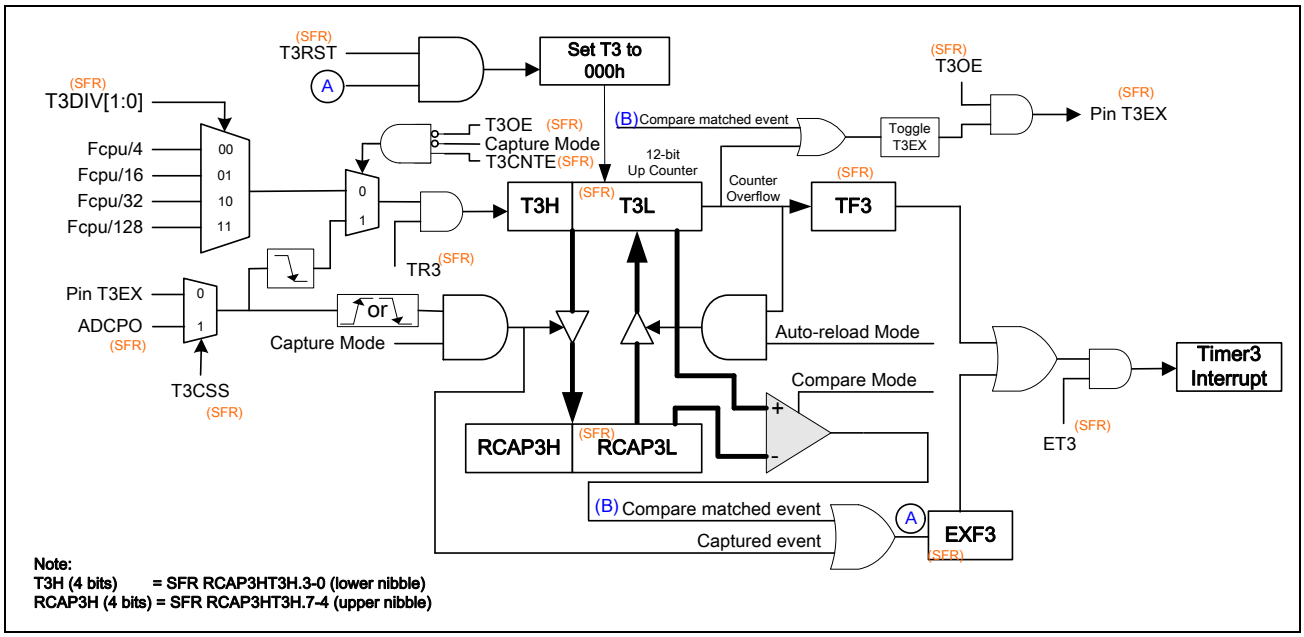


Figure 19-1: Timer 3 block diagram

Note: Timer 3 counter is writable only when TR3 = 0.

The timer clock can be programmed to be of 1/4, 1/16, 1/32 and 1/128 of the Fcpu clock.

19.1 Timer/Counter Mode

Timer 3 has one 8 bits register and 4 bits register forming the 12 bits counting registers. There bits are located at SFR T3L (LSB bits) and RCAP3HT3H.3-0 (MSB bits). The timer can be configured to operate either as timer or as counter counting external input.

The "Timer" or "Counter" function is selected by the T3CNTE bit in the T3CON Special Function Register.

When configured as a "Timer", the timer counts clock cycles. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T3. The T3 input is sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented.

When enable T3OE, T3 pin is toggled whenever timer 3 overflow (or compare matched occurs).

19.2 Capture Mode

In this mode, each time external pin T3 triggers (either rising or falling edge), the content of timer 3 will be captured/transferred into capture registers, RCAP3L.7-0 and RCAP3HT3H.7-4. This event will caused EXF3 flag bit in SFR T3CON.6 to be set, which will also generate an interrupt if enabled by ET3 bit (EIE2.0). The flag is set by hardware and clear by software. Setting T3RST bit (T3CON.3), will allow hardware to reset timer 3 automatically after the values of timer 3 has been captured. Otherwise, the timer 3 continues counting.

ADC compare result, ADCPO, is another alternative source for capture mode. It is selected by T3CSS bit.

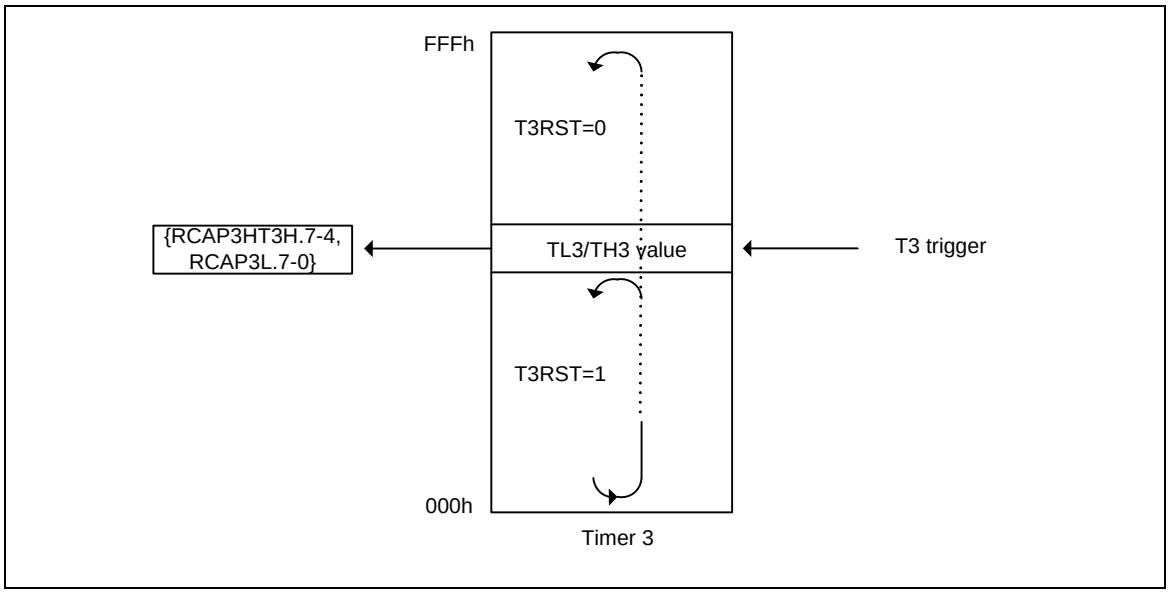


Figure 19-2: Timer 3 – capture function

19.3 Compare Mode

In this mode, RCAP3L and RCAP3HT3H.7-4 serve as compare registers. As timer 3 counting up, upon matching the compare registers, EXF3 flag will also be set. Similarly, an interrupt will be generated if enabled by ET3 bit (EIE2.0). If T3RST = 0, the timer 3 will continue count up, until overflow follow by count up again from zero. Setting T3RST bit, will allow hardware to reset timer 3 automatically after there is compare matched.

When enable T3OE, T3 pin is toggled whenever compare matched occurs (or timer 3 overflows).

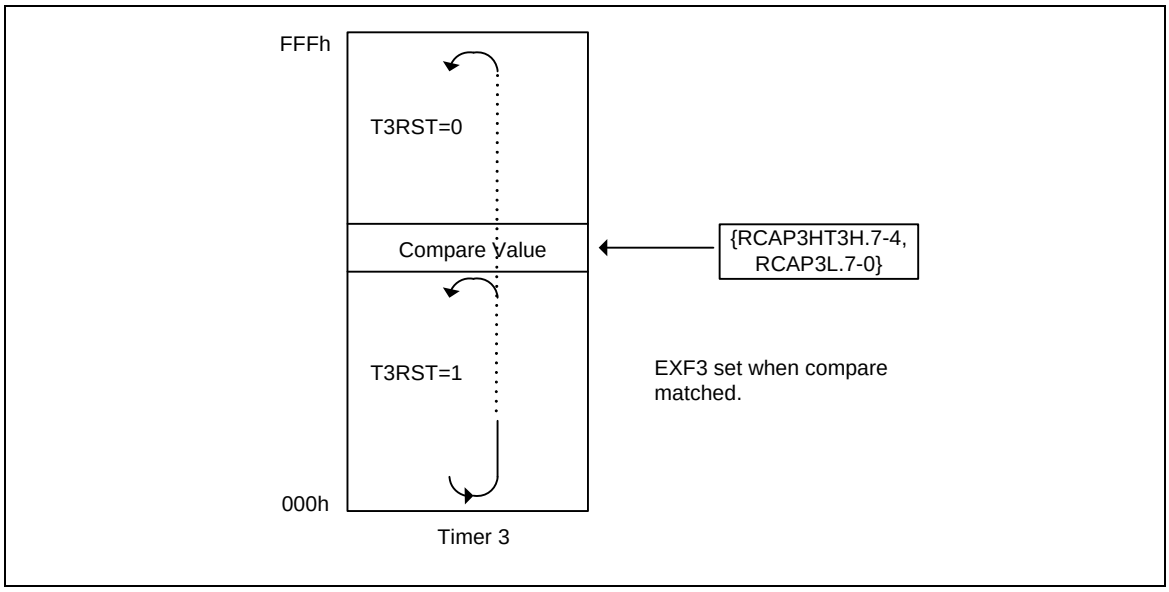


Figure 19-3: Timer 3 – compare function

19.4 Auto-reload Mode

In this mode, RCAP3L and RCAP3HT3H.7-4 serve as reload registers. When timer 3 overflows, a reload is generated that causes the content of RCAP3L and RCAP3HT3H.7-4 reloaded to T3L and RCAP3HT3H.3-0. TF3 flag is set, and interrupt request is generated if ET3 bit is enabled.

20 WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set and WDT interrupt is requested if WDT interrupt is enabled(EIE.EWDI=1) and global interrupt is enabled(EA=1),and a system reset can also be caused if it is enabled. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

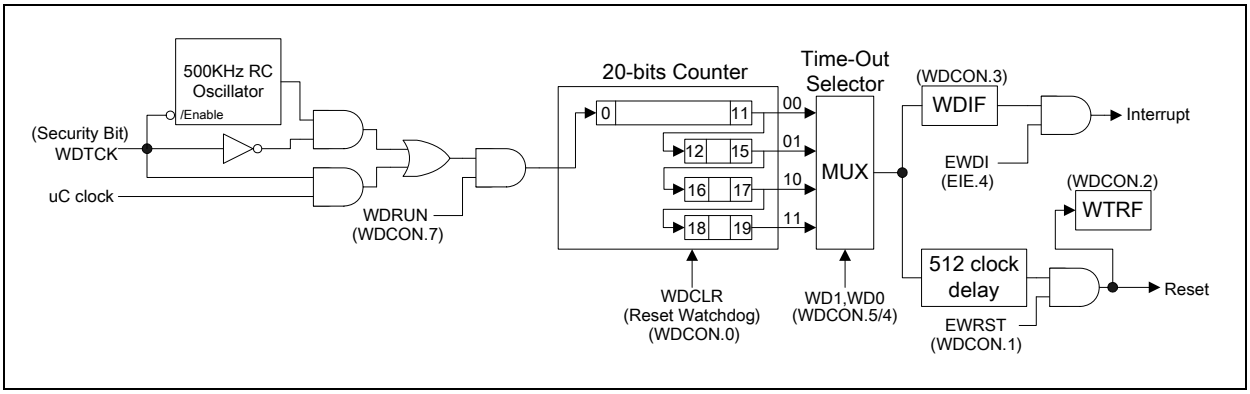


Figure 20-1 Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the hardware will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the

Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset will occur, when enabled, 512 clocks after the time-out has occurred.

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 10 MHZ
0	0	2^{12}	4096	0.4096 mS
0	1	2^{16}	65536	6.5536 mS
1	0	2^{18}	262144	26.2144 mS
1	1	2^{20}	1048576	104.8576 mS

Table 20-1 Time-out values for the Watchdog timer.

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state. The control bits that support the Watchdog Timer are discussed on the following section.

20.1 WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE14), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

The WDCON SFR is set to a 0x000000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

Reset Type	By external reset	By Watchdog reset	By Power on reset

Value after the reset	0x00 0x00b	0x00 0100b	0x00 000b

20.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{12} clocks, which is the shortest time-out period. The WDRUN, WD0, WD1, EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG0 register. This bit is for user to configure the clock source of watchdog timer either from the internal RC or from the uC clock.

21 SERIAL PORT (UART)

Serial port in the N79E235 series is a full duplex port. It provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode, N79E235 series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

21.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and N79E235 series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the device. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

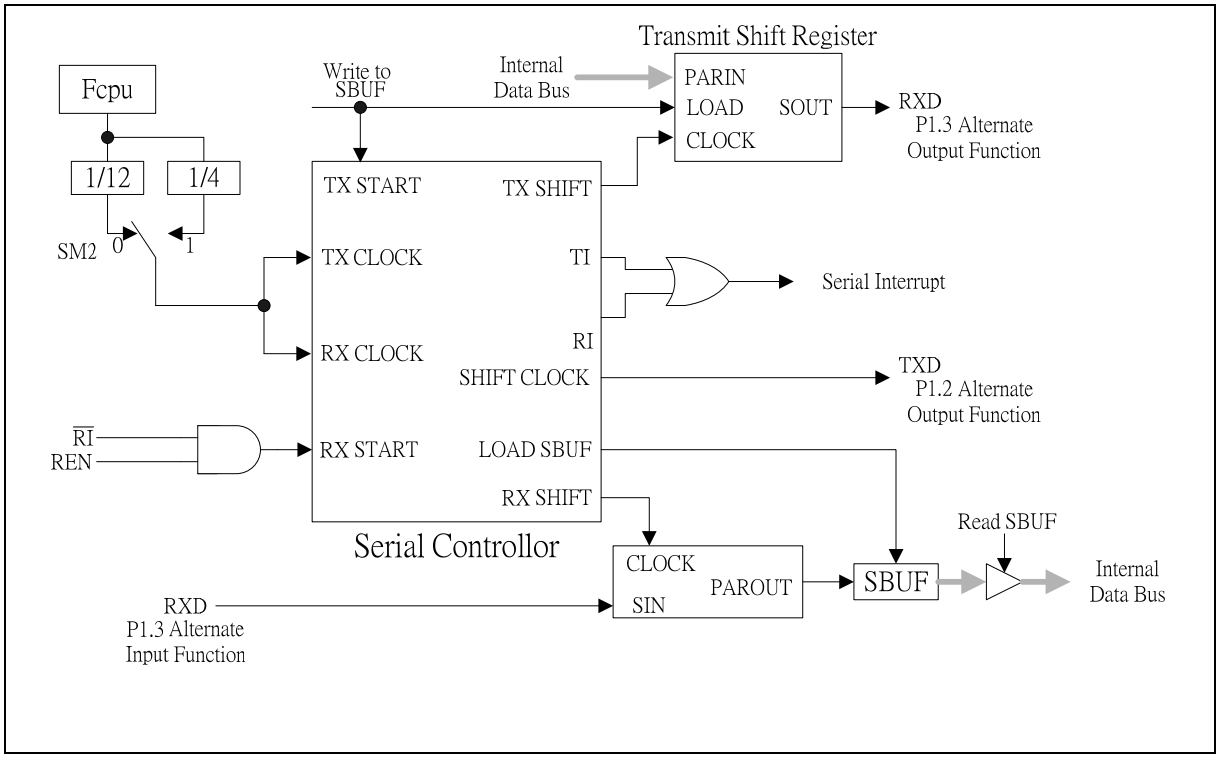


Figure 21-1: Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

21.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a

best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

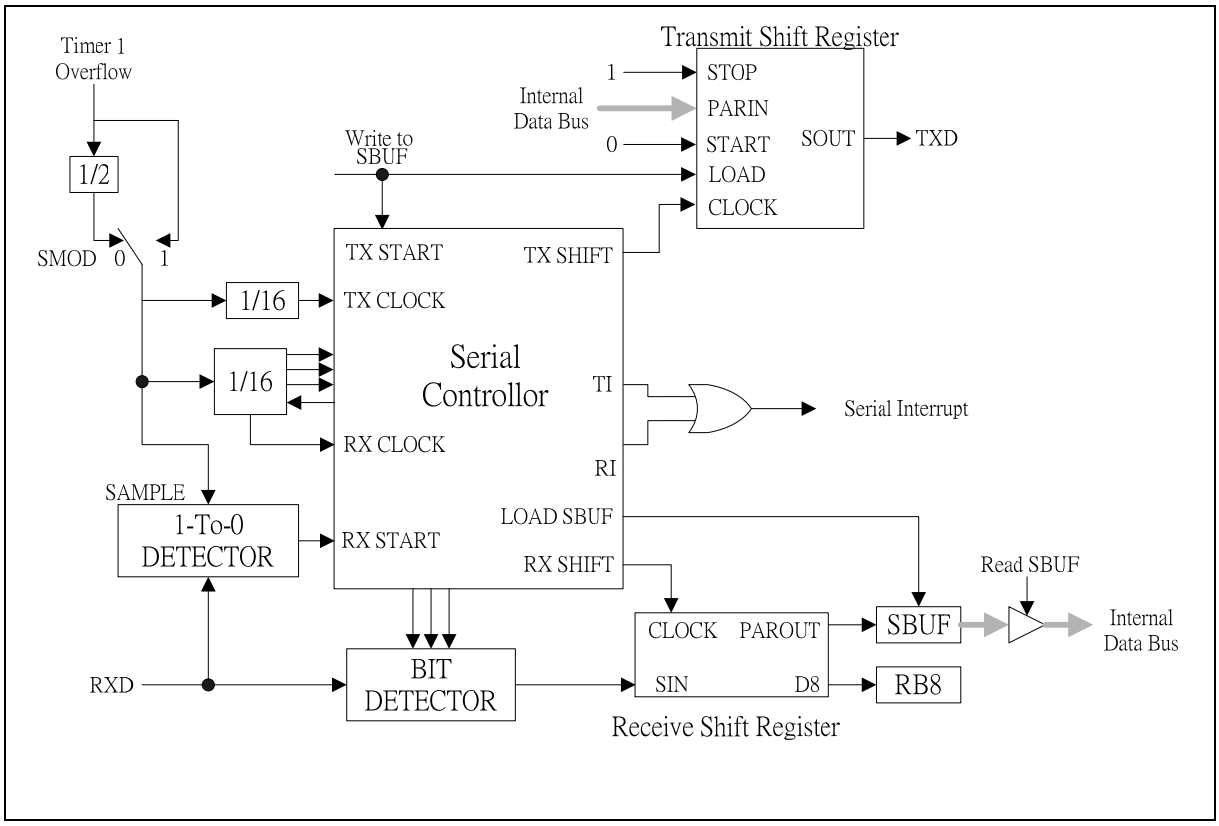


Figure 21-2: Serial Port Mode 1

21.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

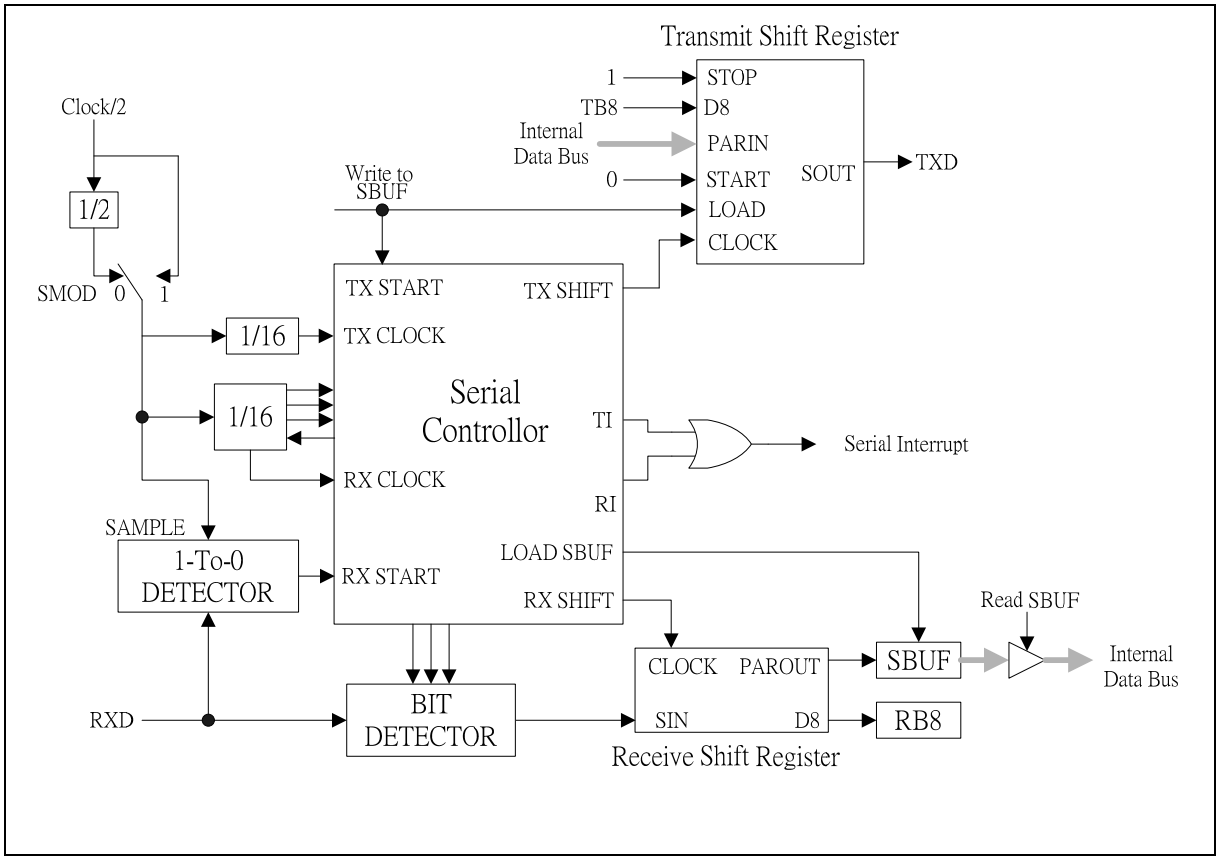


Figure 21-3: Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After

shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

21.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

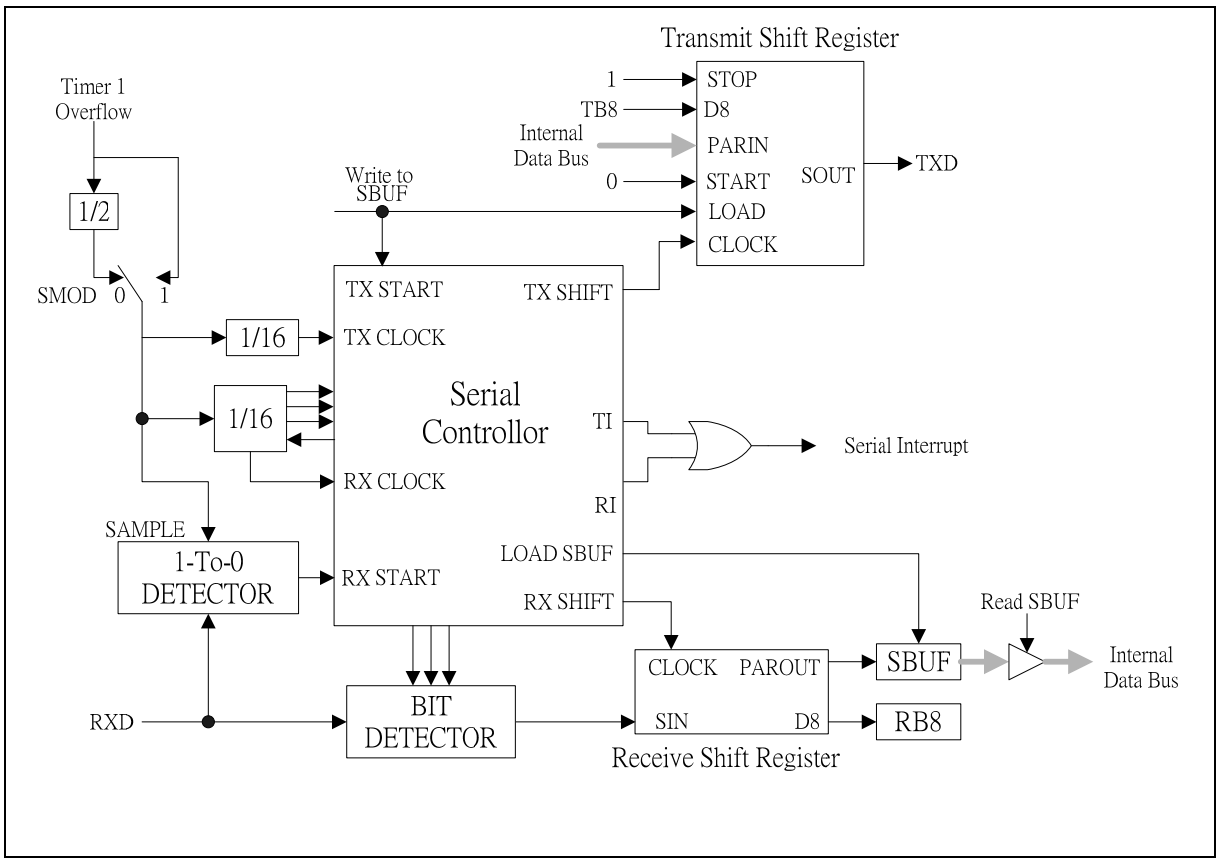


Figure 21-4: Serial Port Mode 3

SM0	SM1	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION

0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1	11 bits	1	1	0, 1

Figure 21-5: Serial Ports Modes

21.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. N79E235 series have the capability to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

21.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. The RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100

SADEN 1111 1010

Given: 1010 0x0x

Slave 2:

SADDR 1010 0111

SADEN 1111 1001

Given : 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXXb (i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

22 I2C SERIAL CONTROL

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I2C interrupt if the I2C bus hangs up and timer-out counter overflows.
- The I2C port pins, SDA and SCL are permanently in Open-drain type. External pull-up are needed for high output

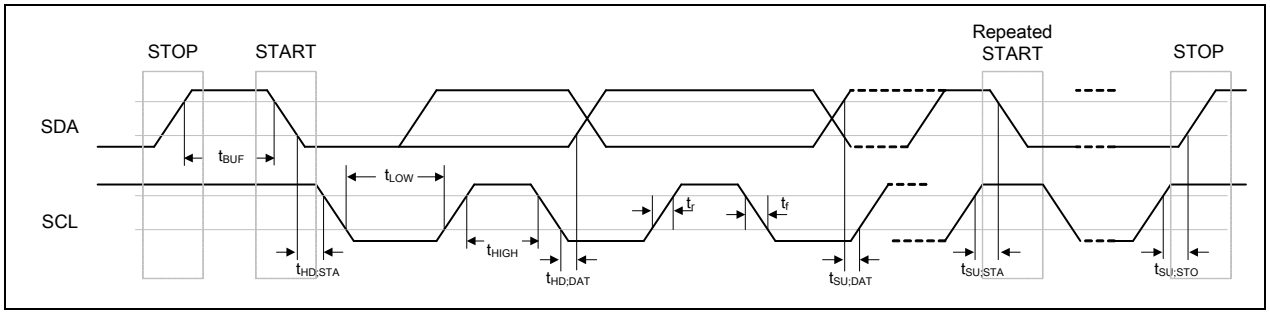


Figure 22-1: I2C Bus Timing

22.1 I2C Port

The device's on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. To enable this port, the bit ENSI in I2CON should be set to '1'. The I2C H/W interfaces to the I2C bus via two pins: SDA (P1.6, serial data line) and SCL (P1.5, serial clock line). Pull up resistors are needed on Pin P1.5 and P1.6 for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins to logic high in advance.

22.2 SFR for I2C Function

The CPU interfaces to the SIO port through the following six special function registers: **I2CON** (control register, C0H), **I2STATUS** (status register, BDH), **I2DAT** (data register, BCH), **I2ADDR** (address registers, C1H), **I2CLK** (clock rate register BEH) and **I2TOC** (Time-out counter register, BFH).

When I2C port is enabled by setting ENSI to high, the internal states will be controlled by I2CON and I2C logic hardware. Once a new status code is generated and stored in I2STATUS, the I2C interrupt flag (SI) will be set automatically. If both EA and EI2C are also in logic high, the I2C interrupt is requested. The 5 most significant bits of I2STATUS stores the internal state code, the lowest 3 bits are always zero and the content keeps stable until SI is cleared by software.

22.2.1 I2C Address Registers, I2ADDR

I2C port is equipped with one slave address register. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR are matched with the received slave address.

The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

When GC bit is set, the I2C is in Slave mode, it can be received the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode. If it is in Master mode, the AA bit must be cleared when it will send general call address of 00H to I2C bus.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxx0B

22.2.2 I2C Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. This occurs when SIO is in a defined state and the serial interrupt flag (SI) is set. Data in I2DAT remains stable as long as SI bit is set. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus. Thus, in the event of arbitration lost, the transition from master transmitter to slave receiver is made with the correct data in I2DAT.

I2DAT and the acknowledge bit form a 9-bit shift register, the acknowledge bit is controlled by the SIO hardware and cannot be accessed by the CPU. Serial data is shifted through the acknowledge bit into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses, and is shifted into I2DAT on the rising edges of SCL clock pulses.

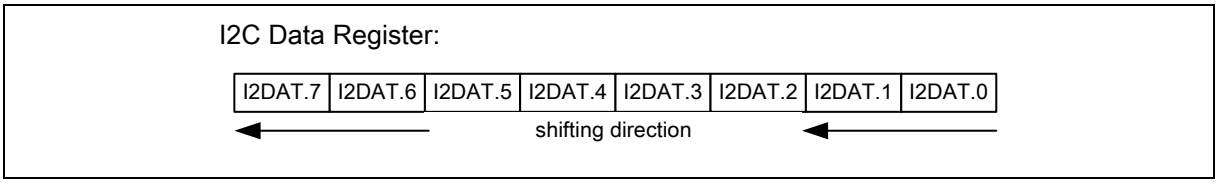


Figure 22-2 I2C Data Shifting Direction

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2DAT	I2C DATA REGISTER	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxB

22.2.3 I2C Control Register, I2CON

The CPU can read from and write to this 8-bit, directly addressable SFR. Two bits are affected by hardware: the SI bit is set when the I2C hardware requests a serial interrupt, and the STO bit is cleared when a STOP condition is present on the bus. The STO bit is also cleared when ENSI = "0".

ENSI Set to enable I2C serial function block. When ENS=1 the I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode. This means it is NO LONGER in the slave receiver mode to receive data from the master transmit device.

SI I2C Interrupt Flag. When a new SIO state is present in the I2STATUS register, the SI flag is set by hardware, and if the EA and EI2C bits are both set, the I2C interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge control bit. When AA=1 prior to address or data received, an acknowledged (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when 1.) A slave is acknowledging the address sent from master, 2.) The receiver devices are acknowledging the data sent by transmitter. When AA=0 prior to address or data received, a Not acknowledged (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2CON	I2C CONTROL REGISTER	C0H	(CF) -	(CE) ENSI	(CD) STA	(CC) STO	(CB) SI	(CA) AA	(C9) -	(C8) -	x000 00xxB

22.2.4 I2C Status Register, I2STATUS

I2STATUS is an 8-bit read-only register. The three least significant bits are always 0. The five most significant bits contain the status code. There are 26 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined SIO states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

In addition, state 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data byte or an acknowledge bit. To recover I2C from bus error, STO should be set and SI should be clear to enter not addressed slave mode. Then clear STO to release bus and to wait new communication. I2C bus can not recognize stop condition during this action when bus error occurs.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2STATUS	I2C STATUS REGISTER	BDH	B7	B6	B5	B4	B3	B2	B1	B0	1111 1000B

22.2.5 I2C Clock Baud Rate Bits, I2CLK

The data baud rate of I2C is determines by I2CLK register when SIO is in a master mode. It is not important when SIO is in a slave mode. In the slave modes, SIO will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting is Data Baud Rate of I2C = Fcpu /(4x(I2CLK+1)). If Fcpu=16MHz, the I2CLK = 40(28H), so data baud rate of I2C = 16MHz/(4X (40 +1)) = 97.5Kbits/sec. The block diagram is as below figure.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B

22.2.6 I2C Time-out Counter Register, I2TOC

There is a 14-bit time-out counter which can be sued to deal with the I2C bus hang-up. If the time-out counter is enabled, the counter starts up counting until it overflows(TIF=1) and requests I2C interrupt from CPU or stops counting by clearing ENTI to 0. When time-out counter is enabled, setting flag SI to high will reset counter and re-start up counting after SI is cleared. If I2C bus hangs up, it causes the I2STATUS and flag SI are not updated for a period, the 14-bit time-out counter may overflow and acknowledge CPU the I2C interrupt. Refer to Figure 22-3 for the 14-bit time-out counter.

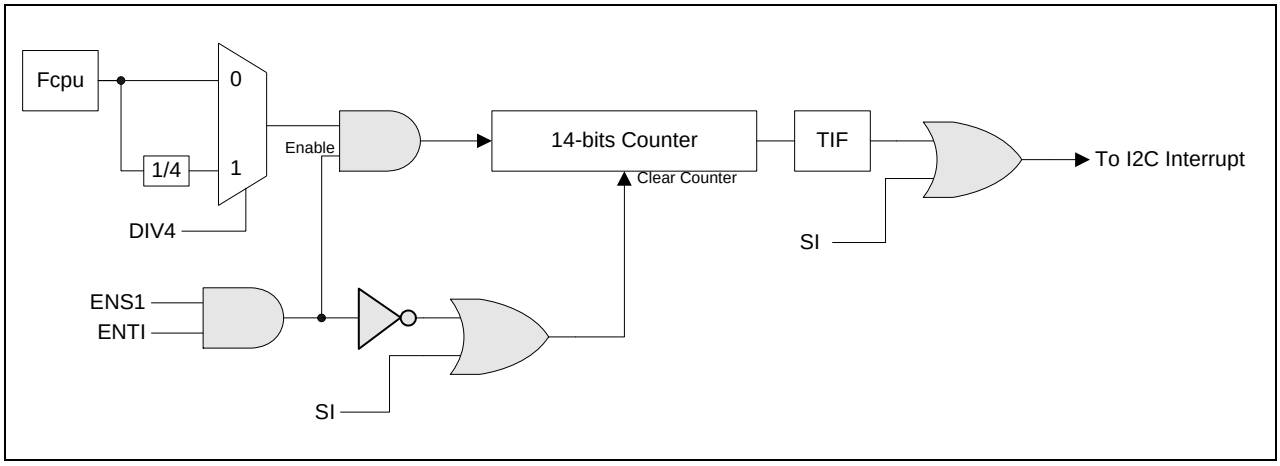


Figure 22-3: I2C Time-out Count Block Diagram

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
I2TOC	I2C TIME-OUT COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF	0000 0000B

22.3 Modes of Operation

The on-chip I2C ports support five operation modes, Master transmitter, Master receiver, Slave transmitter, Slave receiver, and GC call.

In a given application, I2C port may operate as a master or as a slave. In the slave mode, the I2C port hardware looks for its own slave address and the general call address. If one of these addresses is detected, and if the slave is willing to receive or transmit data from/to master(by setting the AA bit), acknowledge pulse will be transmitted out on the 9th clock, hence an interrupt is requested on both master and slave devices if interrupt is enabled. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible

slave action is not interrupted. If bus arbitration is lost in the master mode, I2C port switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

22.3.1 Master Transmitter Mode

Serial data output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and it is represented by "W" in the flow diagrams. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

22.3.2 Master Receiver Mode

In this case the data direction bit (R/W) will be logic 1, and it is represented by "R" in the flow diagrams. Thus the first byte transmitted is SLA+R. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

22.3.3 Slave Receiver Mode

Serial data and the serial clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

22.3.4 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

22.4 Data Transfer Flow in Five Operating Modes

The five operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter, Slave/Receiver and GC Call. Bits STA, STO and AA in I2CON register will determine the next state of the SIO hardware after SI flag is cleared. Upon complexion of the new action, a new status code will be updated and the SI flag will be set. If the I2C interrupt control bits (EA and EI2C) are enable, appropriate action or software branch of the new status code can be performed in the Interrupt service routine.

Data transfers in each mode are shown in the following figures.

*** Legend for the following five figures:

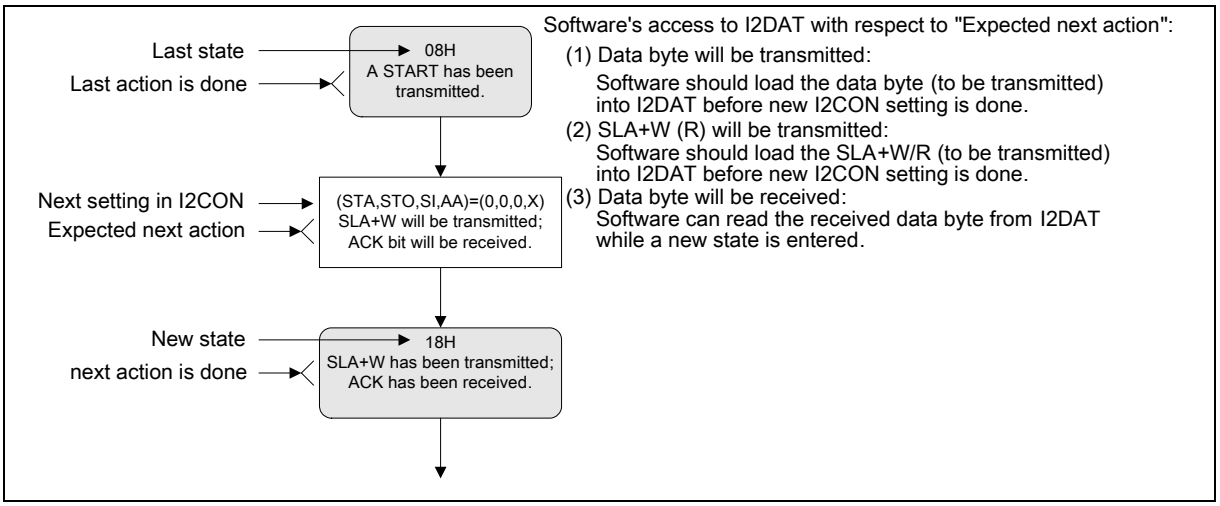


Figure 22-4 Legend for the following four figures

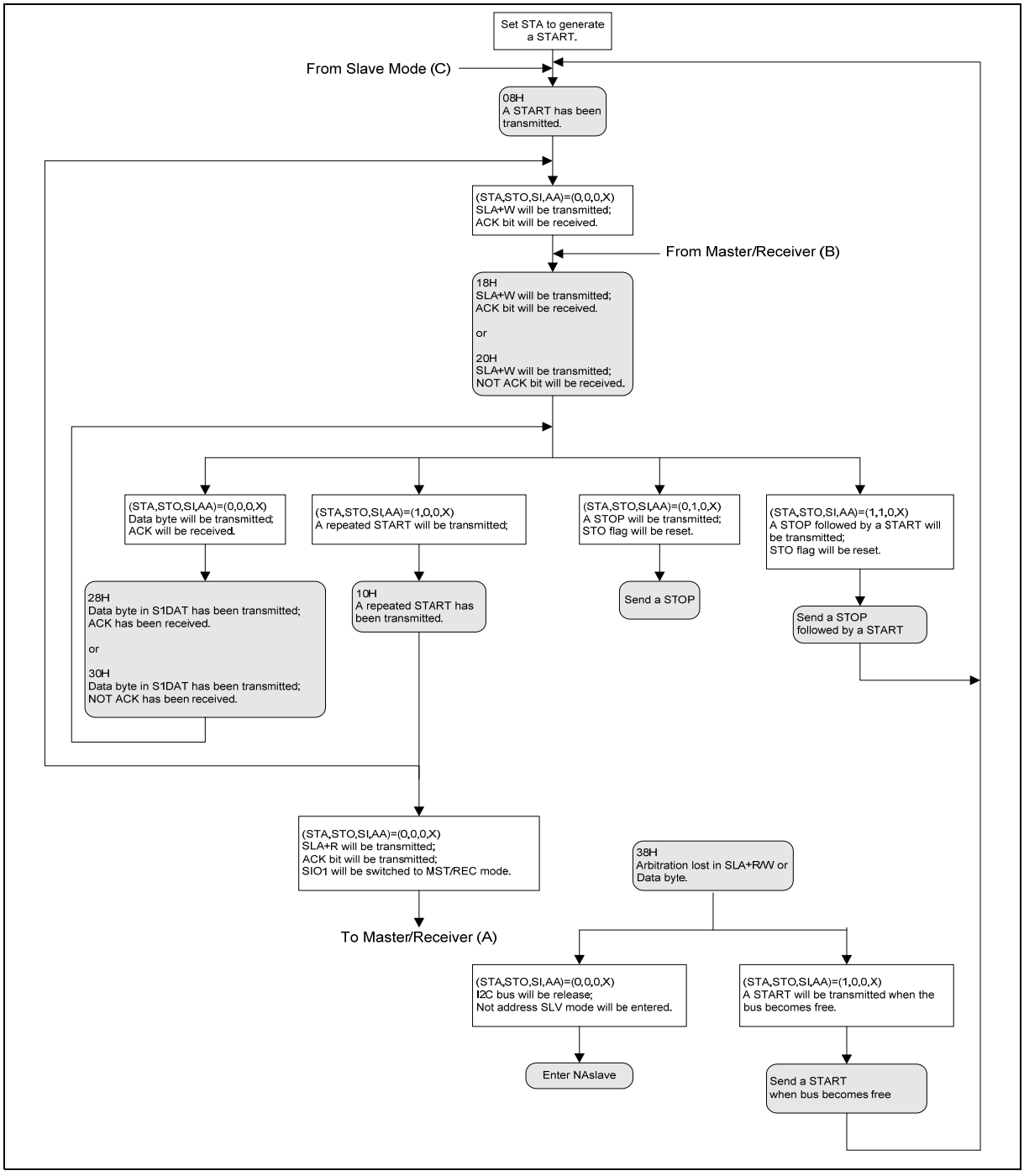


Figure 22-5 Master Transmitter Mode

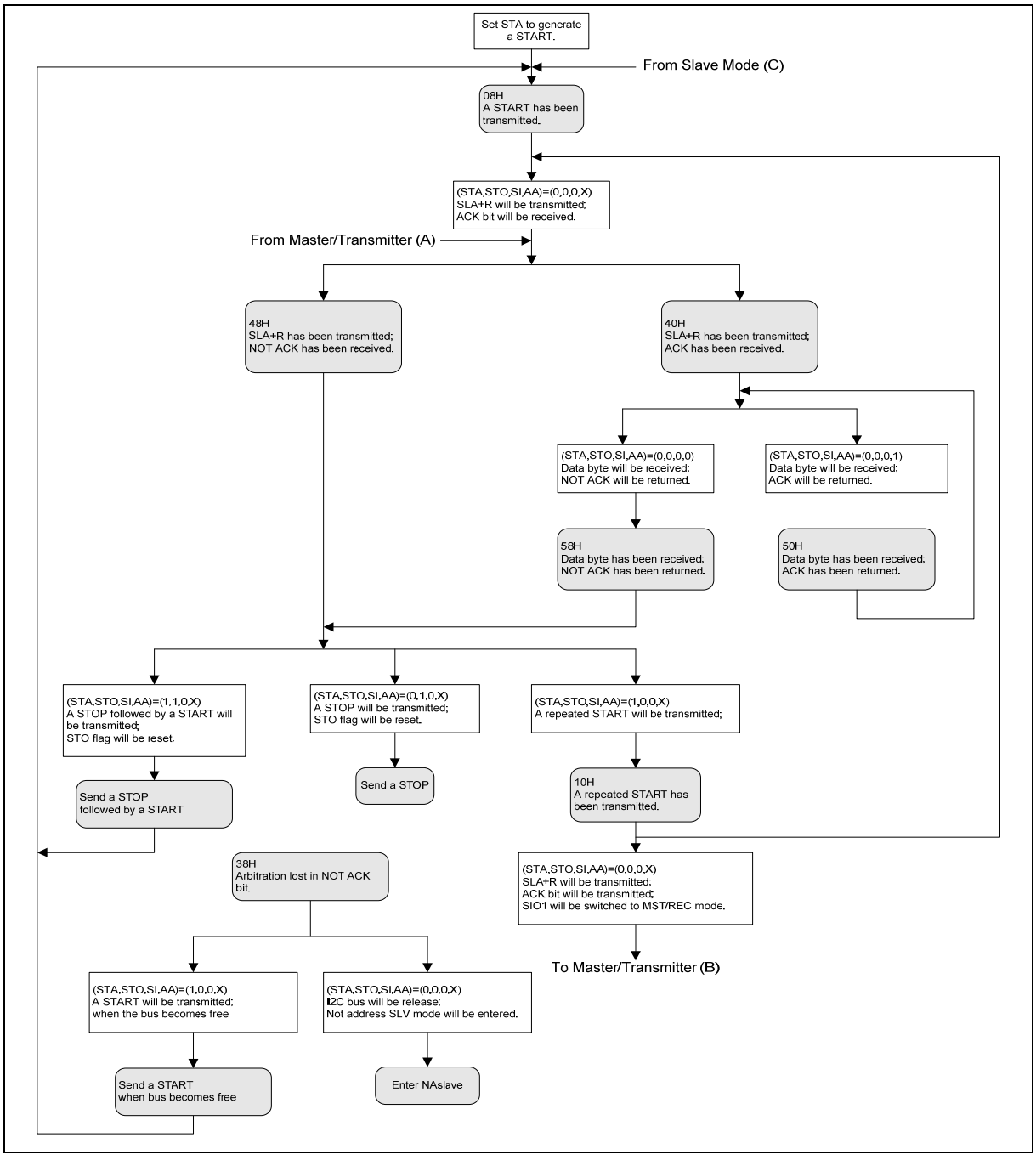


Figure 22-6 Master Receiver Mode

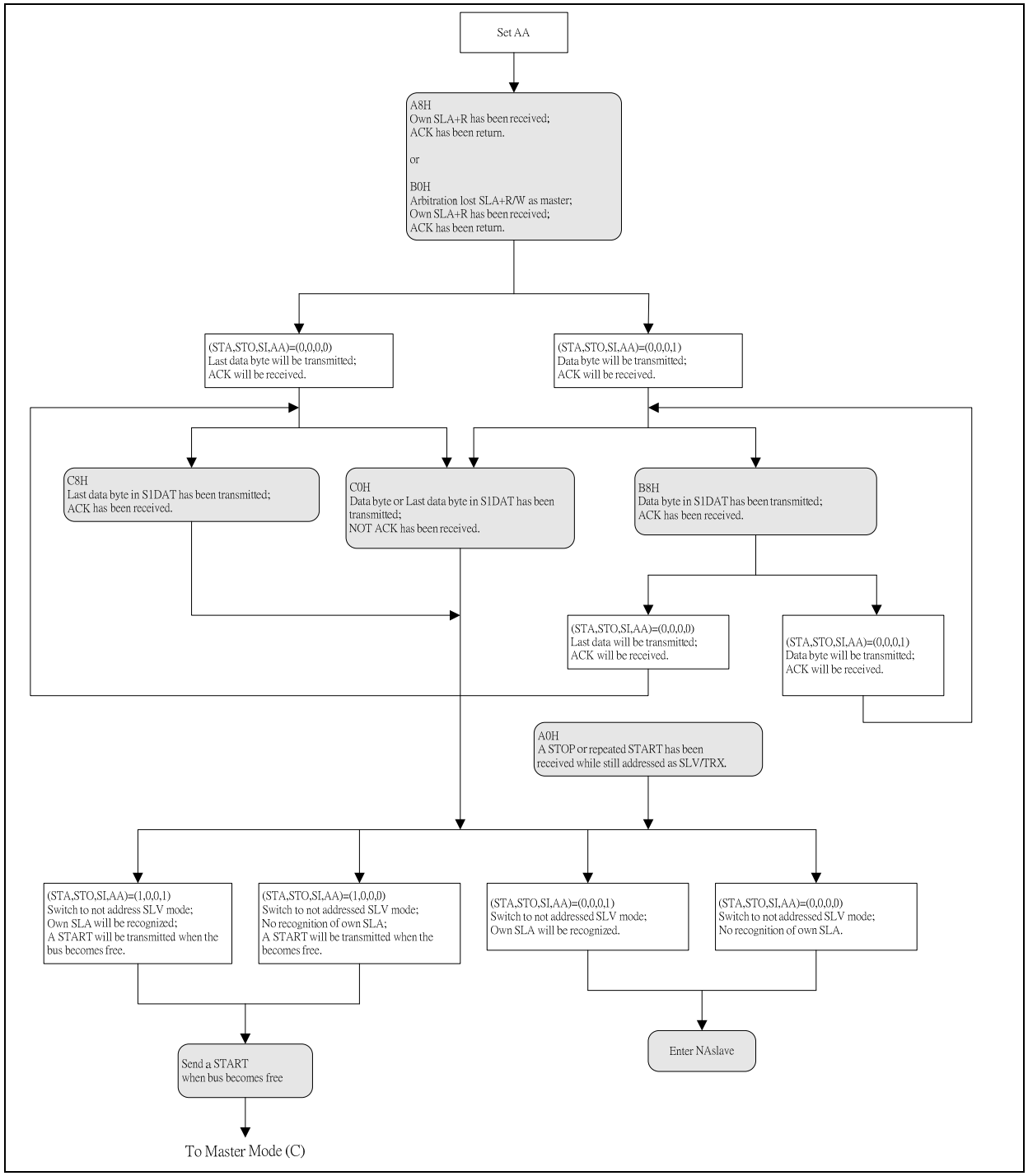


Figure 22-7 Slave Transmitter Mode

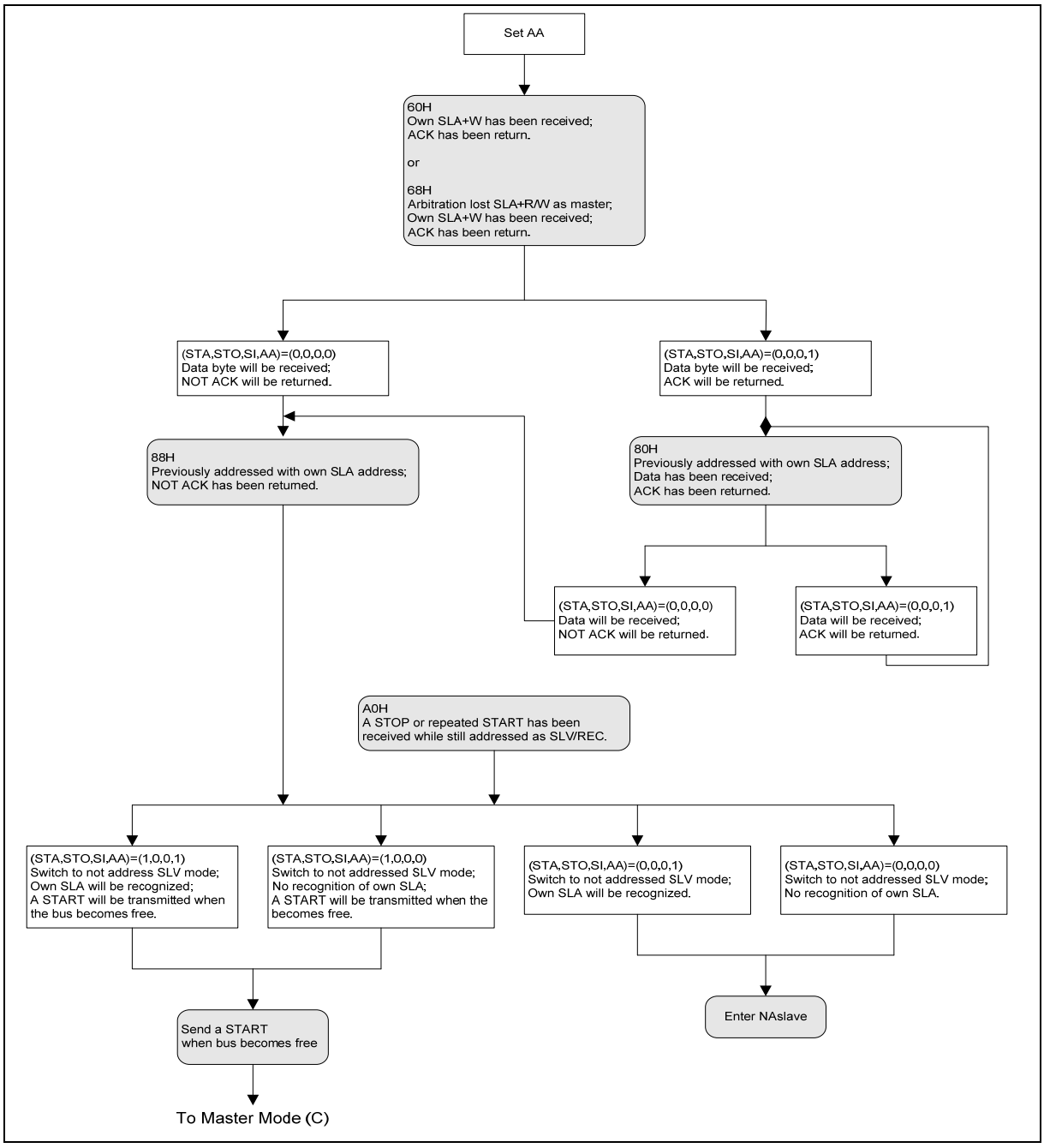


Figure 22-8 Slave Receiver Mode

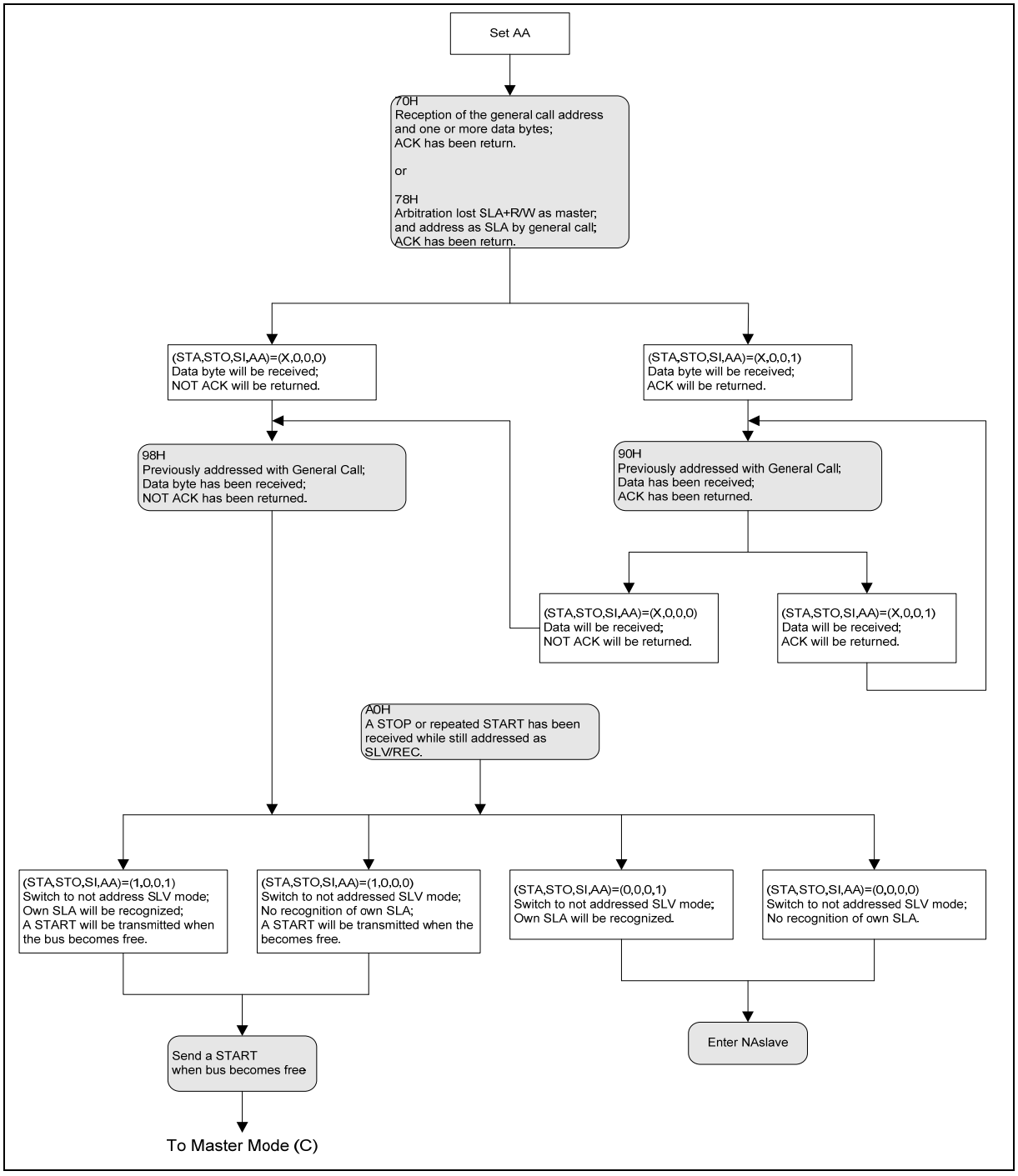


Figure 22-9 GC Mode

23 SERIAL PHERIPHERAL INTERFACE (SPI)

23.1 General descriptions

N79E235 series consist of SPI block to support high speed serial communication. It's capable of supporting data transfer rates of 2.5 Mbit/s, for 40MHz bus frequency. This device's SPI support the following features;

- Master and slave mode.
- Slave select output.
- Programmable serial clock's polarity and phase.
- Receive double buffered data register.
- MSB first(default) or LSB first selectable.
- Write collision detection.
- Transfer complete interrupt.

23.2 Block descriptions

The following figure shows SPI block diagram. It provides an overview of SPI architecture in this device. The main blocks of SPI are SPI register blocks, control logics, baud rate control, and pin control logics;

Shift register and read data buffer. It is single buffered in the transmit direction and double buffered in the receive direction. Transmit data cannot be written to the shifter until the previous transfer is complete. When the SPIF set, user will not be able to write to the shift register. User has to clear the SPIF before writing to the shift register. Receive logics consist of parallel read data buffer so the shifter is free to accept a second data, as the first received data will be transferred to the read data buffer.

SPI Control block. This provide control functions to configure the device for SPI enable, master or slave, clock phase and polarity, MSB/LSB access first selection, and Slave Select output enable.

Baud rate control. This control logics divide CPU clock to 4 different selectable clocks (1/16, 1/32, 1/64 and 1/128).

SPR1	SPR0	Divider	Baud Rate
0	0	16	2.5 Mbit/s
0	1	32	1.25 Mbit/s
1	0	64	625 Kbit/s
1	1	128	312.5 Kbit/s

Table 23-1 SPI Baud Rate Selection (based on 40 MHz Bus Clock)

SPI registers. There are three SPI registers to support its operations, they are;

- SPI control registers (SPCR)
- SPI status registers (SPSR)
- SPI data register (SPDR)

These registers provide control, status, data storage functions and baud rate selection control. Detail bit descriptions are found at SFR section.

Pin control logic. Controls behavior of SPI interface pins.

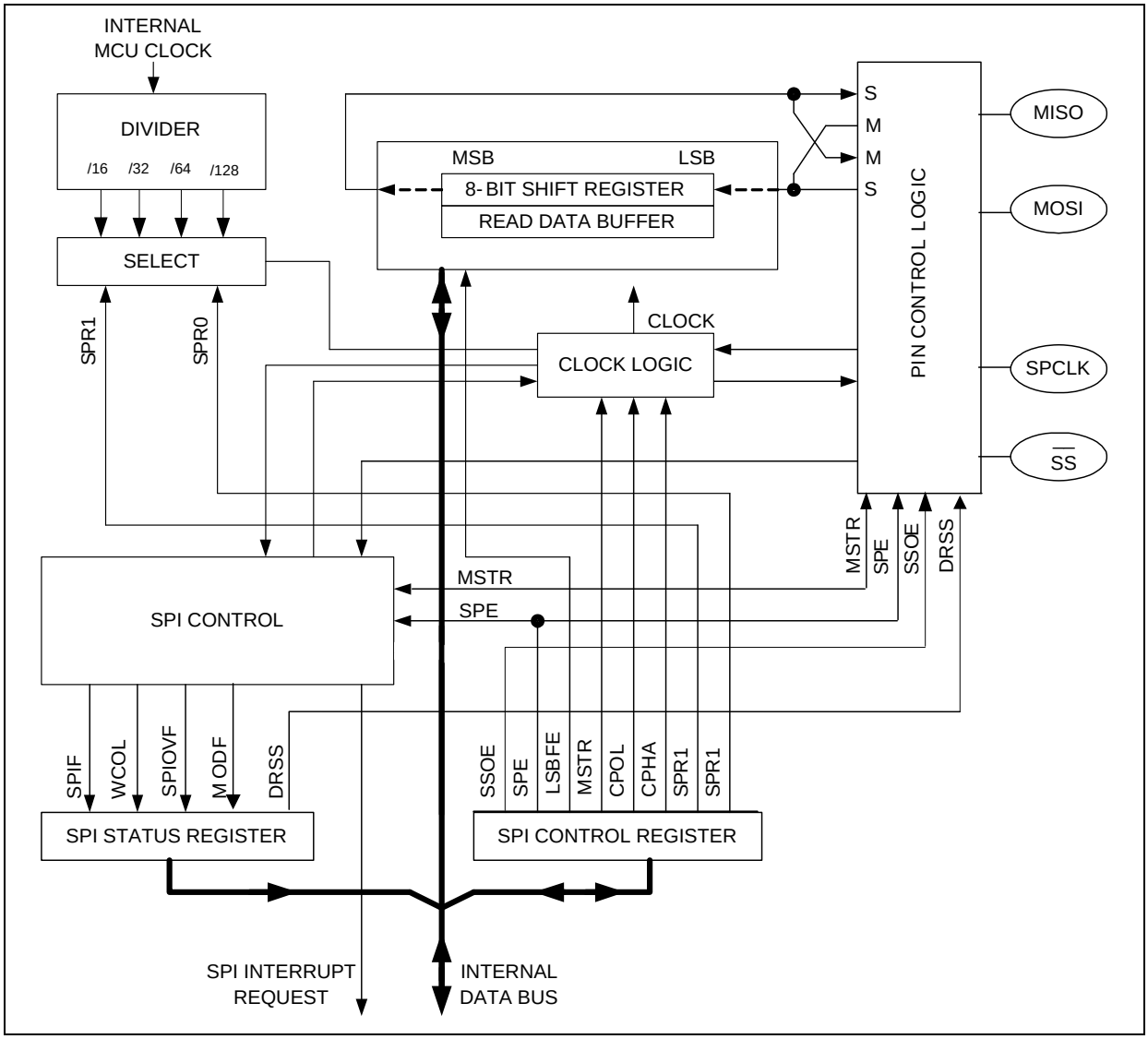


Figure 23-1 SPI block diagram

23.3 Functional descriptions

23.3.1 Master mode

The device can configure the SPI to operate as a master or as a slave, through MSTR bit. When the MSTR bit is set, master mode is selected, when MSTR bit is cleared, slave mode is selected. During master mode, only master SPI device can initiate transmission. A transmission begins by writing to the master SPDR register. The bytes begin shifting out on MOSI pin under the control of SPCLK. The master places data on MOSI line a half-cycle before SPCLK edge that the slave device uses to latch the data bit. The /SS must stay low before data transactions and stay low for the duration of the transactions.

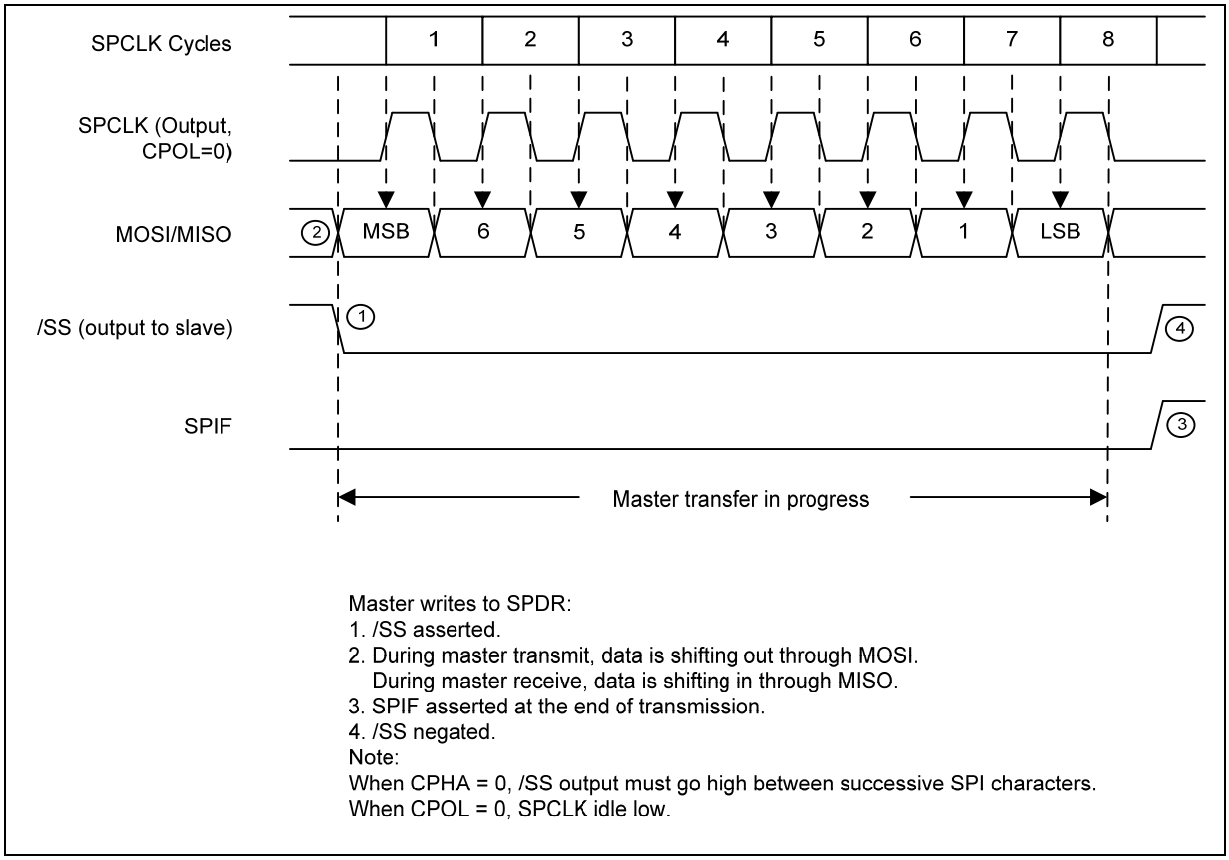


Figure 23-2 Master Mode Transmission (CPOL = 0, CPHA = 0)

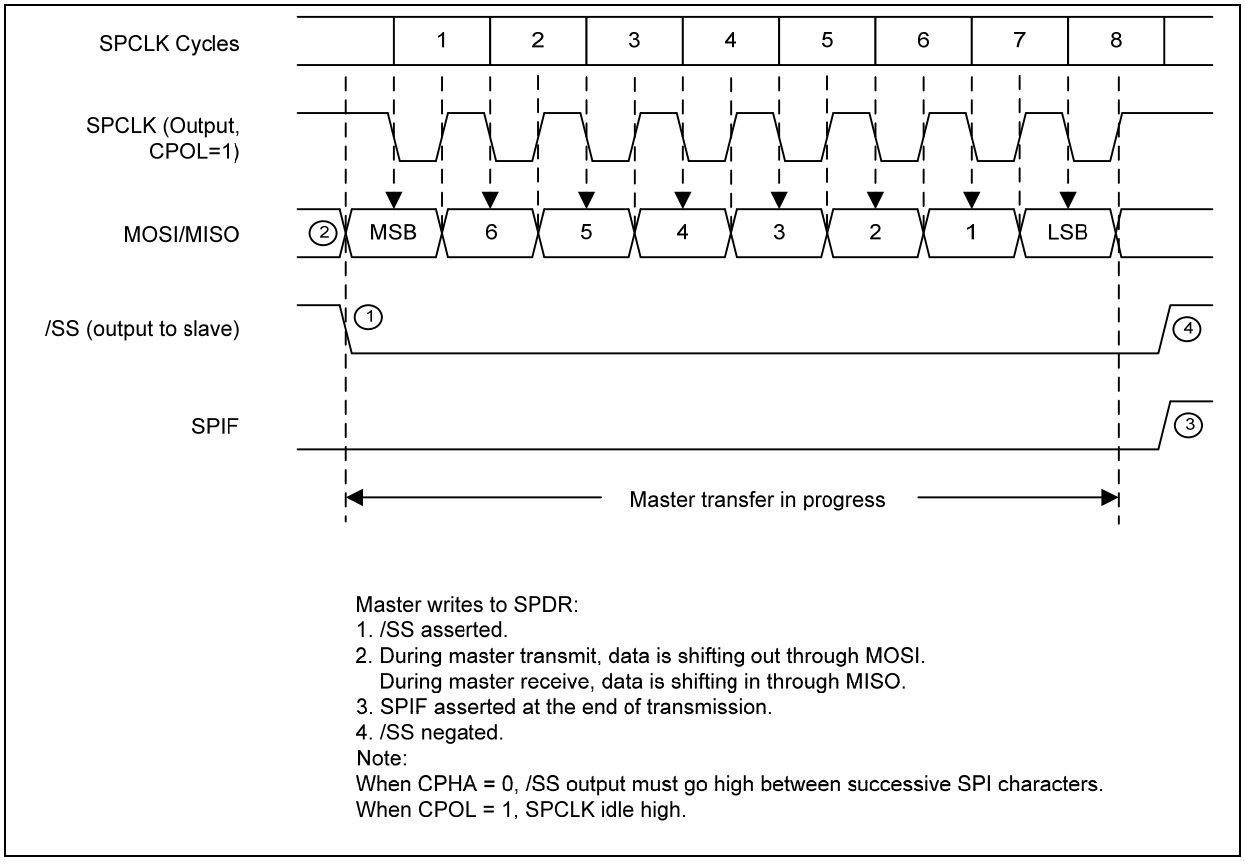


Figure 23-3 Master Mode Transmission (CPOL = 1, CPHA = 0)

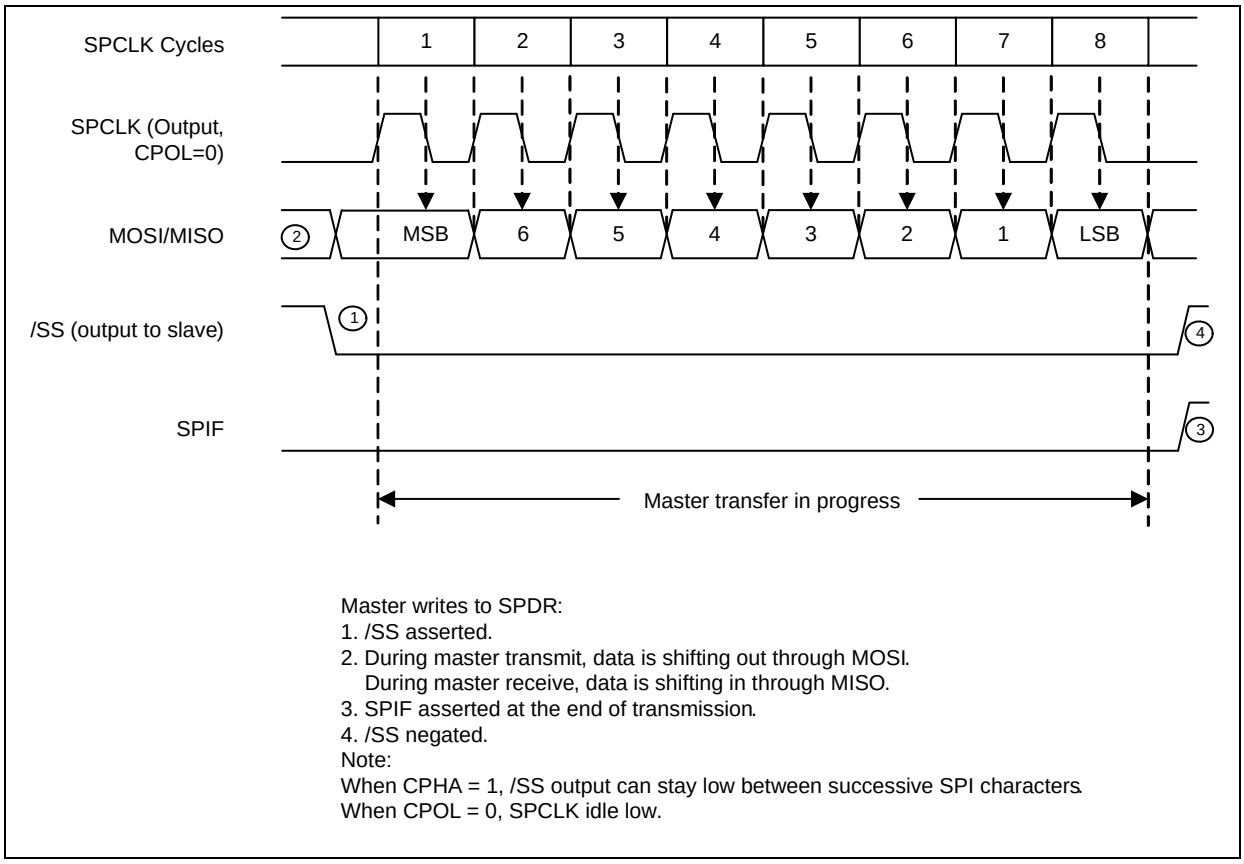


Figure 23-4 Master Mode Transmission (CPOL = 0, CPHA = 1)

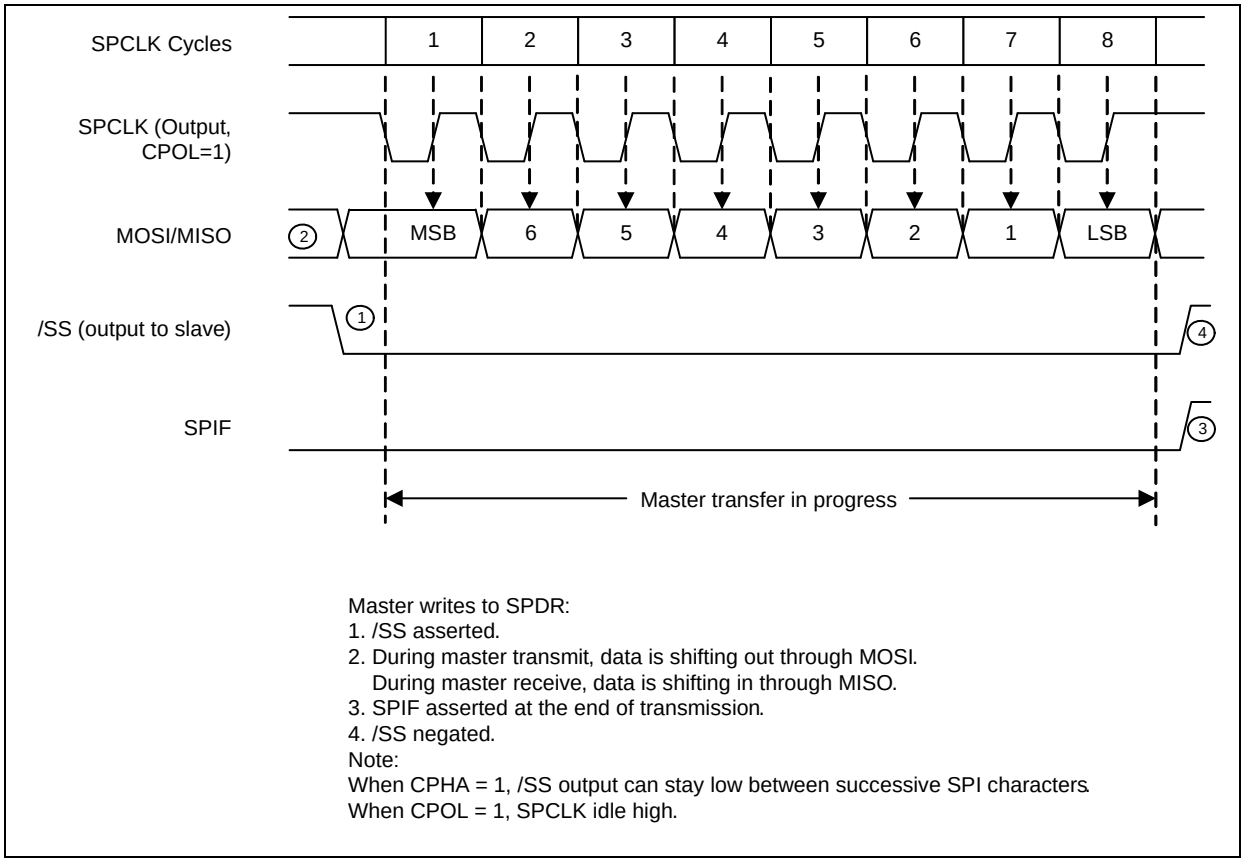


Figure 23-5 Master Mode Transmission (CPOL = 1, CPHA = 1)

23.3.2 Slave Mode

When in slave mode, the SPCLK pin becomes input and it will be clock by another master SPI device. The /SS pin also becomes input. Similarly, before data transmissions occurs, and remain low until the transmission completed. If /SS goes high, the SPI is forced into idle state.

Data flows from master to slave on MOSI pin and flows from slave to master on MISO pin. The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices. A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

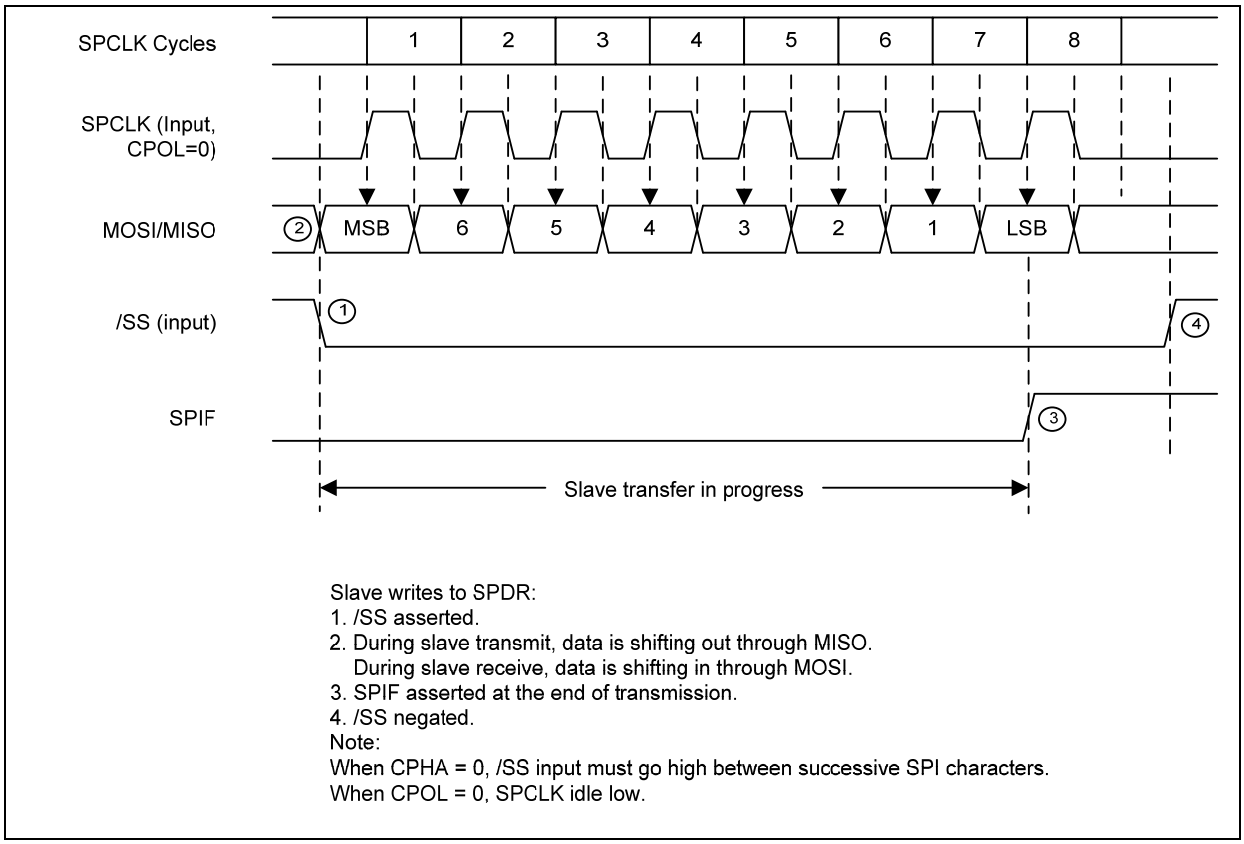


Figure 23-6 Slave Mode Transmission (CPOL = 0, CPHA = 0)

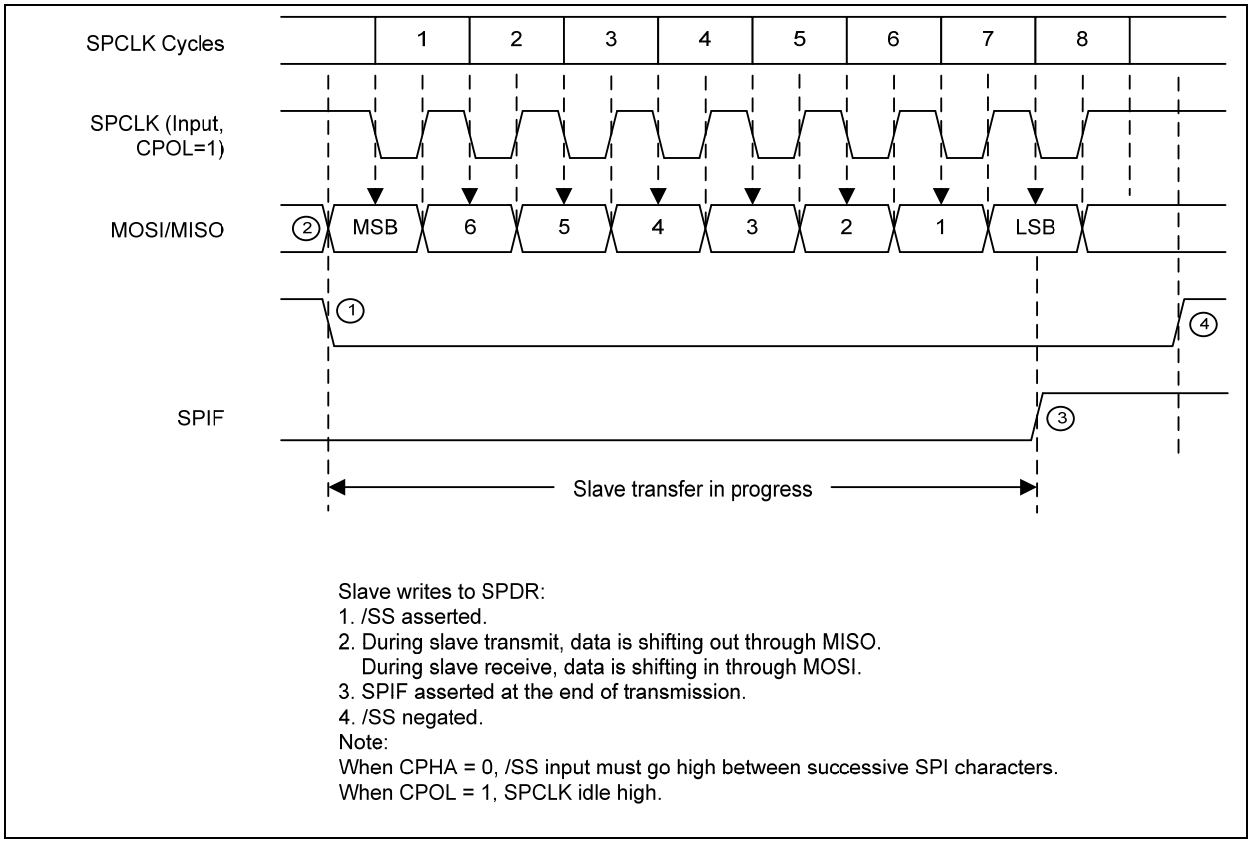


Figure 23-7 Slave Mode Transmission (CPOL = 1, CPHA = 0)

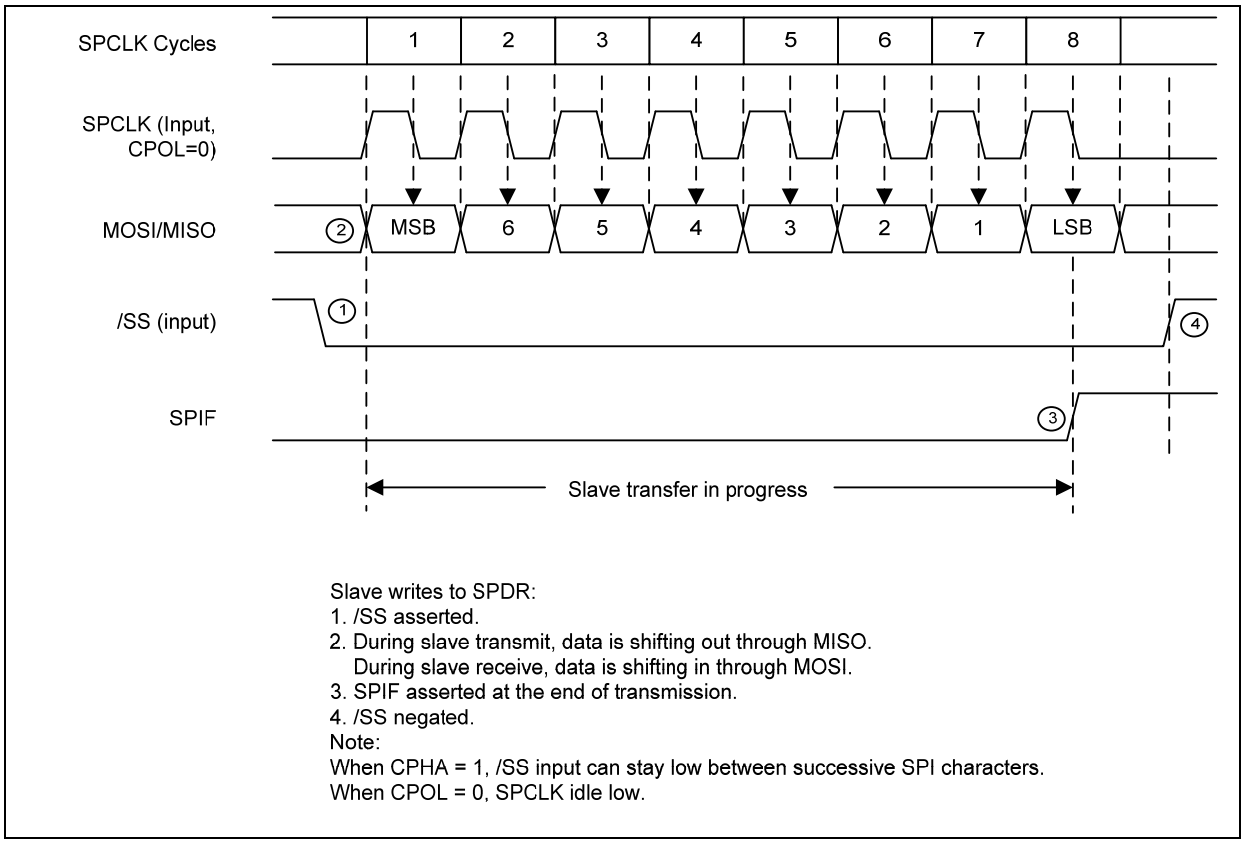


Figure 23-8 Slave Mode Transmission (CPOL = 0, CPHA = 1)

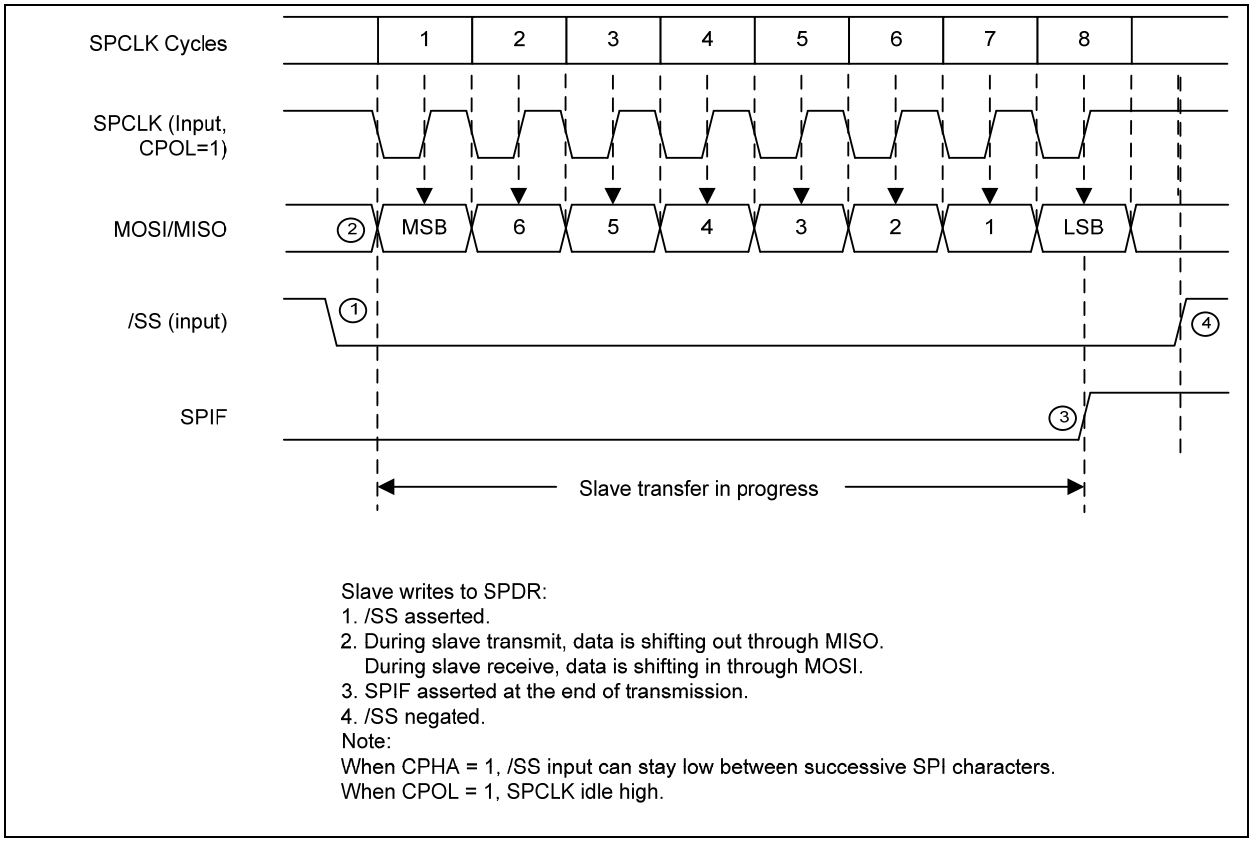


Figure 23-9 Slave Mode Transmission (CPOL = 1, CPHA = 1)

23.3.3 Slave select

The slave select (/SS) input of a slave device must be externally asserted before a master device can exchange data with the slave device. /SS must be low before data transactions and must stay low for the duration of the transaction. The /SS line of the master must be held high.

The other three lines are dedicated to the SPI whenever the serial peripheral interface is on.

The state of the master and slave CPHA bits affects the operation of /SS. CPHA settings should be identical for master and slave. When CPHA = 0, the shift clock is the OR of /SS with SCK. In this clock phase mode, /SS must go high between successive characters in an SPI message. When CPHA = 1, /SS can be left low between successive SPI characters. In cases where there is only one SPI slave MCU, its /SS line can be tied to VSS as long as only CPHA = 1 clock mode is used.

23.3.4 Slave Select output enable

Available in master mode only, the /SS output is enabled with the SSOE bit in the SPCR register. The /SS output pin is connected to the /SS input pin of the slave device. The /SS output automatically goes low for each transmission when selecting external device and it goes high during each idling state to deselect external devices.

DRSS	SSOE	Master Mode	Slave Mode
0	0	/SS input (With Mode Fault). See section SPI I/O mode section for detail.	/SS Input (Not affected by SSOE)

0	1	Reserved	/SS Input (Not affected by SSOE)
1	0	/SS General purpose I/O (No Mode Fault)	/SS Input (Not affected by SSOE)
1	1	/SS output (No Mode Fault)	/SS Input (Not affected by SSOE)

Table 23-2 /SS output

During master mode (with SSOE=DRSS= 0), mode fault will be set if /SS pin is detected low. When mode fault is detected hardware will clear MSTR bit and SPE bit in the meantime it will also generated interrupt request, if ESPI is enabled.

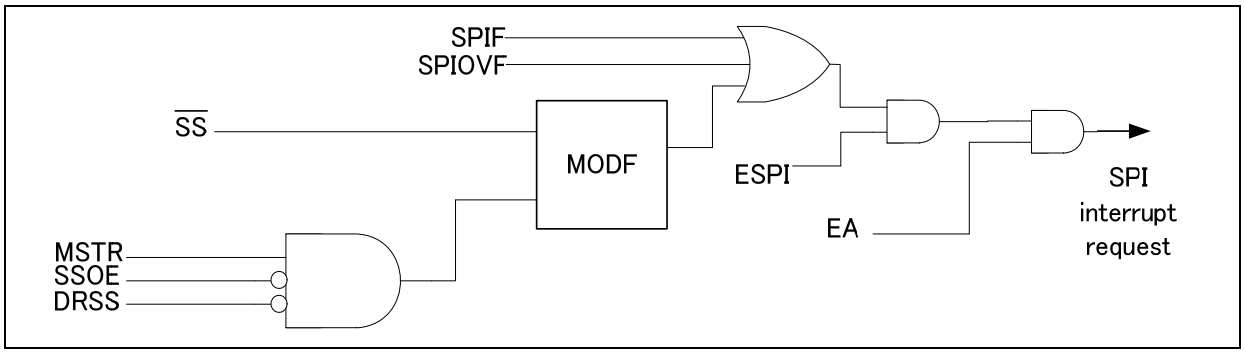


Figure 23-10 SPI interrupt request

23.3.5 SPI I/O pins mode

When SPI is disabled (SPE = 0) the corresponding I/O is following the setting determined by port mode setting (SFR P2M1 & P2M2). When SPI is enabled (SPE = 1) the SPI pins I/O mode follow the below table. For /SS pin it is always at Quasi-bidirectional mode whether it is configured as master or slave.

	MISO	**MOSI**	**CLK**	**/SS**
Master	Input	Output	Output	**Output**[1]**:** DRSS=1,SSOE=1 **Input**: DRSS=0, SSOE=0
Slave	**Output**[2] during /SS = Low Else Input mode	Input	Input	Input

Table 23-3 SPI I/O pins mode

Input = Quasi-bidirectional mode; Output = Push-pull mode

Output[1] = This output mode in /SS is Quasi-bidirectional output mode. Master needs to detect mode fault during master outputs /SS low.

Output[2] = In SLAVE mode, MISO is in output mode only during the time of /SS =Low. Otherwise it must keep in input mode (Quasi-bidirectional).

23.3.6 Programmable serial clock's phase and polarity

The clock polarity SPCR.CPOL control bit selects active high or active low SCK clock, and has no significant effect on the transfer format. The clock phase SPCR.CPHA control bit selects one of two different transfer protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges. Thus, both these bits enable selection of four possible clock formats to be used by SPI system.

The clock phase and polarity should be identical for the master SPI device and the communicating slave device.

When CPHA equals 0, the /SS line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while /SS is low, a write collision error results. When CPHA equals 1, the /SS line can remain low between successive transfers.

When CPHA = 0, data is sample on the first edge of SPCLK and when CPHA = 1 data is sample on the second edge of the SPCLK. Prior to changing CPOL setting, SPE must be disabled first.

23.3.7 Receive double buffered data register

This device is single buffered in the transmit direction and double buffered in the receive direction. This means that new data for transmission cannot be written to the shifter until the previous transfer is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial byte. As long as the first byte is read out of the read data buffer before the next byte is ready to be transferred, no overrun condition occurs.

If overrun occur, SPIOVF is set. Second byte serial data cannot be transferred successfully into the data register during overrun condition and the data register will remains the value of the previous byte. The figure below shows the receive data timing waveform when overrun occur.

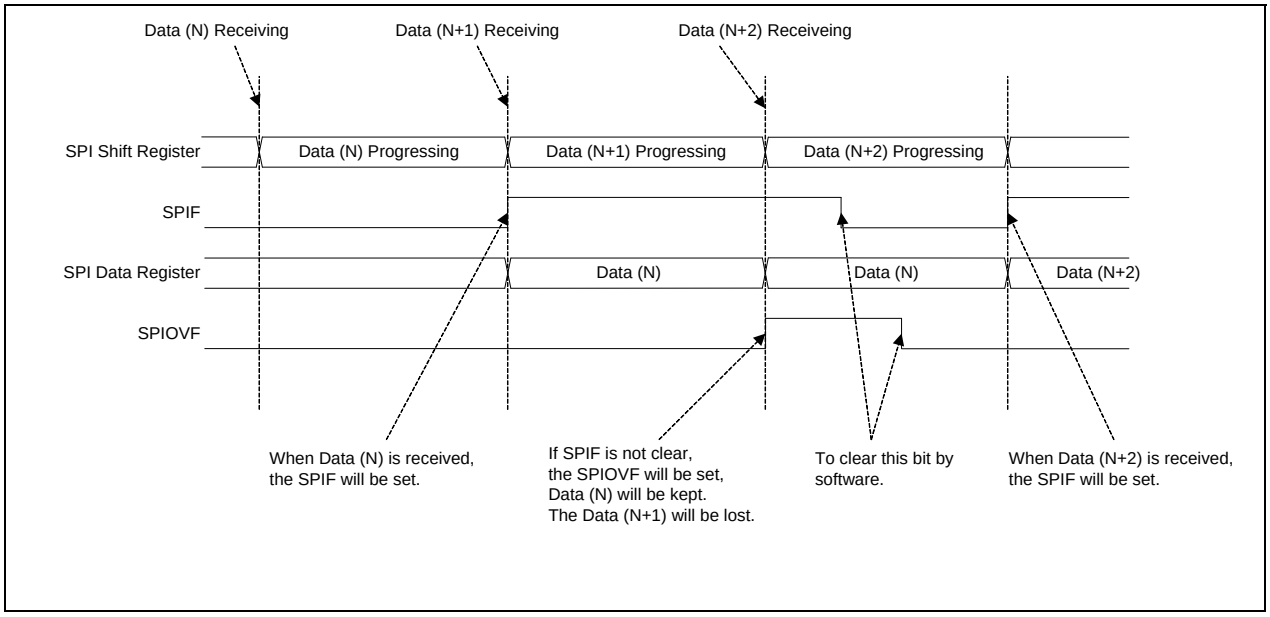


Figure 23-11 SPI receive data timing waveform

23.3.8 LSB first enable

By default, this device transfer the SPI data most significant bit first. This device provides a control bit SPCR.LSBFE to allow support of transfer of SPI data in least significant bit first.

23.3.9 Write Collision detection

Write collision indicates that an attempt was made to write data to the SPDR while a transfer was in progress. SPDR is not double buffered in the transmit direction, any writes to SPDR cause data to be written directly into the SPI shift register. This write corrupts any transfer in progress, a write collision error is generated (WCOL will be set). The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

WCOL flag is clear by software.

23.3.10 Transfer complete interrupt

This device consists of an interrupt flag at SPSR.SPIF. This flag will be set upon completion of data transfer with external device, or when a new data have been received and copied to SPDR. If interrupt is enable (through ESPI located at EIE2.3), the SPI interrupt request will be generated, if global enable is also enabled. SPIF is a software clear interrupt.

23.3.11 Mode Fault

Error arises in a multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a mode fault.

When the SPI system is configured as a master and the /SS input line goes to active low, a mode fault error has occurred — usually because two devices have attempted to act as master at the same time. In cases where more than one device is concurrently configured as a master, there is a chance of contention between two pin drivers. For push-pull CMOS drivers, this contention can cause permanent damage. The mode fault mechanism attempts to protect the device by disabling the drivers. The MSTR & SPE control bits in the SPCR associated with the SPI are cleared and an interrupt is generated subject to masking by the ESPI control bit.

Other precautions may need to be taken to prevent driver damage. If two devices are made masters at the same time, mode fault does not help protect either one unless one of them selects the other as slave. The amount of damage possible depends on the length of time both devices attempt to act as master.

MODF bit is set automatically by SPI hardware, if the MSTR control bit is set and the slave select input pin becomes 0. This condition is not permitted in normal operation. In the case where /SS is set, it is an output pin rather than being dedicated as the /SS input for the SPI system. In this special case, the mode fault function is inhibited and MODF remains cleared. This flag is cleared by software.

The following figures show the sample hardware connection for multi-master/slave environment, and flow diagram which shows how s/w handles mode fault.

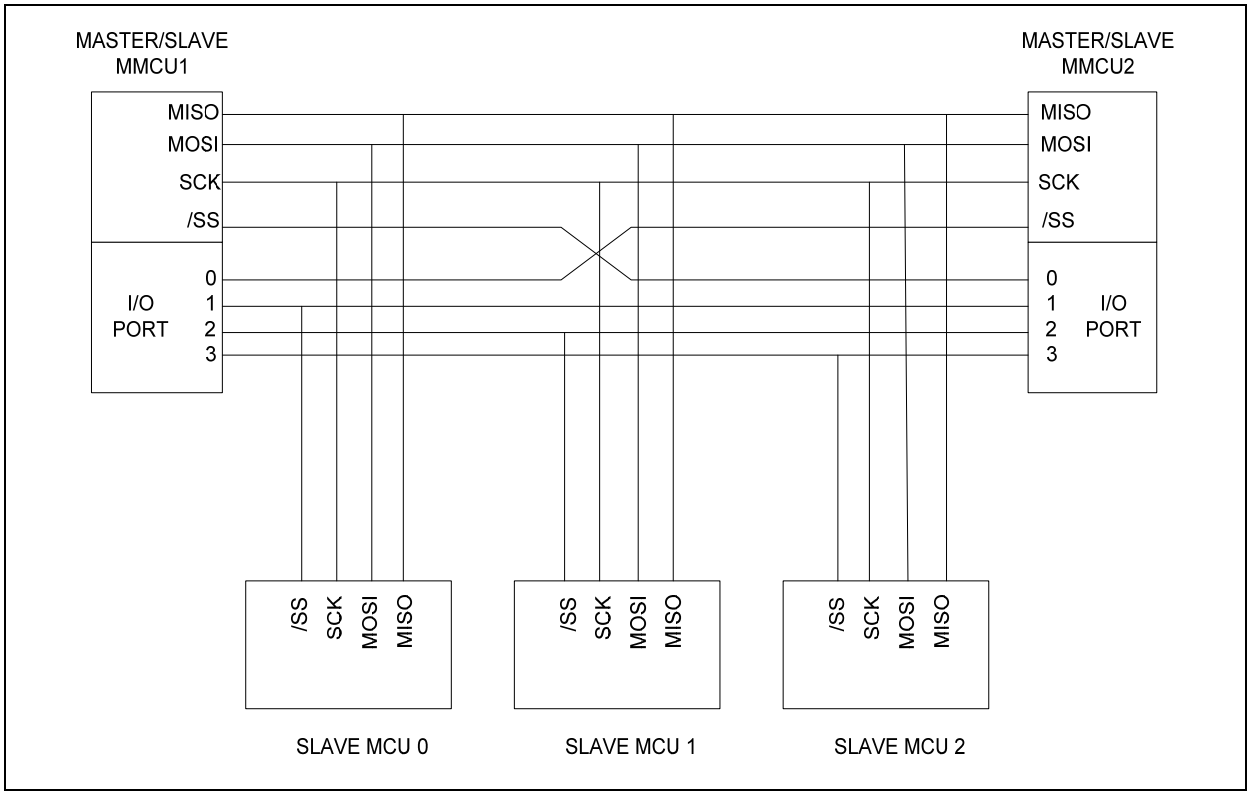


Figure 23-12 SPI multi-master slave environment

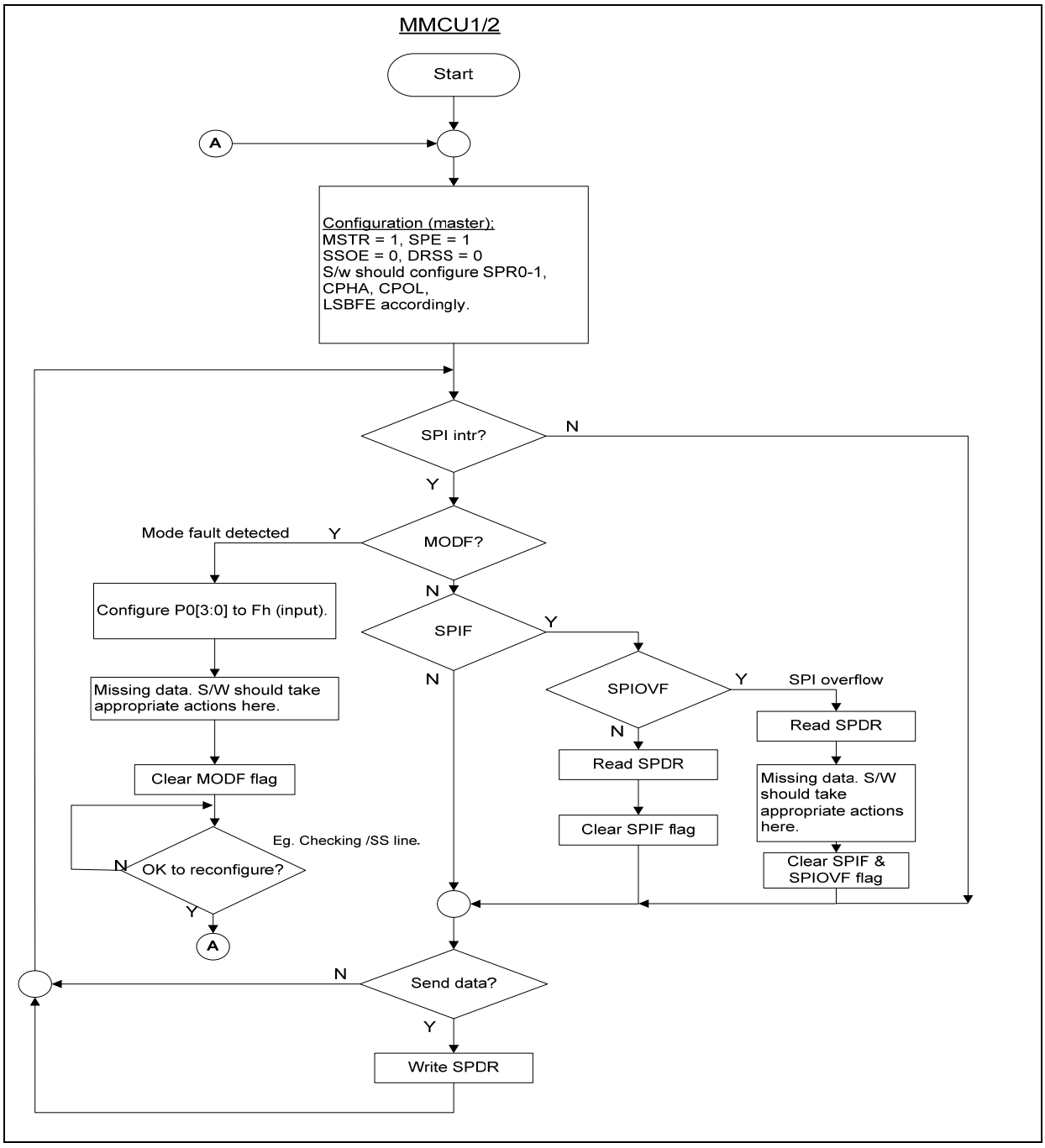


Figure 23-13 SPI multi-master slave s/w flow diagram

24 TIMED ACCESS PROTECTION

In this MCU, some functions are crucial to proper operation of the system like the Watchdog Timer. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, it has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

There registers, PDTC0(AEh), DTCNT(ABh) and WDCON(D8h) have the timed access protection when CPU has a write access to one of the three registers.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h        ; Define new register TA, located at 0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
MOV     TA, #0AAh       ; 3 M/C; Note: M/C = Machine Cycles
MOV     TA, #055h       ; 3 M/C
MOV     WDCON, #00h     ; 3 M/C
```

Example 2: Valid access

```
MOV     TA, #0AAh       ; 3 M/C
MOV     TA, #055h       ; 3 M/C
NOP                     ; 1 M/C
SETB    EWRST           ; 2 M/C
```

Example 3: Valid access

```
 MOV    TA, #0Aah               ; 3 M/C
MOV     TA, #055h               ; 3 M/C
ORL     WDCON, #00000010B  ; 3M/C
```

Example 4: Invalid access

```
MOV     TA, #0AAh       ; 3 M/C
```

```
MOV     TA, #055h       ; 3 M/C
NOP                     ; 1 M/C
NOP                     ; 1 M/C
CLR     EWT             ; 2 M/C
```

Example 5: Invalid Access

```
MOV     TA, #0AAh       ; 3 M/C
NOP                     ; 1 M/C
MOV     TA, #055h       ; 3 M/C
SETB    EWT             ; 2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles' window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

25 PULSE-WIDTH-MODULATED (PWM) OUTPUTS

In SA8218, the build-in PWM function is specially designed for driving motor control applications. Using the PWM and timer2/input capture module with proper control flow by software can drive 3-phase Brushless DC motor, 3-phase AC induction motor and DC motor.

25.1 PWM Features

The PWM block supports the features as below;

- Four independent 12-bit PWM duty control units with maximum 8 port pins:
  - 4 independent PWM output: PWM0, PWM2, PWM4 and PWM6
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion:
    (PWM0,PWM1), (PWM2,PWM3) and (PWM4,PWM5)
  - 3 synchronous PWM pairs, with each pin in a pair in-phase:
    (PWM0,PWM1), (PWM2,PWM3) and (PWM4,PWM5)
- Group control bit:
  PWM2 and PWM4 are synchronized with PWM0
- Support Edge aligned mode and Center aligned mode.
- Programmable dead-time insertion between complementary paired PWMs.
- Each pin of from PWM0 to PWM5 has independent polarity setting control.
- Mask output control for Electrically Commutated Motor operation.
- Tri-state output at reset.
- Hardware brake protections.
- Support 2 independent interrupts.
  - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (edge aligned mode) or underflow (center aligned mode).
  - Interrupt is requested when external brake pins asserted
- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- High Source/Sink current.

After CPU reset the internal output of the each PWM channels depends on the polarity setting. The interval between successive outputs is controlled by a 12–bit up/down counter which uses the oscillator frequency with configurable internal clock pre-scalar as its input. The PWM counter clock has the frequency as the clock source $F_{PWM} = F_{CPU}$/Pre-scalar. The Figure 25-1 is the block diagram for PWM.

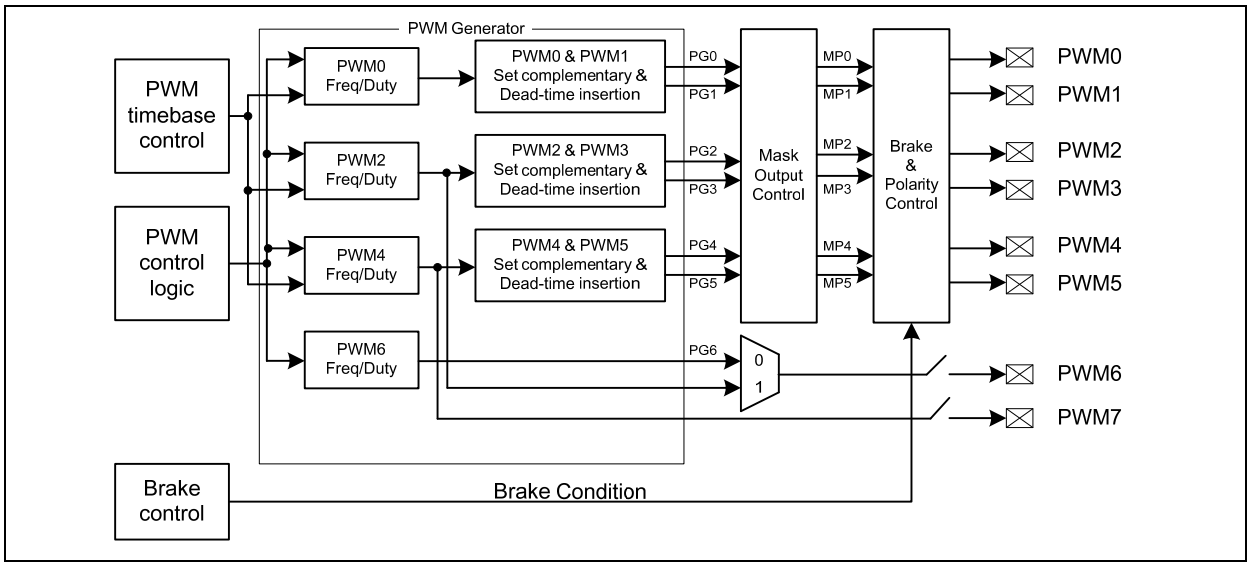


Figure 25-1: PWM Block Diagram

25.2 PWM Operation

The following diagram shows PWM time-base generator.

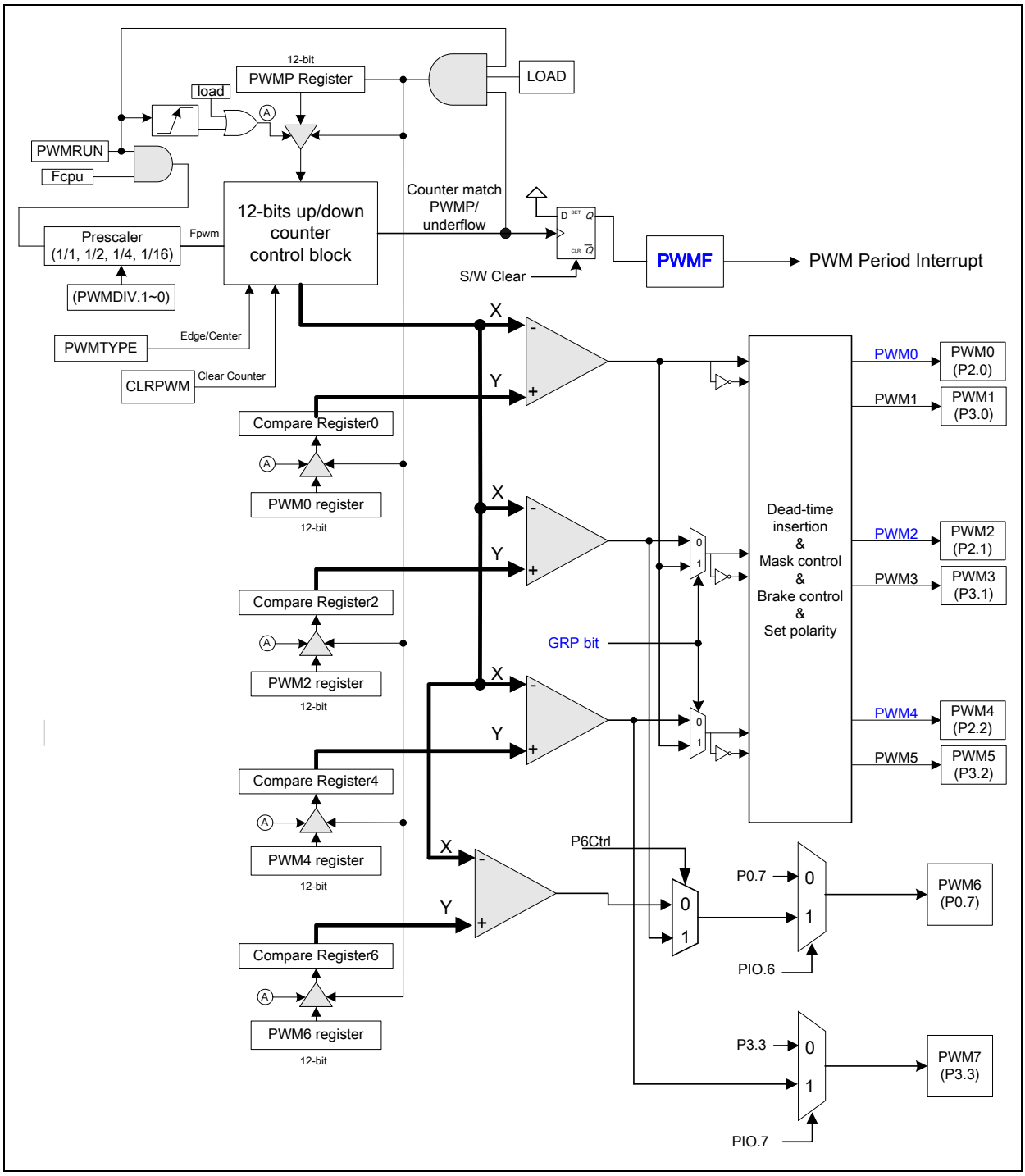


Figure 25-2: PWM Time-base Generator

The overall functioning of the PWM module is controlled by the contents of the PWMCON1, PWMB and PWMCON3 registers. The operation of most of the control bits is straightforward. PWMCON1.7 (PWMRUN) allows the PWM to be either in the run or idle state. The transfer of the data from the PWMP register to 12-bit counter will occur on the rising edge of PWMCON1.7 (PWMRUN) or during PWMRUN with PWMCON1.6 (load) and counter match/underflow occur. The transfer of the data from the PWMn registers to the compare registers is controlled by the PWMCON1.6 (load) (with condition that PWMRUN=1 and match/underflow occurs).

Notes:

- A compare value greater than the counter reloaded value resulted in the PWM output being permanently high. In addition there are two special cases. If compare register is set to 000H, the PWMn output will stay at low, and if compare register is set to FFFH, the PWMn output will stuck at high until there is a change in the compare register. [n = 0-3].
- During ICP mode, PWM pins will be tri-stated. PWM operation will be stop. When exit from ICP mode, the PWM pins will follow the last SFR port values.

The PWMP register fact that writes are not into the Counter register that controls the counter; rather they are into a holding register. The transfer of data from this holding register, into the register which contains the actual reload value, occurs when the following conditions are met; Load = 1, PWMRUN = 1 and PWM match/underflow. The width of each PWM output pulse is determined by the value in the appropriate compare register. Each PWM register pair of **(PWMPH,PWMPL), (PWM0H,PWM0L), (PWM2H,PWM2L), (PWM4H,PWM4L) and (PWM6H, PWM6L)**, in the format of 12-bit width by combining 4 LSB of high byte register and 8 bits of low byte register, decides the PWM period and each channel's duty cycle.

Please take note that duty registers PWM0~6 and period registers PWMP are double-buffered registers used to set the duty cycle and counting period for the PWM time base respectively. For the 1st buffer it is accessible by user while the 2nd buffer holds the actual compare value used in the present period. Load bit must be set to 1 to enable the value to be loaded in to the 2nd buffer register when counter underflow/match.

25.2.1 PWM Operation Mode

This device supports 2 operation modes: Edge-aligned and Centre-aligned mode.

The following equations show the formula for period and duty for each pwm operation mode:

Edge aligned:

Period = (PWMP +1) * CPU clock period/pre-scalar

Duty = duty * CPU clock period /pre-scalar

Centre aligned:

Period = (PWMP* 2) * CPU clock period/pre-scalar

Duty = (duty*2 - 1) * CPU clock period/pre-scalar

Note: "duty" refers to PWM0/2/4/6 register value.

25.2.2 Edge aligned PWM (up-counter)

In Edge-aligned PWM Output mode, the 12 bits counter will starts counting from 0 to match with the value of the duty cycle PWM0 (old), when this happen it will toggle the PWM0 generator output to low. The counter will continue counting to match with the value of the period register PWMP (old), at this

moment, it toggles the PWM0 generator output to high and new PWM0 (new) and PWMP(new) are updated with Load=1 and request the PWM interrupt if PWM interrupt is enabled(EIE1.6=1).

Figure 25-3, Figure 25-4 and Figure 25-5 depict the Edge-aligned PWM timing and operation flow.

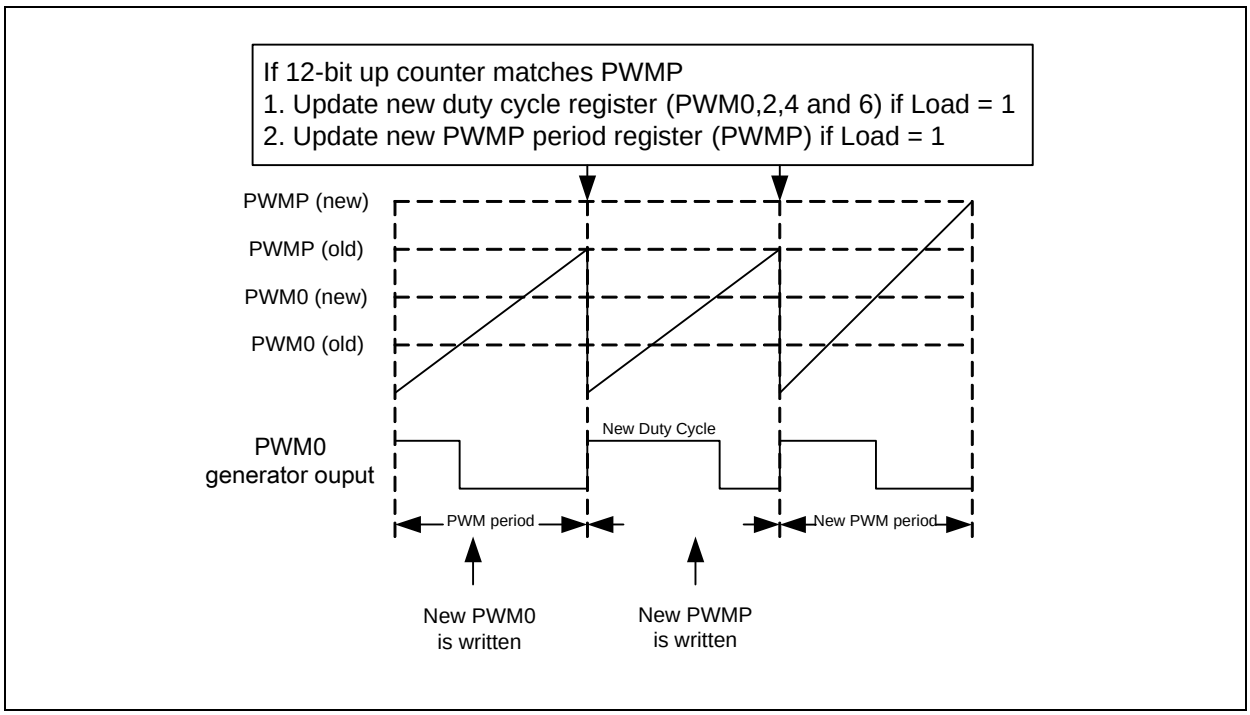


Figure 25-3: Edge-Aligned PWM

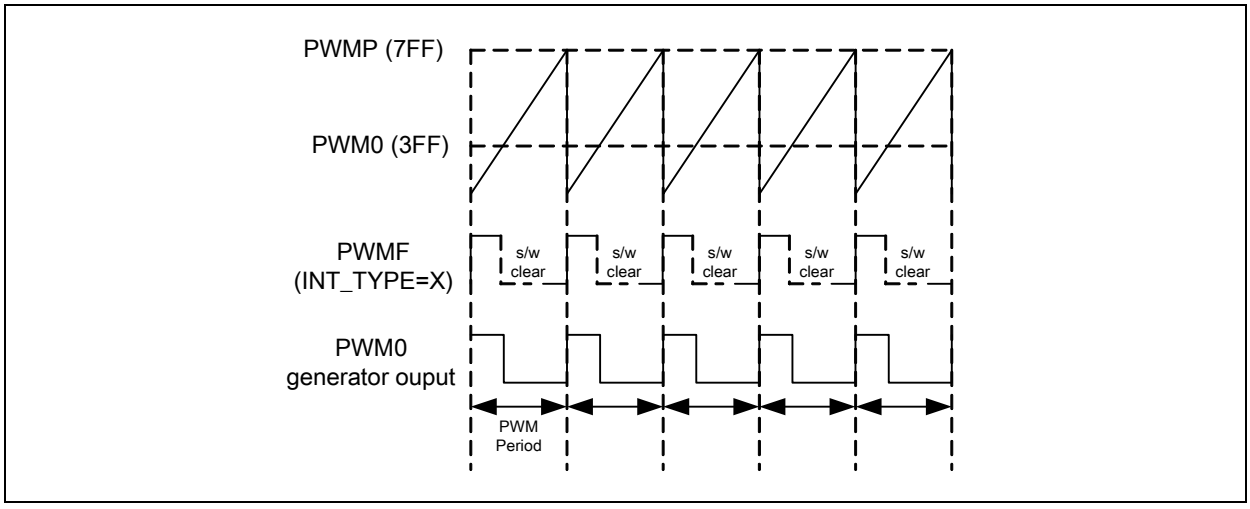


Figure 25-4: PWM0 Edge Aligned Waveform Output

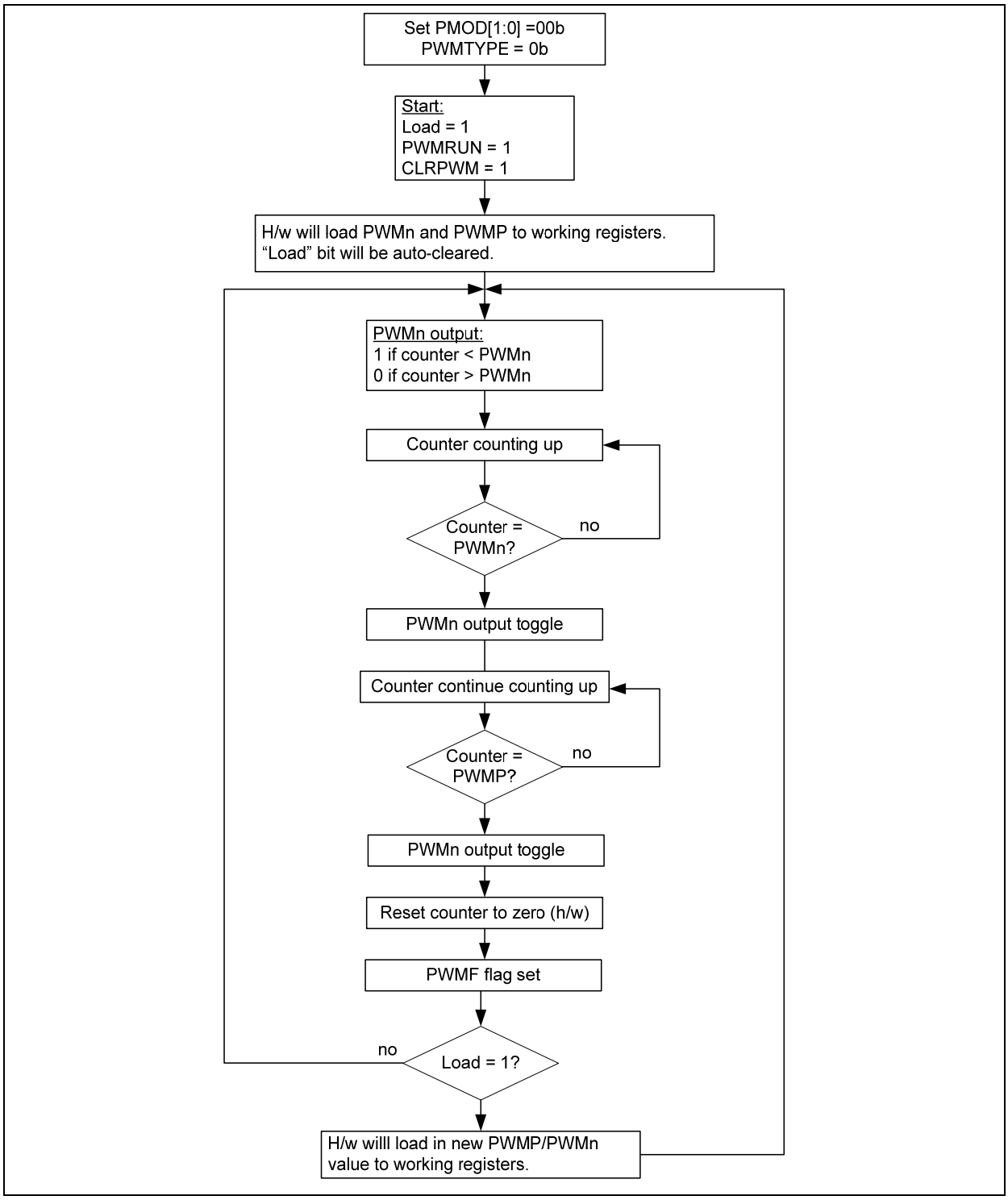


Figure 25-5: Edge-Aligned Flow Diagram

25.2.3 Center Aligned PWM (up/down counter)

The Center-aligned PWM signals are produced by the module when the PWM time base is configured in an Up/Down Counting mode. The counter will start counting-up from 0 to match the value of PWM0 (old), this will cause the toggling of the PWM0 generator output to low. The counter will continue counting to match with the PWMP (old). Upon reaching this states counter is configured automatically to down counting, when counter matches the PWM0 (old) value again the PWM0 generator output toggles to high. Once the counter underflows it will update the PWM period register PWMP(new) and duty cycle register PWM0(new) with Load = 1.

In Center-aligned mode, the PWM interrupt is requested at down-counter underflow if INT_TYPE (PWMCON3.0)=0 or at up-counter matching with PWMP if INT_TYPE(PWMCON3.0)=1.

Figure 25-6, Figure 25-7 and Figure 25-8 depict the Center-aligned PWM timing and operation flow.

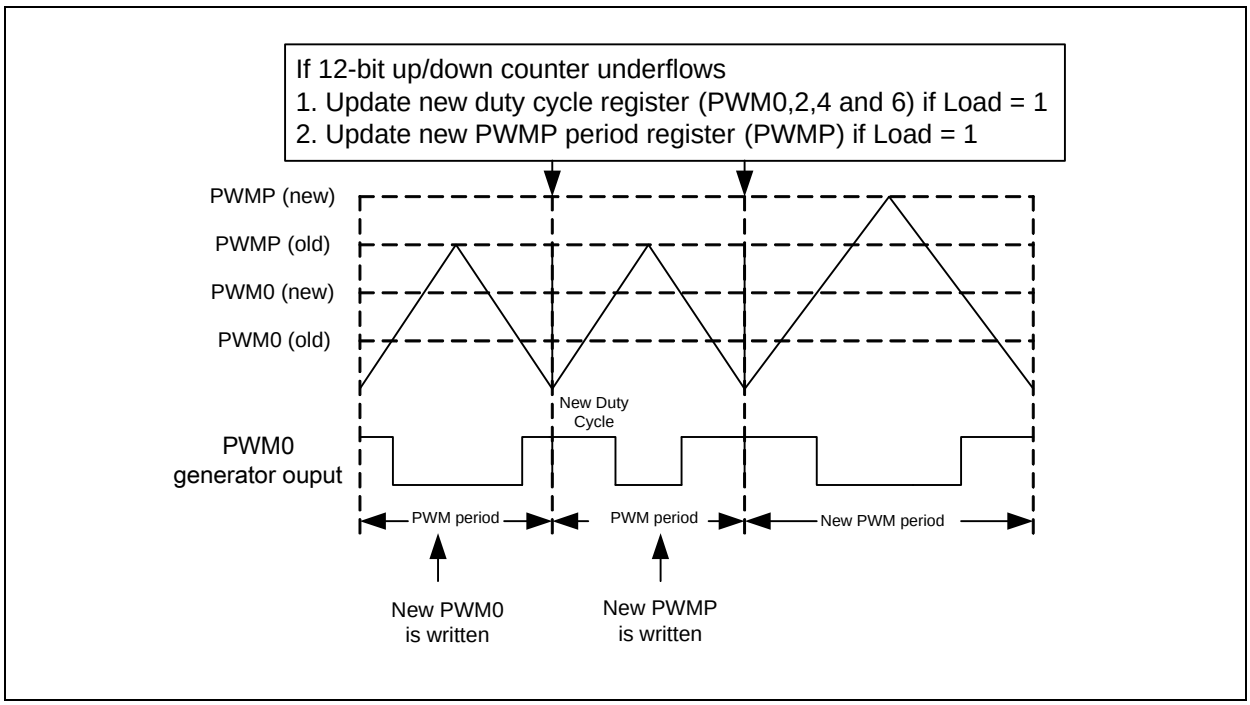


Figure 25-6: Center-Aligned Mode

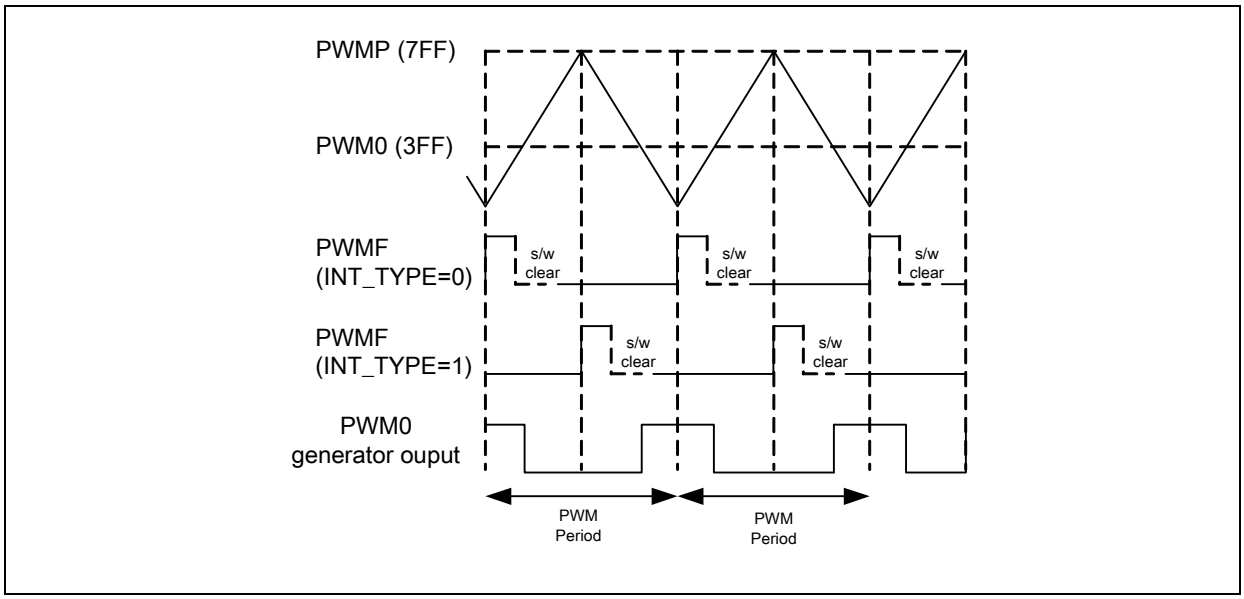


Figure 25-7: PWM0 Center Aligned Waveform Output

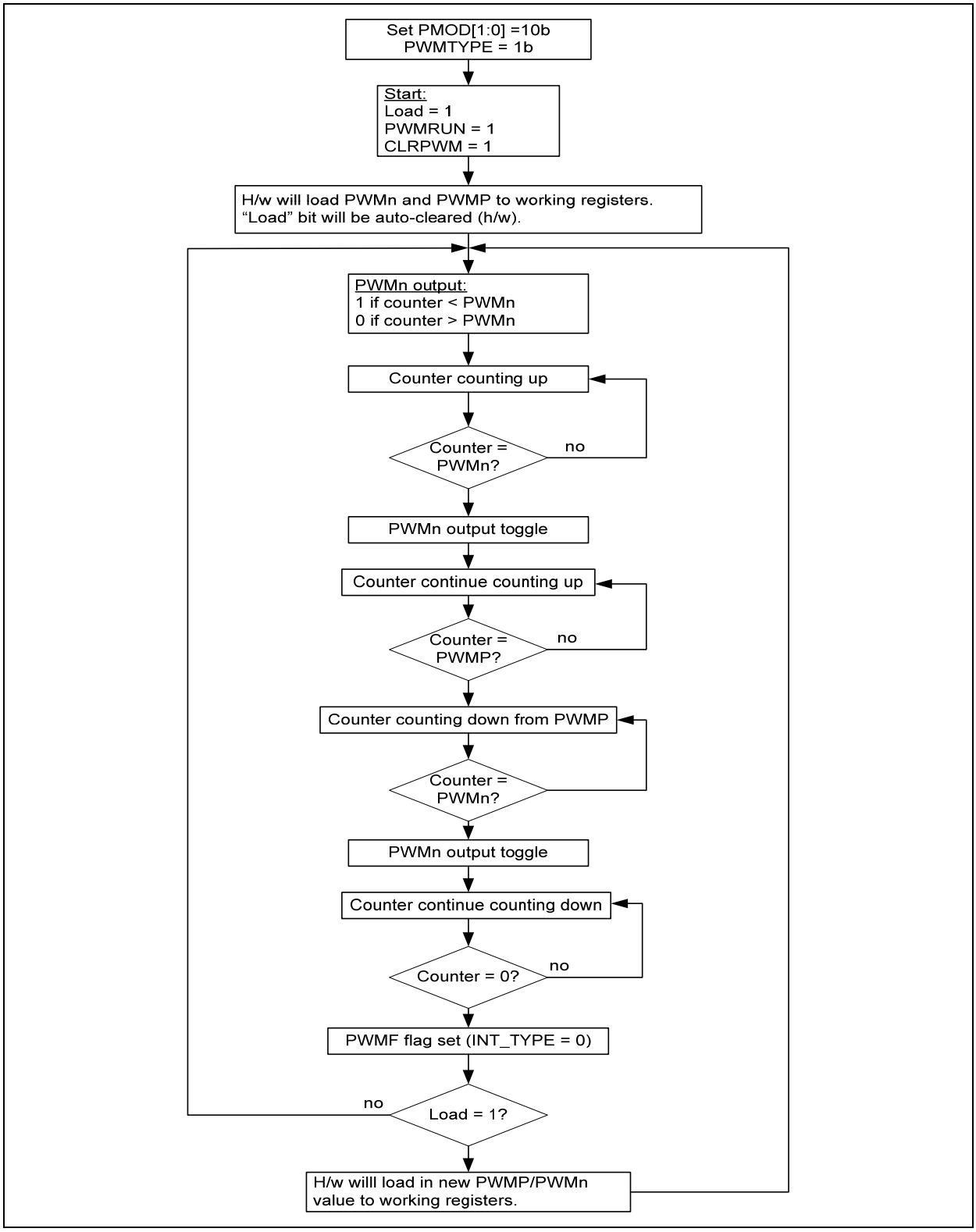


Figure 25-8: Center-aligned Flow Diagram (INT_TYPE = 0)

25.3 PWM Brake Function

This device supported 2 external brake pins; BKP0 and BKP1 pins. Both brake pins have each a 4-degree digital filter that is user controllable through BKnFILT.1-0 bits (n=0,1). The Brake function is controlled by the contents of the SFR PWMCON1-4 registers.

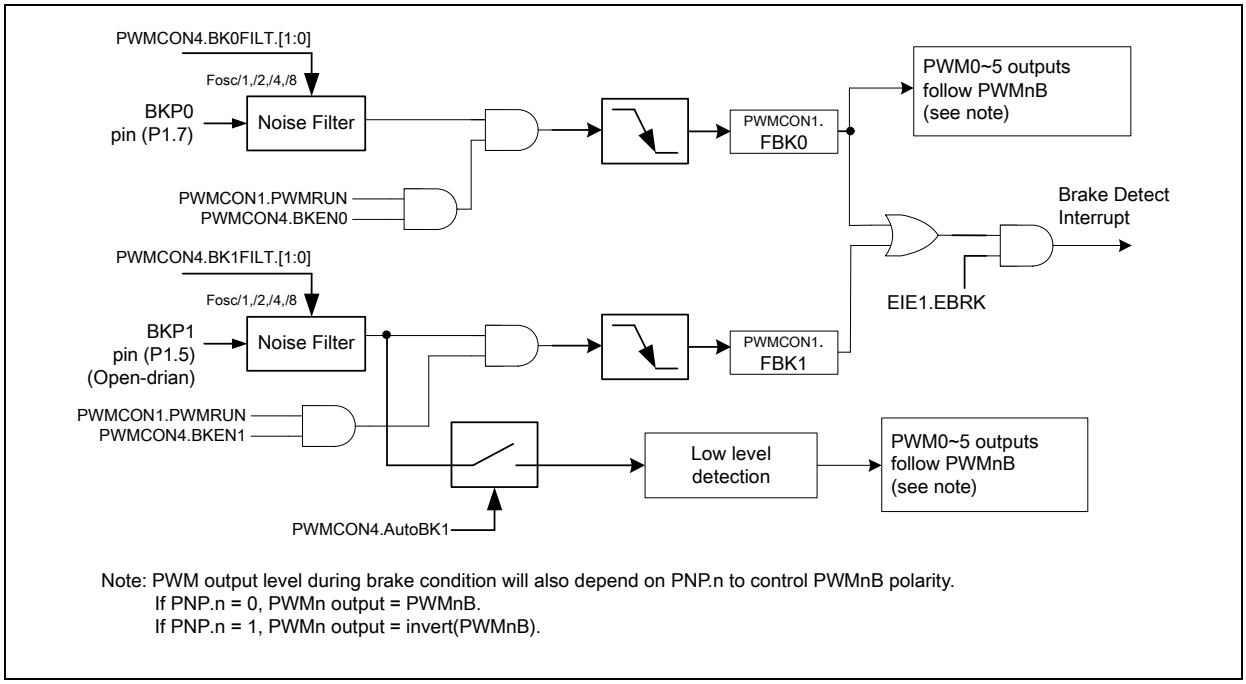


Figure 25-9: PWM Brake Function

The following table summaries the effect of each brake pins; the Figure 25-10 and Figure 25-11 illustrate the brake signals vs PWM operation.

Brake Pin	Brake trigger condition	Actions
BKP0	A falling edge at BKP0	1. FBK0 flag set by H/W; but cleared by S/W. 2. PWM0~5 outputs follow PWMnB bits. PNP bits are also able to control the polarity of PWMnB. If PNP.n=0, PWMn pin output = PWMnB. If PNP.n=1, PWMn pin output = invert(PWMnB). 3. H/W sets PWMRUN=0 to stop PWM generator. 4. PWM0~5 pin outputs does not resume on release of BKP0 pin. PWM0~5 will remain in PWMnB state after the s/w clearing of FBK0 flag, if user keep PWMRUN = 0. If user re-enabled PWMRUN, the brake state will be release on next PWM cycle/period.
BKP1	A falling edge at BKP1; Low level state	1. FBK1 flag set by the falling edge at BKP1; but cleared by S/W. 2. If AUTOBK1=1 and BKP1 detected as low level, PWM0~5 pin outputs follow PWMnB bits.

		Otherwise, PWM0~5 will continue follow PWM generators' output. In both situations, PNP bits are also able to control port polarity. 3. PWMRUN bit remain asserted to keep PWM generators running. 4. PWM0~5 resume if BKP1 pin state returns to high state. PWM0~5 will resume on start of next PWM cycle/period.

Note that user require to enable brake enable bits, BKENn, in order for the above to be effective.

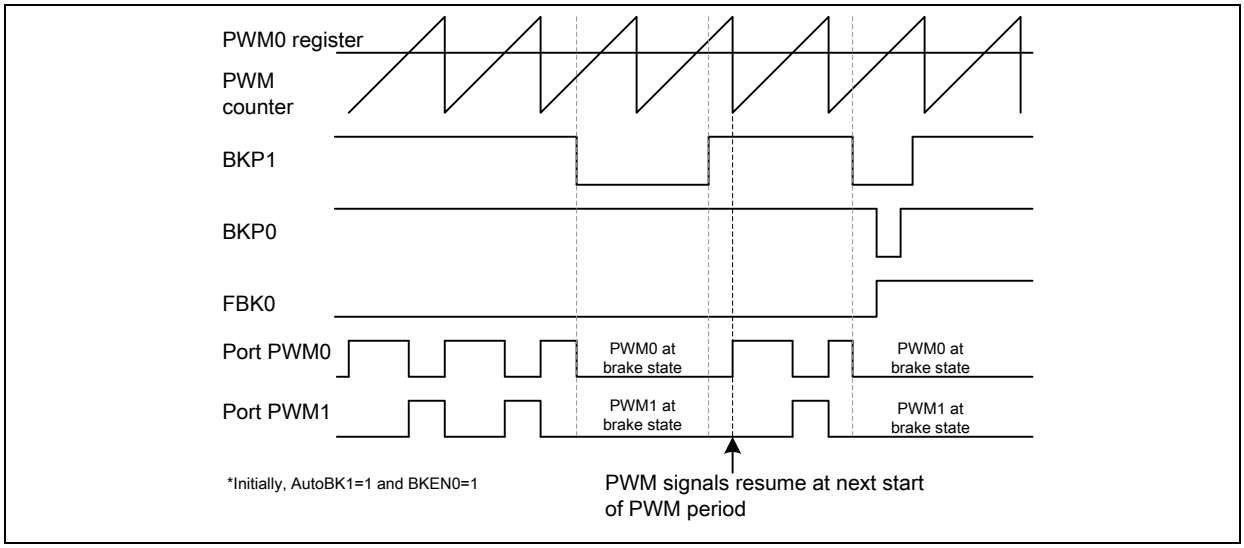


Figure 25-10: PWM brake condition (edge aligned mode)

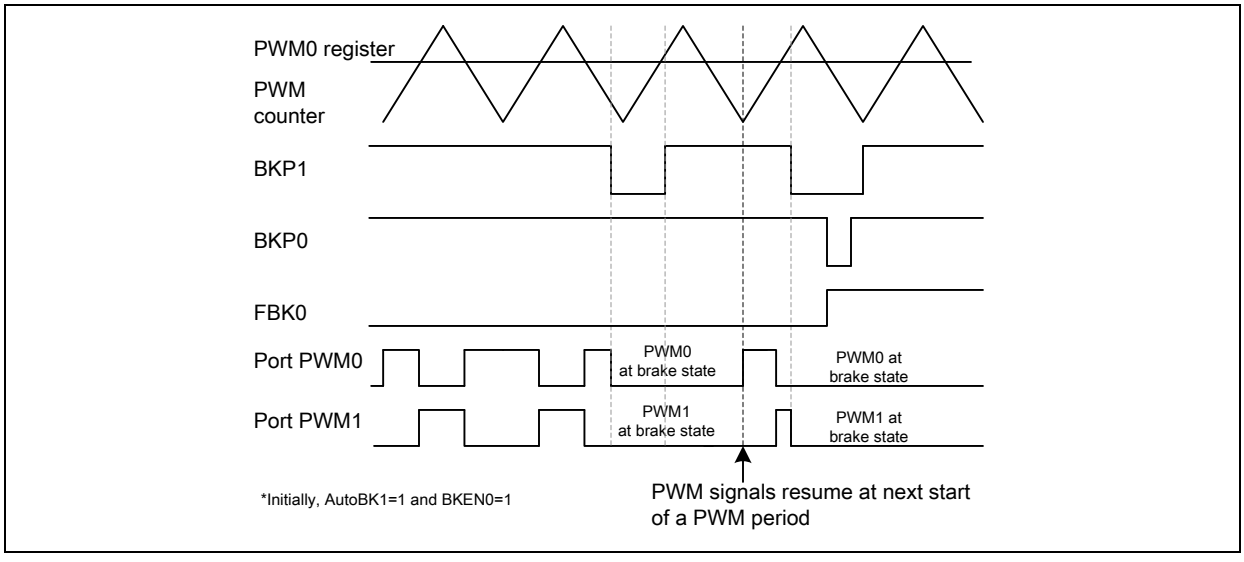


Figure 25-11: PWM brake condition (centre aligned mode)

Since the both brake conditions being asserted will automatically cause FBKn flag will be set, the user program can poll these brake flag bits or enable PWM's brake interrupt to determine which condition

causes a brake to occur.

25.4 PWM Output Driving Control

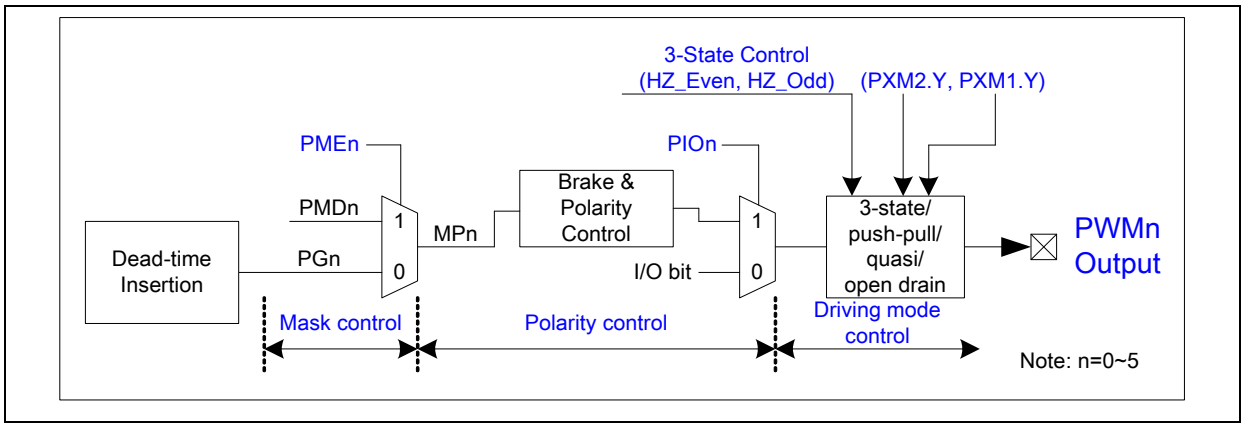


Figure 25-12: PWM Output Driving Control

The driving type of PWM output ports can be initialized as Tri-state type or other type dependent with SFR PxMy setting after any reset. As show in the above diagram, PWM output structures are controllable through option bits (config1.0-1), SFR (PWMCON3.HZ_Even,HZ_Odd) bits and SFR PxMy mode registers.

HZ_Even/HZ_Odd (SFR PWMCON3 BITS)	PWM Output Drive mode
0	Depend on PxMy SFR.
1	Driving mode = Hi-Z.

Note: SFR bits for HZ_Even and HZ_Odd are latched from config1.0 and config1.1, respectively, during all reset.

25.5 PWM modes

This powerful PWM unit supports Independent mode which may be applied to DC and BLDC motor system, Complementary mode with dead-time insertion which may be used in the application of AC induction motor and synchronous motor, Synchronous mode that makes both pins of each pair are in phase. Besides, the Group mode, forces the PWM0, PWM2 and PWM4 synchronous with PWM0 generator, may simplify updating duty control in DC and BLDC motor applications.

25.5.1 Independent mode

Independent mode is enabled when PMOD.1-0 = 00b.

On default, the PWM is operating in independent mode, with four PWM even channels outputs: PWM0, PWM2, PWM4 and PWM6. Each channel is running off its own duty-cycle generator module.

PWM6 can be user controllable to output from PWM2 generator if P6CTRL = 1.

PWM7 is taking output from PWM4 generator.

25.5.2 Complementary mode

Complementary mode is enabled when PMOD.1-0 = 01b.

In this module there are three duty-cycle generators utilized for complementary mode, with total of three PWM output pair pins in this module. The total six PWM outputs are grouped into output pairs of even and odd numbered outputs. In complimentary modes, the internal odd PWM signal PGx, refer to Figure 25-1, must always be the complement of the corresponding even PWM signal. For example, PG1 will be the complement of PG0. PG3 will be the complement of PG2 and PG5 will be the complement of PG4. The time base for the PWM module is provided by its own 12-bit timer, which also incorporates selectable pre-scalar options.

25.5.2.1 Dead-Time Insertion

The dead time generator inserts an “off” period called “dead time” between the turnings off of one pin to the turning on of the complementary pin of the paired pins. This is to prevent damage to the power switching devices that will be connected to the PWM output pins. The complementary output pair mode has an 8-bit counter used to produce the dead time insertion. The complementary outputs are delayed until the timer counts down to zero.

The dead-time can be calculated from the following formula:

Dead-time = F_{CPU} * (DTCNT.[7:0]+1).

The timing diagram below indicates the dead time insertion for one pair of PWM signals.

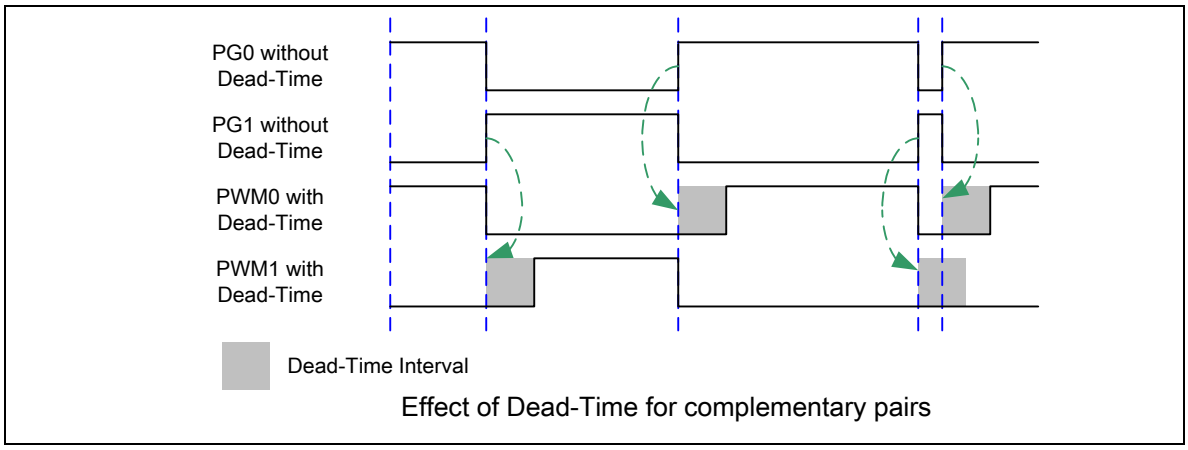


Figure 25-13: Dead-Time Insertion

PDTC0 and DTCNT have time access protection in writing access. In Power inverter application, a dead time insertion avoids the upper and lower switches of the half bridge from being active at the same time. Hence the dead time control is crucial to proper operation of a system. Some amount of time must be provided between turning off of one PWM output in a complementary pair and turning on the other transistor as the power output devices cannot switch instantaneously.

25.5.3 Synchronous mode

Synchronous mode is enabled when PMOD.1-0 = 10b.

In the synchronization mode the PWM pair signals from PWM Generator are in-phase.

PG1=PG0, PG3=PG2 and PG5=PG4.

25.5.4 Group mode

Group mode is enabled when PMOD.1-0 = 11b.

This device support Group Mode control. This control allows all even PWM channels output to be duty controllable by PWM0 duty register.

If GRP = 1, both (PG2, PG3) and (PG4, PG5) pairs will follow (PG0, PG1), which imply;

PG4 = PG2 = PG0;

PG5 = PG3 = PG1 = invert (PG0) if Complementary mode is enabled (PMOD.1-0=01b)

25.6 Polarity Control

Each PWM port of from PWM0 to PWM5 has independent polarity control to configure the polarity of active state of PWM output. At default, the PWM output is active high. This implies the PWM OFF state is low and ON state is high. This is controllable through SFR PNP on each individual PWM channel.

The following diagram show the initial state before PWM starts with different polarity settings.

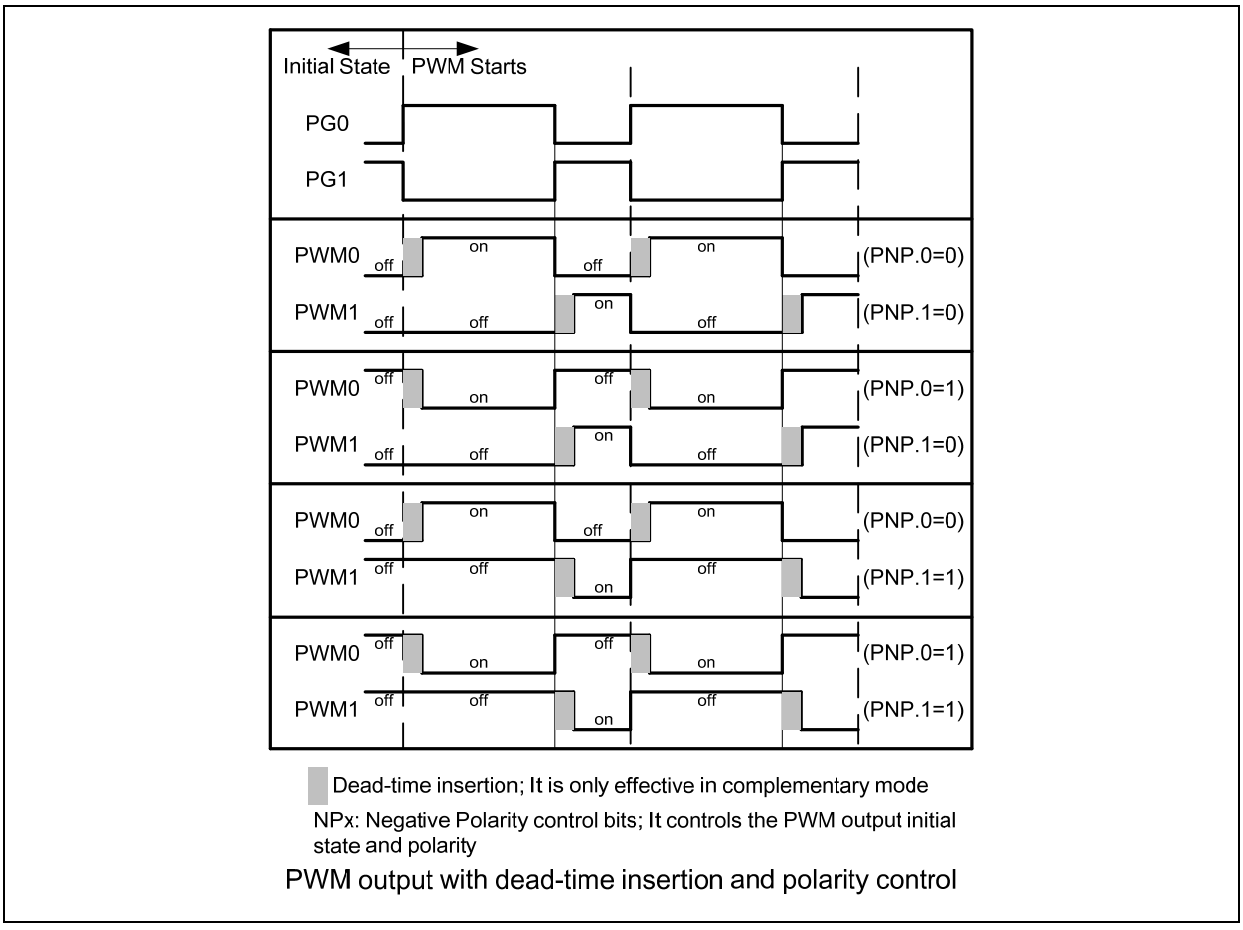


Figure 25-14: Initial state and polarity control with rising edge dead time insertion

25.7 PWM Mask Output

Each of the PWM output channels can be manually overridden by using the appropriate bits in the SFR PME and PMD registers to drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units. The PWM mask bits are useful when controlling various types of Electrically Commutated Motor (ECM) like a BLDC motor. The PMD register contains six bits,

PMD[5:0] determine which PWM I/O pins will be overridden. On reset PMD is 00H.

The PME register contains six bits, PME[5:0] determine the state of the PWM I/O pins when a particular output is masked via the PMD bits. On reset PME is 00H. The PME[5:0] bits are active-high. When the PME[5:0] bits are set, the corresponding PMD[5:0] bit will have effect on the PWM channel. When one of the PME bits is sets, the output on the corresponding PWM I/O pin will be determined by the state of the PMD bit and polarity control bit.

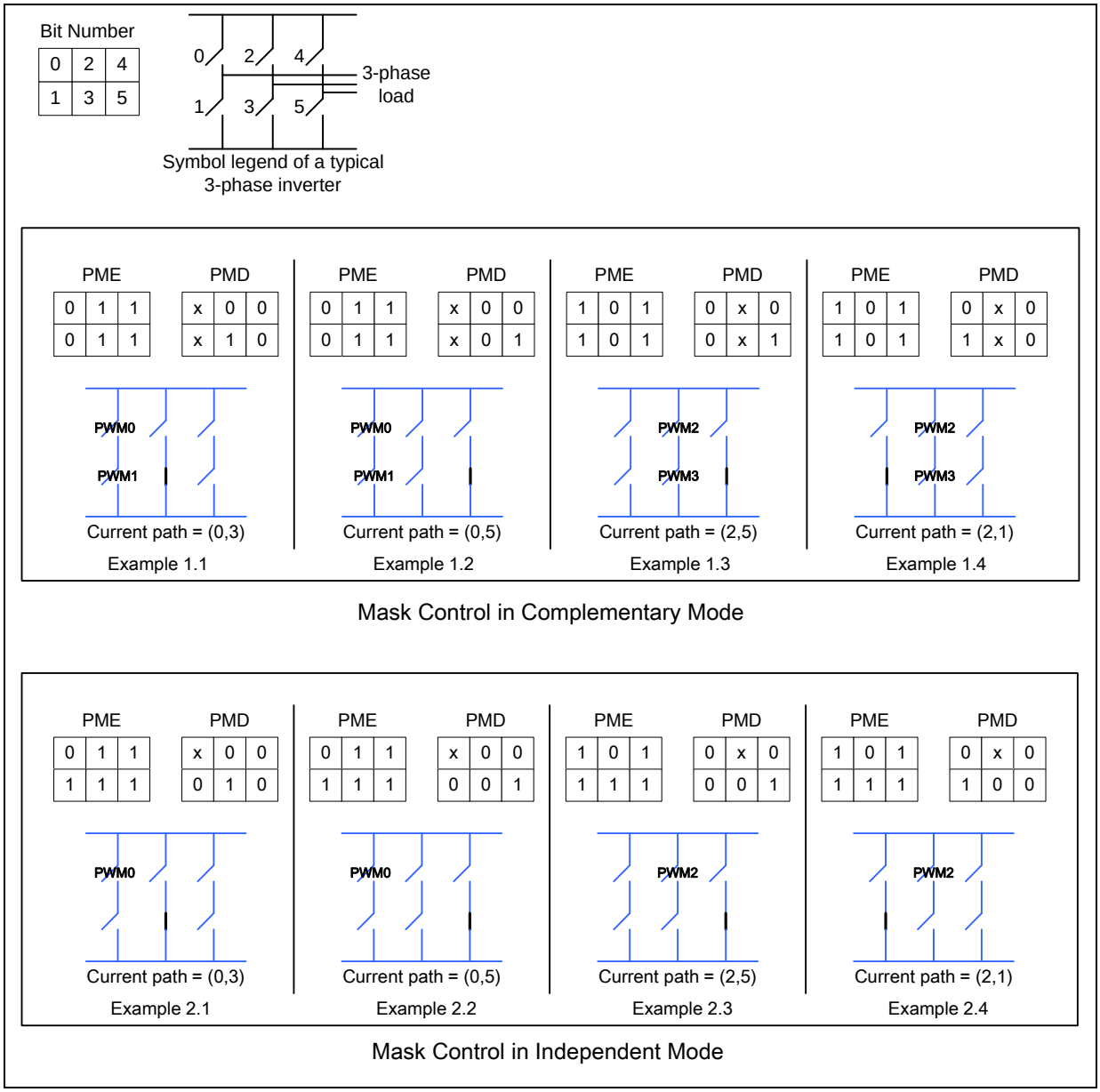


Figure 25-15 Illustration of Mask Control

Figure above shows example of how PWM mask control can be used for the override feature.

In example 1.1; PME[5:0] = 11 1100b, PMD[5:0] = 0010xxb (complementary mode)

- PWM channels 2-5 are masked from pwm frequency/duty generators.
- PWM channels 2-5 outputs are determined by state of PMD bits.
- PWM channels 0 and 1 follow pwm generator.

Switch 0 (On/Off) : Control by PWM0 (pwm0 frequency/duty generator).

Switch 1 (On/Off) : Control by PWM1 (inverted of PWM0, complementary mode).

Switch 2 (Off) : PMD.2 = 0.

Switch 3 (On) : PMD.3 = 1.

Switch 4 (Off) : PMD.4 = 0.

Switch 5 (Off) : PMD.5 = 0.

In example 1.3; PME[5:0] = 11 0011b, PMD[5:0] = 10xx00b (complementary mode)

- PWM channels 0, 1, 4 and 5 are masked from pwm frequency/duty generators.
- PWM channels 0, 1, 4 and 5 outputs are determined by state of PMD bits.
- PWM channels 2 and 3 follow pwm generator.

Switch 0 (Off) : PMD.0 = 0.

Switch 1 (Off) : PMD.1 = 0.

Switch 2 (On/Off) : Control by PWM2 (pwm2 frequency/duty generator).

Switch 3 (On/Off) : Control by PWM3 (inverted of PWM2, complementary mode).

Switch 4 (Off) : PMD.4 = 0.

Switch 5 (On) : PMD.5 = 1.

In example 2.1; PME[5:0] = 11 1110b, PMD[5:0] = 00100xb (independent mode)

- PWM channels 1-5 are masked from pwm frequency/duty generators.
- PWM channels 1-5 outputs are determined by state of PMD bits.
- PWM channel 0 follow pwm generator.

Switch 0 (On/Off) : Control by PWM0 (pwm0 frequency/duty generator).

Switch 1 (Off) : PMD.1 = 0.

Switch 2 (Off) : PMD.2 = 0.

Switch 3 (On) : PMD.3 = 1.

Switch 4 (Off) : PMD.4 = 0.

Switch 5 (Off) : PMD.5 = 0.

In example 2.3; PME[5:0] = 11 1011b, PMD[5:0] = 100x00b (independent mode)

- PWM channels 0,1,3,4 and 5 are masked from pwm frequency/duty generators.
- PWM channels 0,1,3,4 and 5 outputs are determined by state of PMD bits.
- PWM channel 2 follow pwm generator.

Switch 0 (Off) : PMD.0 = 0.

Switch 1 (Off) : PMD.1 = 0.

Switch 2 (On/Off) : Control by PWM2 (pwm2 frequency/duty generator).

Switch 3 (Off) : PMD.3 = 0.

Switch 4 (Off) : PMD.4 = 0.

Switch 5 (On) : PMD.5 = 1.

25.8 SFR of PWM Unit

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
PWM6H	PWM 6 HIGH BITS REGISTER	FEH		-			PWM6.11	WM6.10	PWM6.9	PWM6.8	XXXX 0000b
PWM6L	PWM 6 LOW BITS REGISTER	FDH	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0	0000 0000b
PWMCON4	PWM CONTROL REGISTER 4	FCH	BK1FILT.1	BK1FILT.0	BK0FILT.1	BK0FILT.0	AUTOBK1	-	BKEN1	BKEN0	0000 0X00b
PMD	PWM MASK DATA REGISTER	EEH	-	-	PMD.5	PMD.4	PMD.3	PMD.2	PMD.1	PMD.0	XX00 0000b
PME	PWM MASK ENABLE REGISTER	EDH	-	-	PME.5	PME.4	PME.3	PME.2	PME.1	PME.0	XX00 0000b
PWMB	PWM BRAKE OUTPUT	DFH	-	-	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B	XX00 0000b
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000b
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	LOAD	PWMF	CLRPWM	FBK1	FBK0	PMOD.1	PMOD.0	0000 0000b
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000b
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000b
PWMCON3	PWM CONTROL REGISTER 3	D7H	HZ_Even	HZ_Odd	GRP	PWMTYPE	-	-	P6CTRL	INT_TYPE	XX00 XX00b
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	PWM2.11	PWM2.10	PWM2.9	PWM2.8	XXXX 0000b
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8	XXXX 0000b
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8	XXXX 0000b
PNP	PWM NEGATIVE POLRARITY	C3H	-	-	PNP.5	PNP.4	PNP.3	PNP.2	PNP.1	PNP.0	XX00 0000b
P3	PORT 3	B0H	(B7) P3.7	(B6) P3.6	(B5) P3.5	(B4) P3.4	(B3) P3.3 PWM7	(B2) P3.2 PWM5	(B1) P3.1 PWM3	(B0) P3.0 PWM1	1111 1111b[1] 0000 0000b
PDTC0	PWM DEAD TIME CONTROL 0 REGISTER	AEH	-	-	-	-	-	DTENB4	DTENB2	DTENB0	XXXX X000b
DTCNT	PWM DEAD TIME COUNTER REGISTER	ABH	DTCNT.7	DTCNT.6	DTCNT.5	DTCNT.4	DTCNT.3	DTCNT.2	DTCNT.1	DTCNT.0	0000 0000b
P2	PORT 2	A0H	(A7) P2.7 T1	(A6) P2.6 IC2 MOSI	(A5) P2.5 IC1 MISO	(A4) P2.4 IC0 /SS	(A3) P2.3 T3 SCLK	(A2) P2.2 PWM4	(A1) P2.1 PWM2 CP1O	(A0) P2.0 PWM0 CP2O	1111 1111b[1] 0000 0000b
PIO	PWM IO REGISTER	9BH	PIO.7	PIO.6	PIO.5	PIO.4	PIO.3	PIO.2	PIO.1	PIO.0	0000 0000b
PWM4H	PWM 4 HIGH BITS REGISTER	97H	-	-	-	-	PWM4.11	PWM4.10	PWM4.9	PWM4.8	XXXX 0000b
PWM4L	PWM 4 LOW BITS REGISTER	96H	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0	0000 0000b

Note:

1. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset

26 ANALOG-TO-DIGITAL CONVERTER (ADC)

N79E235 series support a 10-bit analog-to-digital converter (ADC) which contains a DAC which converts the contents of a successive approximation register to a voltage (V_{DAC}) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. This is illustrated in the figure below.

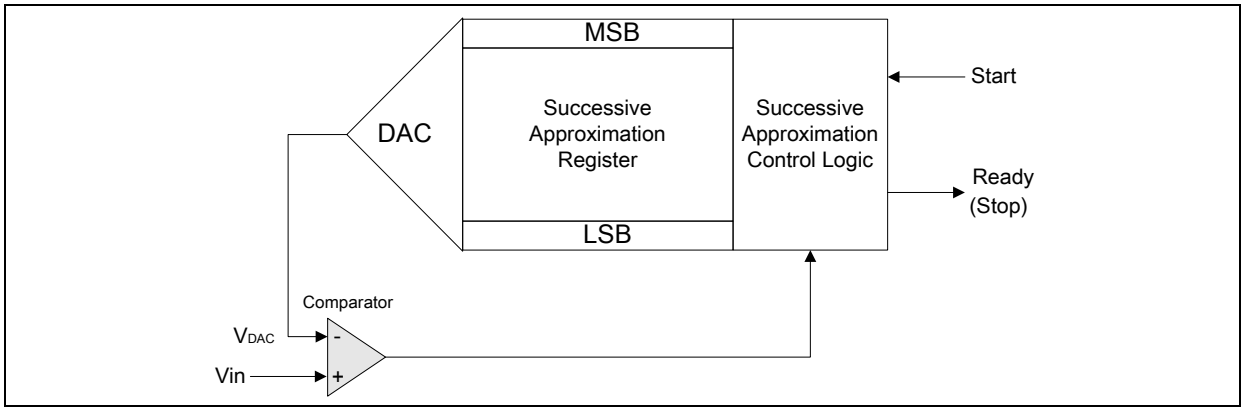


Figure 26-1: Successive Approximation ADC

26.1 Operation of ADC

26.1.1 Normal Operation of ADC

A conversion can be initiated by software only or by either hardware or software. The software only start mode is selected when control bit ADCCON.5 (ADCEX)=0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCEX =1, and a conversion may be started by setting ADCS as above or by applying a rising edge to external pin STADC(P1.7) or by a trigger signal synchronous with PWM unit. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle. When ADCCON.5 (ADCEX) is set by external pin to start ADC conversion, after N79E235 series have entered idle mode, STADC/P1.7 can start ADC conversion at least 1 machine cycle.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 34 ADC clock cycles. ADCI flag is set at end of ADC conversion. ADCS will be hardware cleared when ADCI is set.

Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are used to control an analog multiplexer which selects one of eight analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1.

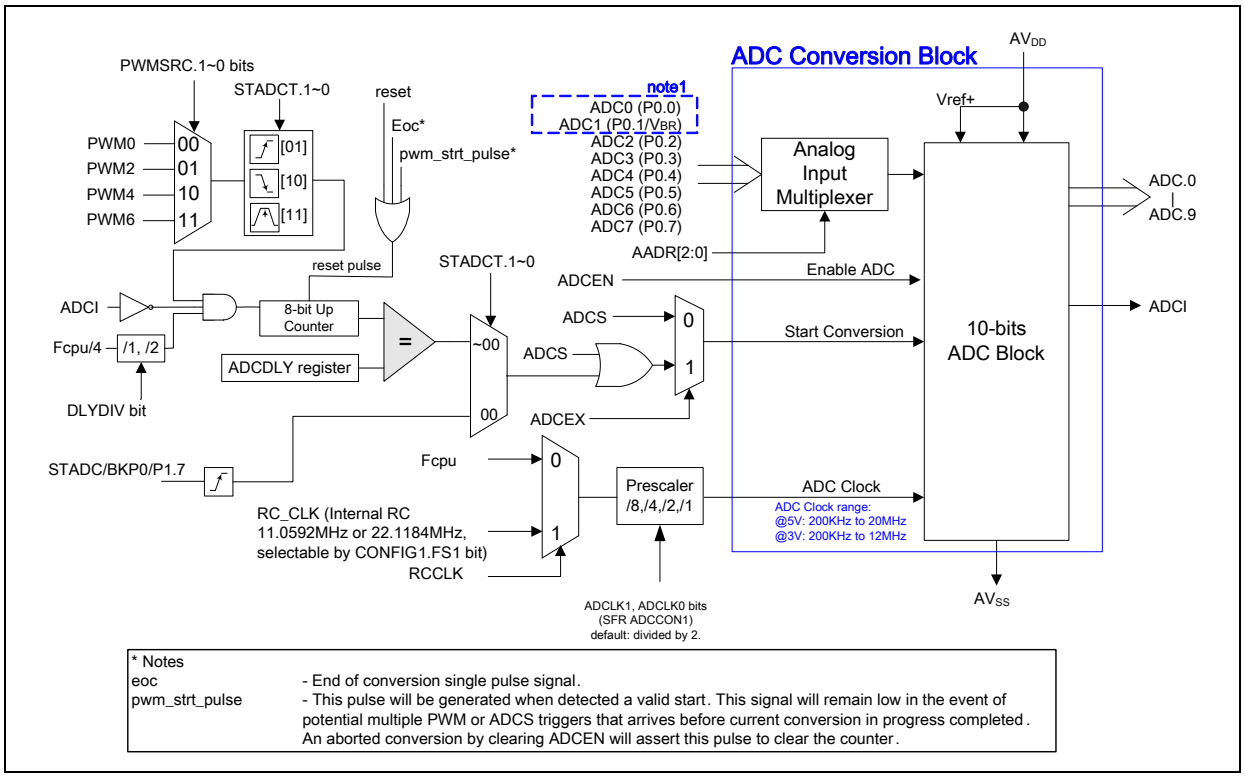


Figure 26-2: ADC Block Diagram

Note:

- SFR ADCCON1(E3H), ADCDLY(AFH) and bit AUXR1(A2H).RCCLK can be set/cleared only when ADC circuit is not enabled(AUXR1.ADCEN=0).
- The ADC1 alternative input source will come from Brownout Reference Voltage, V_{BR}. It can be selected through AUXR2.ADC1SEL bit. Refer to for selecting ADC1 source.

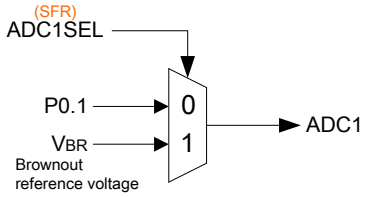


Figure 26-3: ADC1 source selections

26.1.2 ADC Start Synchronous with PWM

Besides software start and external pin STADC (P1.7) to start ADC conversion, this device has new feature to allow PWM ***even channels*** to trigger the ADC start. User may configure any one of the PWM as well as trigger types; rising, falling PWM edge or central point of PWM (centre-aligned mode only) to trigger ADC start. The device also allow user to configure the amount of delay prior to ADC start after hardware detected the PWM edge. See SFR ADCCON1 and ADCDLY for bits descriptions. Figure below shows the programmable delay time for PWM-triggered ADC start conversion. For PWM trigger ADC start conversion in centre align mode, ADC start conversion point will be at the same, regardless of which pwm channel is selected.

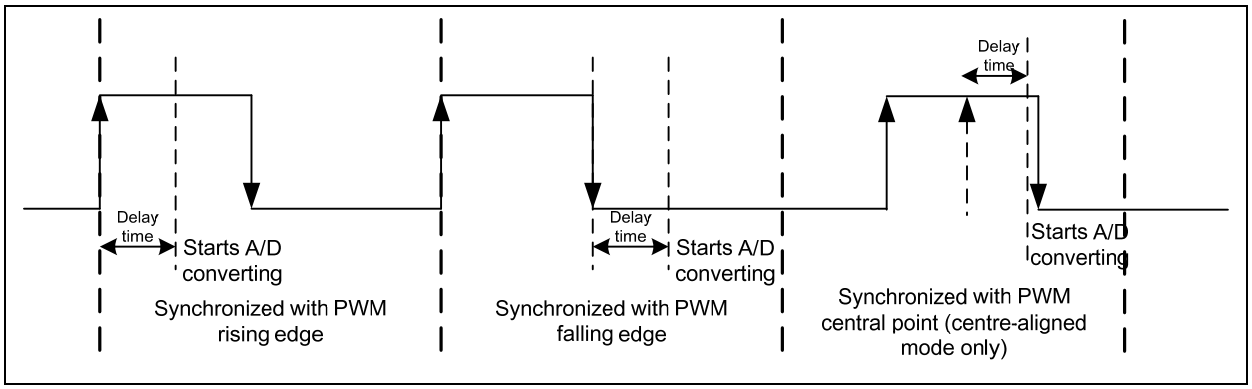


Figure 26-4: PWM-triggered ADC start

26.1.3 ADC Converting in Power-dwon and Idle Mode

When ADC is operating a conversion, the noise induced by CPU clock effects the ADC resolution. N79E235 series allows ADC converting in Power-down and Idle modes to minimize the noise from CPU. Software may enable ADC Interrupt in advanced then set ADCS=1 to start converting and follow setting PD=1(PCON.1) or IDL=1(PCON.0) to force CPU entering power-down or idle mode. When the conversion is completed, hardware requests ADC interrupt and release CPU from power-down or idle mode. Note that due to CPU clock stops in power-down mode, software must set RCCLK=1 to select ADC clock is from internal RC oscillator before CPU enter power-down mode.

26.2 ADC Resolution and Analog Supply:

The ADC circuit has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder that the AVDD and Vref+ are connected to VDD and AVSS is connected to VSS. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5×R above AVss, and the last tap is located 0.5×R below Vref+. This gives a total ladder resistance of 1024×R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between AVss and [(Vref+) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 1111111111B = 3FFH. Vref+ and AVSS may be between AV_{DD} + 0.2V and AV_{SS} – 0.2 V. Vref+ should be positive with respect to AVSS, and the input voltage (Vin) should be between Vref+ and AVSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{\text{Vin}}{\text{Vref}+} \quad \text{or Result} = 1024 \times \frac{\text{Vin}}{\text{VDD}}$$

26.3 ADC Continuous Mode

If ADC continuous mode is enabled, a repeated conversion of the selected channel will be performed until ADCCM or ADCS bit is cleared and the new 10-bit result will overwrite the old data. Unlike the normal ADC function ADCS is cleared automatically at the end of a conversion, in this mode, ADCS keeps high till software clear it or ADCCM is cleared and the last conversion is completed. Figure below explains the behavior of the ADC continuous mode.

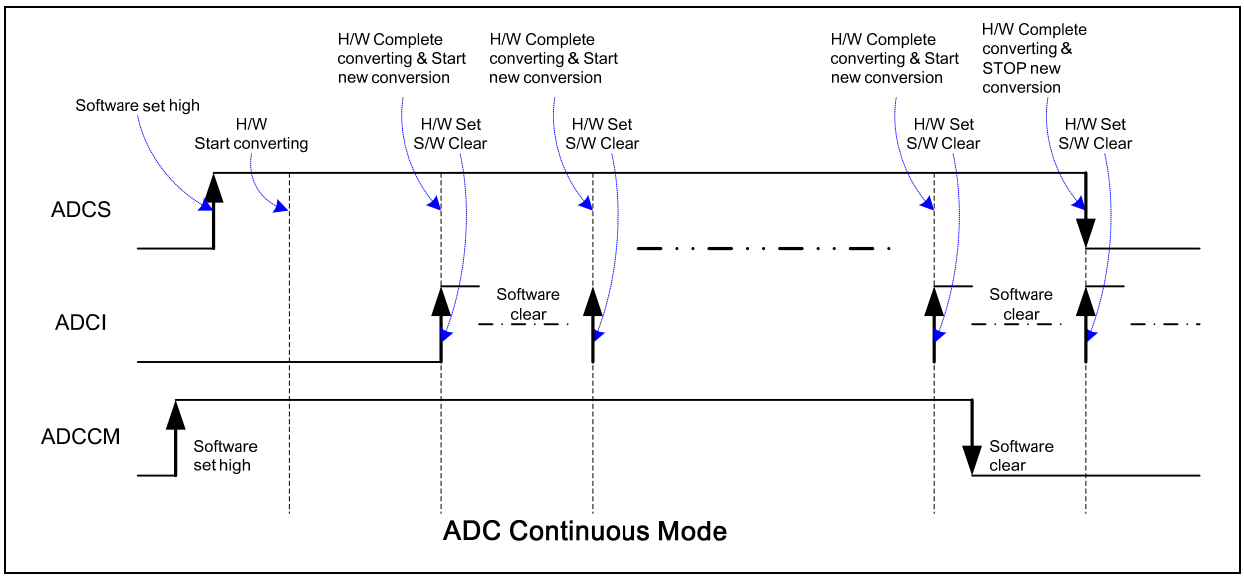


Figure 26-5: ADC Continuous Mode

26.4 ADC Compare Function

N79E235 ADC provides the compare function that compares the 10-bit ADC result and an arbitrary 10-bit reference data. The compare result places in ADCPO bit. When the new conversion result makes ADCPO bit change state, the ADCPI flag is set by H/W and an ADC interrupt is requested if EADCP bit is set in advanced. The block diagram of ADC compare function is shown in the following figure.

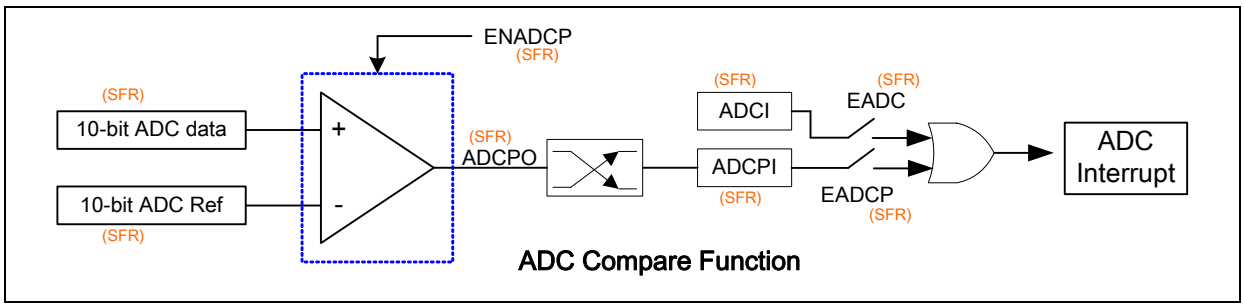


Figure 26-6: ADC Compare Function

The 10-bit reference data ADCR.9-0 bits (located at SFR ADCRH.7-0 and ADCRL.7-6) are writable only when ENADCP = 0. User will have to take of potential false trigger when changing the reference data. The following is the recommended procedure note when using ADC Compare function.

1. Disable ADC compare function (ENADCP=0).
2. Disable ADC compare function interrupt (EADCP=0).
3. Update 10-bit ADC Ref registers.
4. Clear ADCPI flag (this is to avoid unwanted compare trigger due to new reference data).
5. Enable ADC compare function (ENADCP=1).
6. Enable compare function interrupt (EADCP=1).
7. Start next ADC conversion.

27 ANALOG COMPARATORS

This device is also provided with two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause to an interrupt when the comparator output value changes. The block diagram is as below.

The inputs are CPnP and CPnN, and outputs CPnO (n = 1 or 2). User may select the internal reference voltage by enable SFR CMPn.CNn bit. The typical value of internal brownout reference voltage (V_{BR}) is about 1.16V +/- 10%.

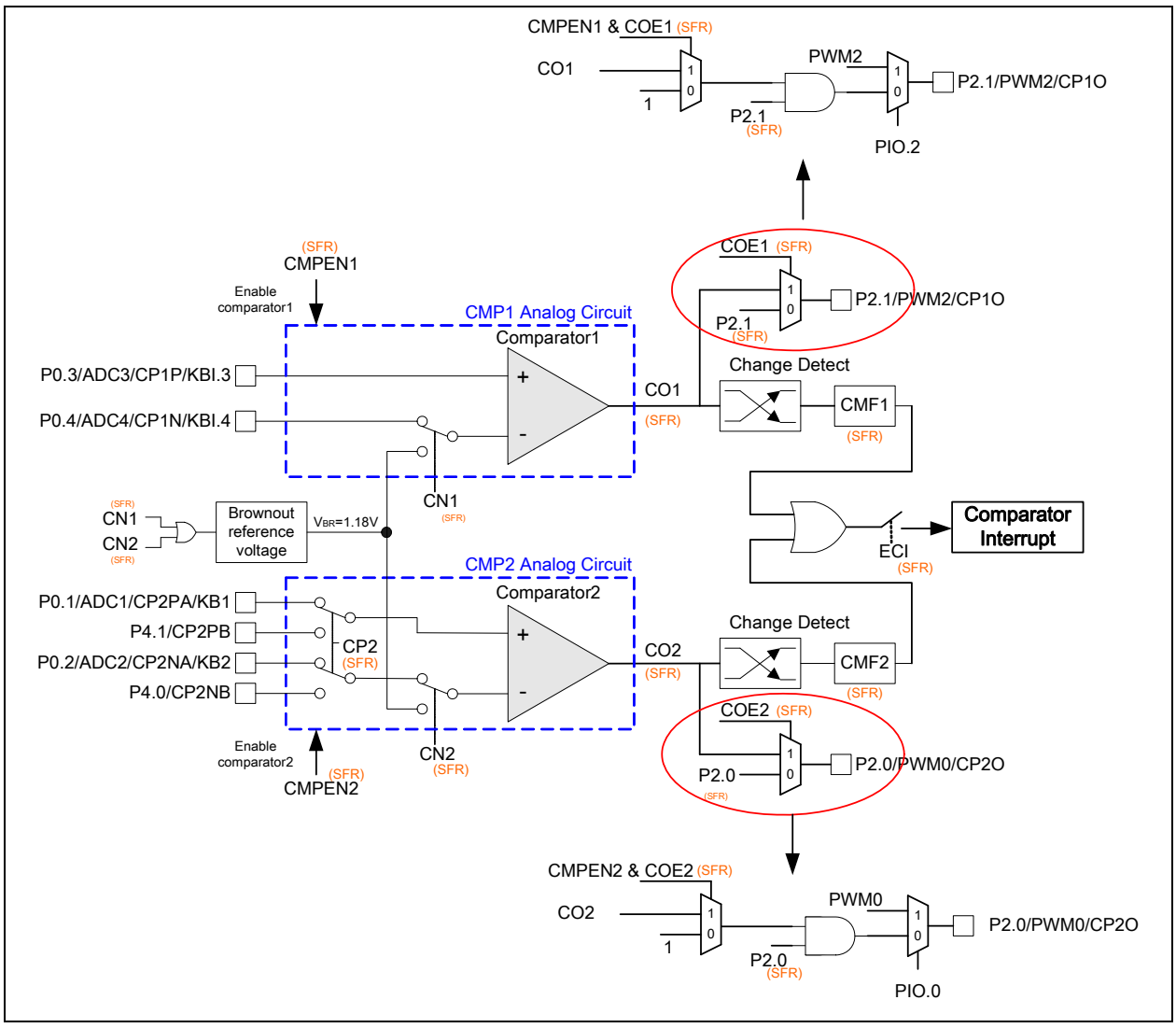


Figure 27-1: Comparators block diagram

Note: When using the both comparators, user should set SFR PADIDS.1-2, PADIDS.3-4 or AUXR2.4-5 bits accordingly to disable digital input at the comparators' input pins.

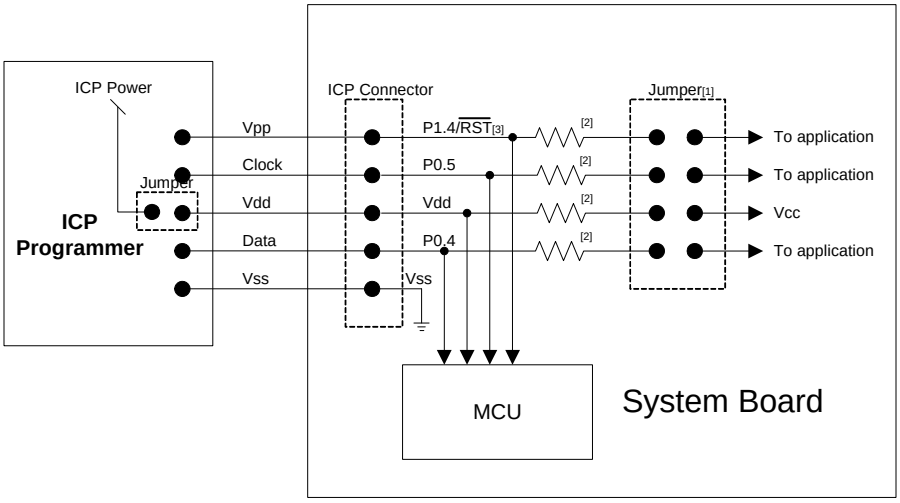
Both comparators have hysterisis function that is controllable through HYSEN1 and HYSEN2 bits.

28 ICP (IN-CIRCUIT PROGRAM) FLASH PROGRAM

The ICP(In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is mode input, shared with /RST pin, which is up to 11 volt in ICP working period. One is clock input, shared with P0.5, which accepts serial clock from external device. Another is data I/O pin, shared with P0.4, that an external ICP program tool shifts in/out data via P0.4 synchronized with clock(P0.5) to access the Flash EPROM of N79E235 series.

Nuvoton's ICP dongle programmer does not provide power to target board. So system must supply power during doing ICP function. User can refer to http://www.nuvoton.com/hq/enu/ProductAndSales/ProductLines/ConsumerElectronicsIC/Microcontroller/TechnicalSupportingFile.htm to get more data

User may refer to http://www.manley.com.cn/english/index.asp for N_LINK, another ICP Programmer Tool by 3rd party provided.



Note:
1. Circuitry separation is optionally needed between ICP and application during ICP operation
2. Resistor is optional by application
3. Voltage of P1.4 is up to about 11V during ICP peration

Notes:

- When using ICP to upgrade code, the P1.4, P0.4 and P0.5 must be taken within design system board.
- After program finished by ICP, to suggest system power must be off and remove ICP connector then power on.
- It is recommended that user performs erase function and programming configure bits continuously without any interruption.
- During ICP mode, all PWM pins will be tri-stated.

29 CONFIG BITS

The N79E235 series has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below. The data of these bytes may be read by the MOVX instruction at the addresses.

29.1 CONFIG0

CONFIG0

Bit:	7	6	5	4	3	2	1	0
	WDTCK	RPD	PRHI	CBOV1	CBOV0	BPFR	Fosc1	Fosc0

BIT	NAME	FUNCTION
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 500KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.4. 1: Disable Reset function of Pin 1.4, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4-3	CBOV.1-0	Brownout Voltage Select bits: 00: Brownout detect voltage is 4.5V. 01: Brownout detect voltage is 3.8V. 1x: Brownout detect voltage is 2.6V (default).
2	BPFR	Bypass Clock Filter of Crystal Oscillator bit: 0: Disable Clock Filter. 1: Enable Clock Filter. (default)

<table>
<tr>
<td>1-0</td>
<td>Fosc1-0</td>
<td>CPU Oscillator Type Select bits
<table>
<tr><th>FOSC1</th><th>FOSC0</th><th>OSC SOURCE</th></tr>
<tr><td>0</td><td>0</td><td>4MHz ~ 40MHz crystal</td></tr>
<tr><td>0</td><td>1</td><td>Internal RC Oscillator, 22.1184MHz/11.0592MHz</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>External Oscillator in XTAL1</td></tr>
</table>
</td>
</tr>
</table>

29.2 CONFIG1

CONFIG1

Bit:	7	6	5	4	3	2	1	0
	C7	C6	FS1	-	SCF	-	PWM_Even	PWM_Odd

BIT	NAME	FUNCTION
7	C7	16K/8K-Byte AP Flash EPROM Lock bit: 0: The 16K/8K-byte embedded AP Flash EPROM and Config registers are protected from reading through any programming tool. 1: The 16K/8K-byte embedded AP Flash and Config registers are not locked that can be read by external programming tool.
6	C6	256-Byte Data Flash Lock bit: 0: The 256-byte Data Flash is protected from reading through any programming tool. 1: The 256-byte Data Flash is not locked that can be read by external programming tool. Refer to the below table for more detail.
5	FS1	***Internal Oscillator 22.1184MHz/11.0592MHz select bit*** 0: Internal OSC frequency is 11.0592MHz. 1: Internal OSC frequency is 22.1184MHz.(default)
4	Reserved	Reserved bit and must be kept high.
3	SCF	***Select Crystal Frequency:*** This bit is used to adjust the oscillation circuit to meet the external crystal frequency. 0: For external crystal frequency < 24MHz. 1: For external crystal frequency > 24MHz.
2	Reserved	Reserved bit and must be kept high.
1	PWM_Even	***PWM Even channels driving mode select bit*** 1: The driving mode of even PWM pins is forced to Hi-Z mode all the time. 0: The driving mode of even PWM pins is controlled by output mode register (PxMy). This bit is latched to SFR PWMCON3.HZ_Even after all reset.

0	PWM_Odd	***PWM Odd channels driving mode select bit*** 1: The driving mode of odd PWM pins is forced to Hi-Z mode all the time. 0: The driving mode of odd PWM pins is controlled by output mode register (PxMy). This bit is latched to SFR PWMCON3.HZ_Odd after all reset.

Lock bits control list:

Bit 7	Bit 6	Function Description
1	1	Both security of 16K/8K-byte AP Flash and 256-byte Data Flash are not locked. They can be erased, programmed or read by Writer, ICP or JTAG mode.
0	1	The 16K/8K-byte AP Flash is locked but 256-byte Data Flash is not locked. **16K/8K-byte AP Flash**; • It can't be read by Writer, ICP or JTAG mode. **256-byte Data Flash**; • It can still support **program or read** by Writer, ICP or JTAG mode. • **Bank erase of this data area is supported in ICP.**
1	0	Not supported.
0	0	Both security of 16K/8K-byte AP Flash and 256-byte Data Flash are locked. They can't be read by Writer, ICP or JTAG mode.

30 ELECTRICAL CHARACTERISTICS

30.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

30.2 DC Electrical Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage (N79E23x**A**/**RA**)	V_{DD}	2.4		5.5	V	V_{DD} =4.5V ~ 5.5V up to 40MHz V_{DD} =3.0V ~ 5.5V up to 24MHz V_{DD} =2.4V ~ 5.5V up to 8MHz
		3.0	-	5.5		Program and erase Data Flash.
Operating Current	I_{DD1}	15		22	mA	V_{DD} = 5.0V @ 40MHz, No load, /RST = Vss
				7.5	mA	V_{DD} = 3.0V @ 24MHz, No load, /RST = Vss
	I_{DD2}			40	mA	V_{DD} = 5.0V @ 40MHz, No load, /RST = V_{DD}, Run NOP
				12	mA	V_{DD} = 3.0V @ 24MHz, No load, /RST = V_{DD}, Run NOP
Idle Current	I_{IDLE}			22	mA	V_{DD} = 5.5V, 40MHz, no load
				7	mA	V_{DD} = 3.0V, 24MHz, no load
Power Down Current	I_{PWDN}		1	10	µA	V_{DD} = 5.5V, no load @ Disable BOV function
			1	10	µA	V_{DD} = 3.0V, no load @ Disable BOV function
			130		µA	V_{DD} = 5.0V, no load, 25°C With BOV function LPBOD=0
			80		µA	V_{DD} = 5.0V, no load, 25°C With BOV function LPBOD=1
Input Current P0, P1, P2, P3, P4	I_{IN1}	-50	-	+15	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.4(/RST pin)[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2 (Open Drain), P3, P4	I_{LK}	-2	-	+2	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4	I_{TL} [*3]	-500	-	-200	µA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage P0, P1, P2, P3, P4 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4 (TTL input)	V_{IH1}	2.2	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input), /RST	V_{ILS}	-0.5	-	0.3V_{DD}	V	

Positive going threshold (Schmitt input), /RST	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		$0.2V_{DD}$		V	
Source Current P0, P1, P2, P3, P4 (Quasi-bidirectional Mode)	I_{SR11}	-150	-210	-360	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-35	-40	-60	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-18	-27	-40	μA	V_{DD} = 2.4V, V_S = 2.0V
Source Current P0, P1, P2, P3, P4 (Push-pulll Mode)	I_{SR21}	12	16	20	mA	V_{DD} = 4.5V, V_S = 3.0V
	I_{SR22}	6	8	10	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	2.5	3.5	4.5	mA	V_{DD} = 2.4V, V_S = 2.0V
Sink Current P0, P1, P2, P3, P4 (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	18	25	32	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	15	20	25	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	13	17	21	mA	V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV[1:0] =0xb	$V_{BO2.5}$	2.40	2.5	2.60	V	
Brownout voltage with BOV[1:0] =10b	$V_{BO3.8}$	3.60	3.75	3.90	V	
Brownout voltage with BOV[1:0] =11b	$V_{BO4.5}$	4.30	4.5	4.70	V	
Hysterisis range of BOD voltage	V_{Bh}	50	-	140	mV	V_{DD} = 2.4V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

30.3 ADC Converter DC Electrical Characteristics

(V_{DD}–V_{SS} = 3.3~5V, TA = -40~85°C, ADC clock=12MHz, AV_{DD} is independent[1], unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVin	AV_{SS}-0.2		AV_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	-	20MHz	Hz	V_{DD} = 5.0V.
				12MHz		V_{DD} = 3.3V.
ADC Current consumption (ADC enable)	I_{ADC}		3.0		mA	V_{DD}=5.0V ADCCLK=11.059Mhz ADC input=GND
	I_{ADC}		2.2		mA	V_{DD}=3.3V ADCCLK=11.059Mhz ADC input=GND
Conversion time	t_C		$34t_{ADC}$[2]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-0.5	-	+3.0	LSB	
Gain error	Ge	-0.6	-	+0.1	%	
Absolute voltage error	Ae	-4 -5	-	+4 +5	LSB	V_{DD} = 5.0V. V_{DD} = 3.3V.

Notes:

1. AV_{DD} needs clear power*, power noise is smaller than 0.5LSB for test condition of resolution. Suggest don't connect AV_{DD} to DV_{DD} directly without any isolation device

*clear power：

For test 8-bit resolution of 10bit-SARADC, power noise need smaller than 2LSB of ADC.

If AV_{DD} is 5V, power noise need small than 9.5mV.

2. t_{ADC}: The period time of ADC input clock.

30.4 Comparator Electrical Characteristics

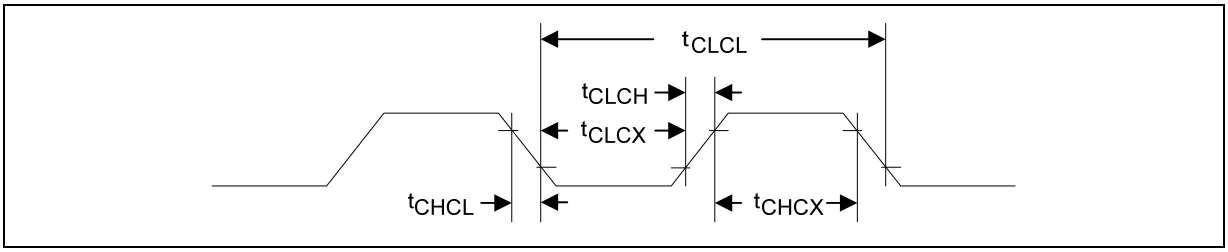
(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fcpu = 16MHz, unless otherwise specified.)

PARAMETERS	SPECIFICATION			UNIT	CONDITIONS
	MIN.	TYP.	MAX.		
Temperature	-40	25	85	℃	
V_{DD}	2.4	3	5.5	V	
Power current	-	20	40	uA	
Output swing	0.1	-	V_{DD}-0.1	V	
Input common mode range(V_{CM})	0.1	-	V_{DD}-1.3	V	
DC gain	-	70	-	dB	Design guarantee
Propagation delay	-	200	-	ns	@ V_{CM} =1V & VDIFF=0.1V
Comparison voltage	10	20	-	mV	20mV@ V_{CM} =1V 50mV@ V_{CM} =0.1V 50mV@ V_{CM} =V_{DD}-1.3 @10mV for non-hysteresis
Hysteresis	-	±20	±35	mV	@ V_{CM}=0.5V ~ V_{DD}-1.3V
Wake up time	-	-	2	us	@CINP=0.9V & CINN=1V
Brownout reference voltage[1] (V_{BR})	1.13 1.11	1.16 1.14	1.20 1.18	V	V_{DD} = 5.0V. V_{DD} = 3.0V.

Notes:

1. Value is guideline only and not tested.

30.5 AC Electrical Characteristics



Note: Duty cycle is 50%.

30.5.1 External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5	-	-	nS	
Clock Low Time	t_{CLCX}	12.5	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

30.5.2 Supplied Voltage-Frequency

Supplied Voltage V_{DD}	Operating CPU Clock			UNIT
	MIN.	TYP.	MAX.	
V_{DD} =4.5V ~ 5.5V			40	MHz
V_{DD} =3.0V ~ 5.5V			24	MHz
V_{DD} =2.4V ~ 5.5V			8	MHz

30.5.3 Internal RC Oscillator Characteristics

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
Fosc of N79E235 On-chip RC oscillator without calibration. Nominal value of Fosc is about 22MHz/11MHz.	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
Fosc of N79E235R On-chip RC oscillator with calibration[1,2] Nominal value of Fosc is 22.1184MHz/11.0592MHz	-2		2	%	V_{DD}=3.3V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-8		8	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:
1. These values are for design guidance only and are not tested.

30.5.4 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
>24MHz	5p~15p	5p~15p	1.8k~2.2k
4MHz ~ 24 MHz	without	without	without

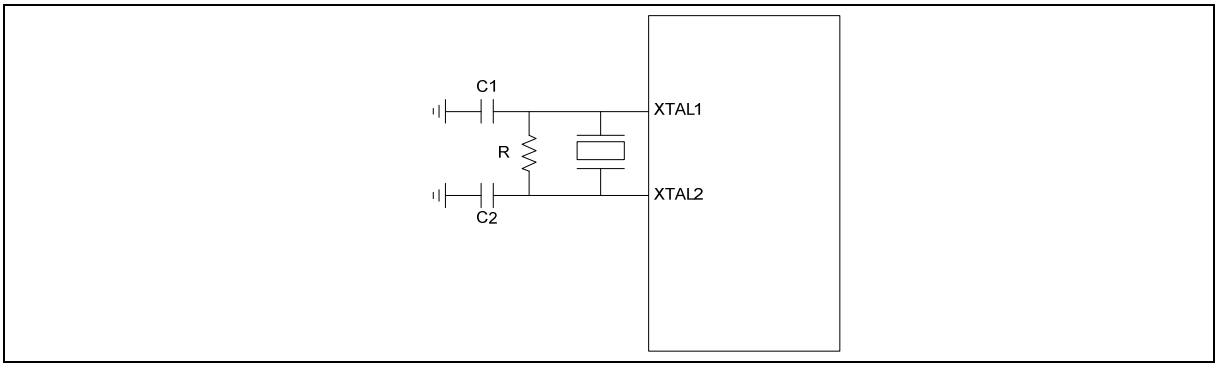
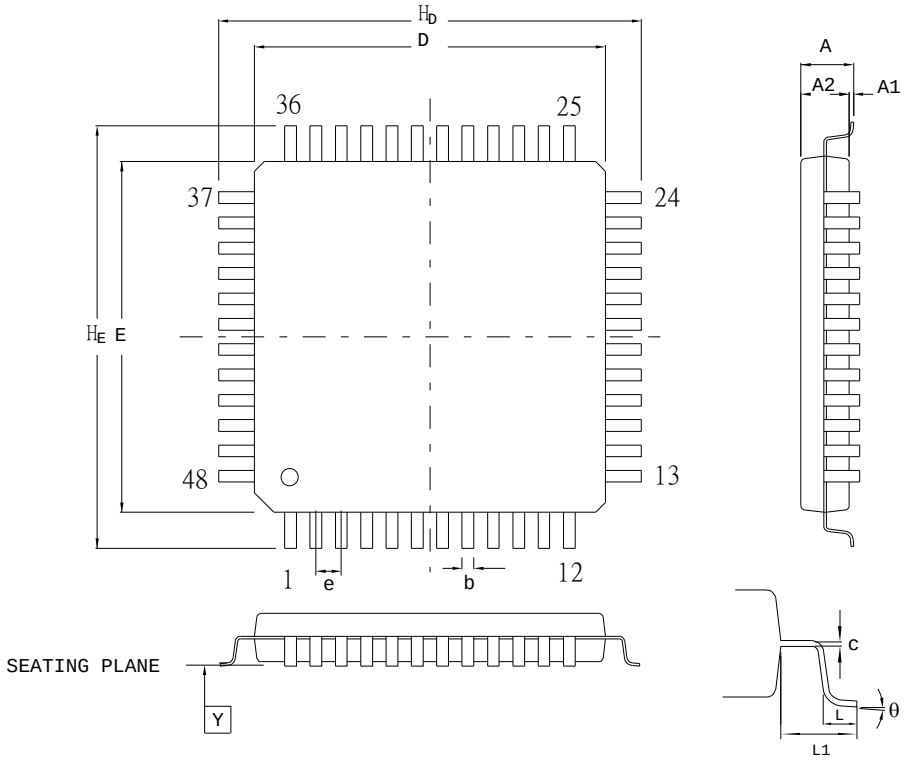


Figure 30-1 Typical Crystal Application Circuit

31 PACKAGE DIMENSIONS

31.1 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

32 APPLICATION NOTE

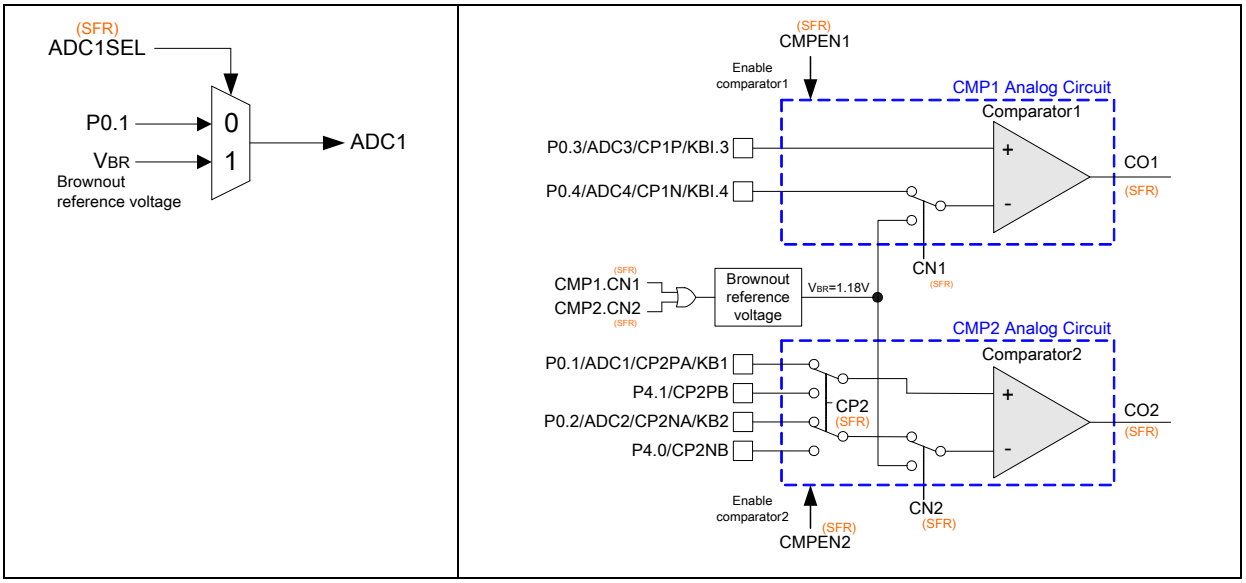
32.1 Programming note

32.1.1 Access to brownout reference voltage

This device provides brownout reference voltage(V_{BR}) to be the source of ADC1 or comparator reference input. When MCU switch ADC1 source to VBR or comparators negative inputs to V_{BR} by setting AUXR2.ADC1SEL(FFH.1) or CMP1.CN1(ACH.3) or CMP2.CN2(ADH.3) to high, the switching transient may induce a noise result Brownout detector misjudges V_{DD}. Below it lists a recommended programming flow to avoid misjudge of brownout detection when CPU accesses to V_{BR}.

Program flow to access brownout reference voltage(V_{BR})

1. Select brownout interrupt instead of brownout reset. (AUXR1.BOI=1)
2. Disable brownout interrupt. (IE.EBO=0)
3. Set ADC1 source from V_{BR}. (AUXR2.ADC1SEL=1)
4. Select ADC1 to be converted by ADC. (ADCCON=0x01) (It might induce a switch noise here)
5. Check and wait AUXR1.BOS=0. (it is not longer than one instruction time)
6. Clear brownout flag PCON.BOF. (PCON &= 0xDF)
7. Enable brownout interrupt if necessary. (IE.EBO=1)
8. Select brownout reset if necessary. (AUXR1.BOI=0)



32.1.2 ADC programming note

- SFR ADCCON1(E3H), ADCDLY(AFH) and bit AUXR1(A2H).RCCLK can be set/cleared only when ADC circuit is not enabled(AUXR1.ADCEN=0).

- The ADC1 alternative input source will come from Brownout Reference Voltage, VBR. It can be selected through AUXR2.ADC1SEL bit. Refer to Figure 26-3: ADC1 source selections for selecting ADC1 source.

32.2 MCU hardware note

32.2.1 Types of I/O pins

Most of I/O pins except power pins in this device support 4 I/O types, Quasi-bidirection(default), open-drain, push-pull and input only which are defined by registers PxMy where x represents P0~P4, y=1~2. The exception are **P1.4**(/RST) pin only support **input** mode, I/O pins of **P1.5**(T0/SCL/BKP1) and **P1.6**(INT0/ SDA) support **open-drain type only**.

33 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V01	February 3, 2010	-	a. Initial Issued

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